- State-of-the-Art *EPIC-IIB™* BiCMOS Design **Significantly Reduces Power Dissipation**
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015
- Latch-Up Performance Exceeds 500 mA Per **JEDEC Standard JESD-17**
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$
- **High-Impedance State During Power Up** and Power Down
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OI</sub>)
- **Package Options Include Plastic** Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs

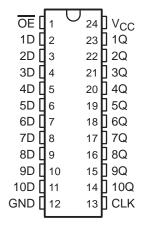
### description

These 10-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

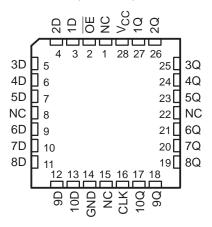
The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the devices provide true data at the Q outputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

SN54ABT821 . . . JT OR W PACKAGE SN74ABT821A . . . DB. DW. OR NT PACKAGE (TOP VIEW)



SN54ABT821 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

OE does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V<sub>CC</sub> is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT821 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT821A is characterized for operation from -40°C to 85°C.



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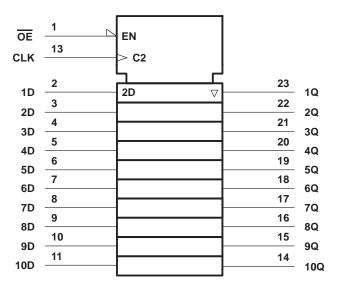
EPIC-IIB is a trademark of Texas Instruments Incorporated



## FUNCTION TABLE (each flip-flop)

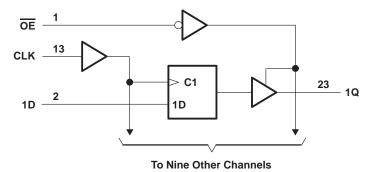
	INPUTS	OUTPUT	
OE	CLK	Q	
L	$\uparrow$	Н	Н
L	$\uparrow$	L	L
L	H or L	Χ	Q <sub>0</sub>
Н	X	Χ	Z

## logic symbol†



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, NT, and W packages.

## logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, NT, and W packages.



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	$-0.5 \text{ V to 7 V}$
Voltage range applied to any output in the high or power-off state, VO	. $-0.5\ V$ to $5.5\ V$
Current into any output in the low state, IO: SN54ABT821	96 mA
SN74ABT821A	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	−50 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2): DB package	104°C/W
DW package	81°C/W
NT package	67°C/W
Storage temperature range, T <sub>stq</sub>	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

		SN54A	BT821	SN74AB	T821A	UNIT
		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
VI	Input voltage	0	VCC	0	VCC	V
loн	High-level output current		-24		-32	mA
loL	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		10		10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate	200		200		μs/V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## SN54ABT821, SN74ABT821A **10-BIT BUS-INTERFACE FLIP-FLOPS** WITH 3-STATE OUTPUTS

SCBS193E - FEBRUARY 1991 - REVISED MAY 1997

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COND	NTIONE	Т	A = 25°C	;	SN54A	BT821	SN74AB	T821A	UNIT
PARAMETER	TEST COND	THONS	MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNII
VIK	V <sub>CC</sub> = 4.5 V,	$I_{I} = -18 \text{ mA}$			-1.2		-1.2		-1.2	V
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.5			2.5		2.5		
\/a	$V_{CC} = 5 V$ ,	$I_{OH} = -3 \text{ mA}$	3			3		3		V
VOH	V <sub>CC</sub> = 4.5 V	$I_{OH} = -24 \text{ mA}$	2			2				V
	VCC = 4.5 V	$I_{OH} = -32 \text{ mA}$	2*					2		
VoL	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA			0.55		0.55			V
VOL	VCC = 4.5 V	I <sub>OL</sub> = 64 mA			0.55*				0.55	V
V <sub>hys</sub>				100						mV
lį	$V_{CC} = 0 \text{ to } 5.5 \text{ V},$	$V_I = V_{CC}$ or GND			±1		±1		±1	μΑ
lozpu <sup>‡</sup>	$V_{CC} = 0 \text{ to } 2.1 \text{ V}, V_{O} = 0.5 \text{ to } 2.7 \text{ V}, \overline{OE} = X$				±50*				±50	μΑ
I <sub>OZPD</sub> ‡	$V_{CC} = 2.1 \text{ V to } 0, V_{O} = 0.5$	5 to 2.7 V, OE = X			±50*				±50	μΑ
IOZH	$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V, V}_{O} =$	2.7 V, <del>OE</del> ≥ 2 V			10		10		10	μΑ
lozL	$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V, V}_{O} =$	0.5 V, <del>OE</del> ≥ 2 V			-10		-10		-10	μΑ
l <sub>off</sub>	$V_{CC} = 0$ ,	$V_I$ or $V_O \le 4.5 \text{ V}$			±100				±100	μА
ICEX	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
IO§	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA
		Outputs high		1	250		250		250	μА
ICC	$V_{CC} = 5.5 \text{ V, I}_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low		24	38		38		38	mA
	1 1 - 100 01 0145	Outputs disabled		0.5	250		250		250	μА
ΔICC¶	$V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND				1.5		1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V			3.5						pF
Co	V <sub>O</sub> = 2.5 V or 0.5 V			7.5						pF

<sup>\*</sup> On products compliant to MIL-PRF-38535, this parameter does not apply.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V <sub>CC</sub> =	= 5 V, 25°C	SN54A	BT821	SN74AB	T821A	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	125	0	125	0	125	MHz
	Pulse duration, CLK high or low	High	2.9		2.9		2.9		no
t <sub>W</sub>	Fulse duration, CER high of low	Low	3.8		3.8		3.8		ns
t <sub>su</sub>	Setup time, data before CLK↑		2.1		2.1		2.1		ns
t <sub>h</sub>	Hold time, data after CLK↑		1.3		1.3		1.3		ns



<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> This parameter is characterized, but not production tested.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

 $<sup>\</sup>P$  This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

				SN	54ABT8	21		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>(</sub>	CC = 5 V 4 = 25°C	/, ;	MIN	MAX	UNIT
			MIN	TYP	MAX			
fmax			125			125		MHz
<sup>t</sup> PLH	CLK	Q	1.6†	4.1	5.6	1.6†	6.9	ns
<sup>t</sup> PHL	OLK	α	2.1†	4.6	6.2	2.1†	6.9	115
<sup>t</sup> PZH	ŌĒ	Q	1	3	4.5	1	6	ns
t <sub>PZL</sub>	OE .	ά	2.2	4.1	5.6	2.2	6.5	115
<sup>t</sup> PHZ	ŌĒ	Q	2.7	4.7	6.2	2.7	7	ns
t <sub>PLZ</sub>	UE UE	ζ	1.7†	4.6	6.1	1.7 <sup>†</sup>	7	115

<sup>†</sup>This data sheet limit may vary among suppliers.

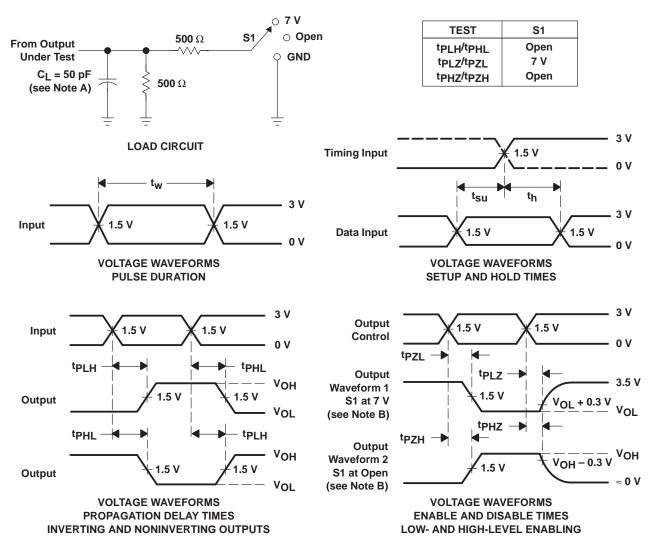
# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

				SN7	'4ABT82	21A		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>(</sub>	CC = 5 V 4 = 25°C	/, ;	MIN	MAX	UNIT
			MIN	TYP	MAX			
f <sub>max</sub>			125			125		MHz
t <sub>PLH</sub>	CLK	Q	1.6†	4.1	5.6	1.6†	6.2	ns
<sup>t</sup> PHL	OLK	ά	2.3†	4.6	6.2	2.3†	6.7	115
<sup>t</sup> PZH	ŌĒ	Q	1	3	4.5	1	5.8	ns
t <sub>PZL</sub>	OE	٧	2.2	4.1	5.6	2.2	6.3	115
<sup>t</sup> PHZ	ŌĒ	Q	2.7	4.7	6.2	2.7	6.7	ns
t <sub>PLZ</sub>	OE .	ď	1.7†	4.6	6.1	1.7	6.5	115

<sup>†</sup> This data sheet limit may vary among suppliers.



#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_{Q}$  = 50  $\Omega$ ,  $t_{f}$   $\leq$  2.5 ns,  $t_{f}$   $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
5962-9469101QLA	Active	Production	CDIP (JT)   24	15   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9469101QL A SNJ54ABT821JT
SN74ABT821ADW	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT821A
SN74ABT821ADW.B	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT821A
SN74ABT821ADWR	Active	Production	SOIC (DW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT821A
SN74ABT821ADWR.B	Active	Production	SOIC (DW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT821A
SNJ54ABT821JT	Active	Production	CDIP (JT)   24	15   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9469101QL A SNJ54ABT821JT

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



## PACKAGE OPTION ADDENDUM

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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## **PACKAGE MATERIALS INFORMATION**

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## **TAPE AND REEL INFORMATION**





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT821ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

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## \*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
ı	SN74ABT821ADWR	SOIC	DW	24	2000	350.0	350.0	43.0	

## **PACKAGE MATERIALS INFORMATION**

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## **TUBE**



## \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ABT821ADW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ABT821ADW.B	DW	SOIC	24	25	506.98	12.7	4826	6.6

## JT (R-GDIP-T\*\*)

#### 24 LEADS SHOWN

### **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

DW (R-PDSO-G24)

## PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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