

# SN54ABT240, SN74ABT240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS098I – JANUARY 1991 – REVISED JUNE 2002

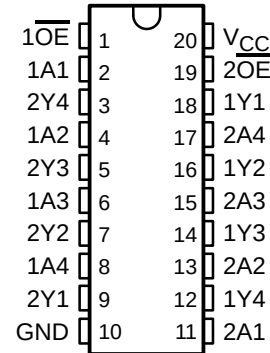
- Typical  $V_{OLP}$  (Output Ground Bounce)  
 $<1\text{ V}$  at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

## description

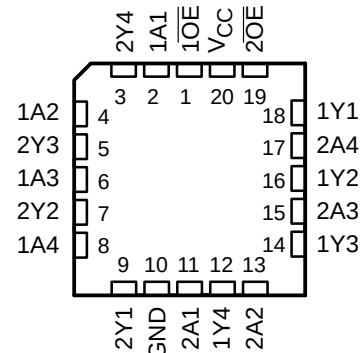
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the SN54ABT241, SN74ABT241A, SN54ABT244, and SN74ABT244A, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ( $\overline{OE}$ ) inputs, and complementary OE and  $\overline{OE}$  inputs.

The SN54ABT240 and SN74ABT240A are organized as two 4-bit buffers/line drivers with separate  $\overline{OE}$  inputs. When  $\overline{OE}$  is low, the devices pass inverted data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

SN54ABT240 . . . J OR W PACKAGE  
 SN74ABT240A . . . DB, DW, N, NS, OR PW PACKAGE  
 (TOP VIEW)



SN54ABT240 . . . FK PACKAGE  
 (TOP VIEW)



## ORDERING INFORMATION

| $T_A$          | PACKAGE <sup>†</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------|---------------|-----------------------|------------------|
| -40°C to 85°C  | PDIP – N             | Tube          | SN74ABT240AN          | SN74ABT240AN     |
|                | SOIC – DW            | Tube          | SN74ABT240ADW         | ABT240A          |
|                |                      | Tape and reel | SN74ABT240ADWR        |                  |
|                | SOP – NS             | Tape and reel | SN74ABT240ANSR        | ABT240A          |
|                | SSOP – DB            | Tape and reel | SN74ABT240ADBR        | AB240A           |
| -55°C to 125°C | TSSOP – PW           | Tape and reel | SN74ABT240APWR        | AB240A           |
|                | CDIP – J             | Tube          | SNJ54ABT240J          | SNJ54ABT240J     |
|                | CFP – W              | Tube          | SNJ54ABT240W          | SNJ54ABT240W     |
|                | LCCC – FK            | Tube          | SNJ54ABT240FK         | SNJ54ABT240FK    |

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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 On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

description (continued)

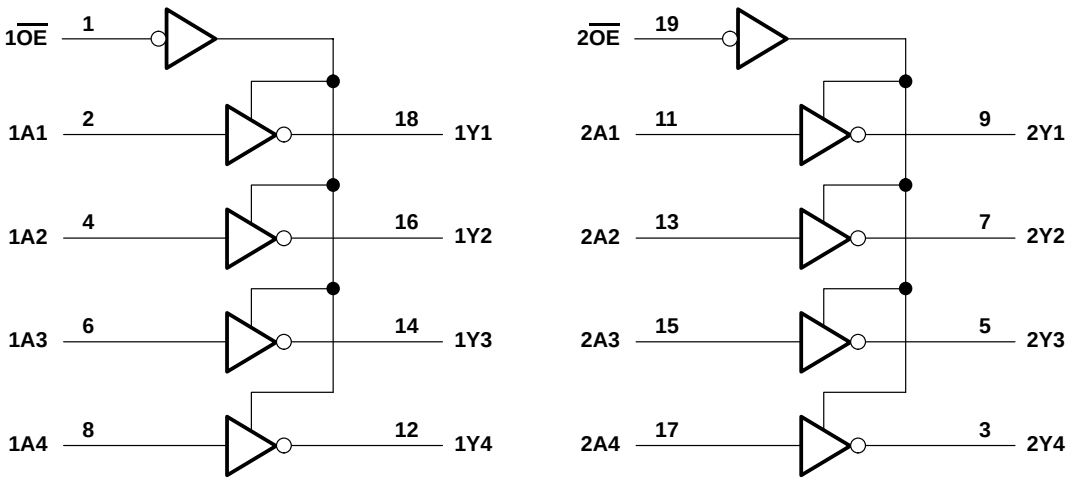
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE  
(each buffer)

| INPUTS          |   | OUTPUT |
|-----------------|---|--------|
| $\overline{OE}$ | A | Y      |
| L               | H | L      |
| L               | L | H      |
| H               | X | Z      |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                                     |                 |
|-------------------------------------------------------------------------------------|-----------------|
| Supply voltage range, $V_{CC}$                                                      | –0.5 V to 7 V   |
| Input voltage range, $V_I$ (see Note 1)                                             | –0.5 V to 7 V   |
| Voltage range applied to any output in the high-impedance or power-off state, $V_O$ | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$ : SN54ABT240                        | 96 mA           |
| SN74ABT240A                                                                         | 128 mA          |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                                         | –18 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                                        | –50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package                   | 70°C/W          |
| DW package                                                                          | 58°C/W          |
| N package                                                                           | 69°C/W          |
| NS package                                                                          | 60°C/W          |
| PW package                                                                          | 83°C/W          |
| Storage temperature range, $T_{stg}$                                                | –65°C to 150°C  |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

# SN54ABT240, SN74ABT240A

## OCTAL BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions (see Note 3)

|                 |                                    |                 | SN54ABT240 |                 | SN74ABT240A |                 | UNIT |
|-----------------|------------------------------------|-----------------|------------|-----------------|-------------|-----------------|------|
|                 |                                    |                 | MIN        | MAX             | MIN         | MAX             |      |
| V <sub>CC</sub> | Supply voltage                     |                 | 4.5        | 5.5             | 4.5         | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage           |                 | 2          |                 | 2           |                 | V    |
| V <sub>IL</sub> | Low-level input voltage            |                 |            | 0.8             |             | 0.8             | V    |
| V <sub>I</sub>  | Input voltage                      |                 | 0          | V <sub>CC</sub> | 0           | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current          |                 |            | –24             |             | –32             | mA   |
| I <sub>OL</sub> | Low-level output current           |                 |            | 48              |             | 64              | mA   |
| Δt/Δv           | Input transition rise or fall rate | Outputs enabled |            | 5               |             | 5               | ns/V |
| T <sub>A</sub>  | Operating free-air temperature     |                 | –55        | 125             | –40         | 85              | °C   |

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER          |                | TEST CONDITIONS                                                                      | T <sub>A</sub> = 25°C |      |       | SN54ABT240 |      | SN74ABT240A |      | UNIT |
|--------------------|----------------|--------------------------------------------------------------------------------------|-----------------------|------|-------|------------|------|-------------|------|------|
|                    |                |                                                                                      | MIN                   | TYP† | MAX   | MIN        | MAX  | MIN         | MAX  |      |
| V <sub>IK</sub>    |                | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = –18 mA                                     |                       |      | –1.2  |            | –1.2 |             | –1.2 | V    |
| V <sub>OH</sub>    |                | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –3 mA                                     | 2.5                   |      |       | 2.5        |      | 2.5         |      | V    |
|                    |                | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = –3 mA                                       | 3                     |      |       | 3          |      | 3           |      |      |
|                    |                | V <sub>CC</sub> = 4.5 V                                                              |                       |      | 2     | 2          |      |             |      |      |
|                    |                |                                                                                      |                       |      | 2*    |            |      | 2           |      |      |
| V <sub>OL</sub>    |                | V <sub>CC</sub> = 4.5 V                                                              |                       |      | 0.55  | 0.55       |      |             |      | V    |
|                    |                |                                                                                      |                       |      | 0.55* |            |      | 0.55        |      |      |
| V <sub>hys</sub>   |                |                                                                                      |                       | 100  |       |            |      |             |      | mV   |
| I <sub>I</sub>     |                | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND                     |                       |      | ±1    |            | ±1   |             | ±1   | μA   |
| I <sub>OZH</sub>   |                | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V                                      |                       |      | 10    | 10         |      | 10          |      | μA   |
| I <sub>OZL</sub>   |                | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V                                      |                       |      | –10   | –10        |      | –10         |      | μA   |
| I <sub>off</sub>   |                | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V                        |                       |      | ±100  |            |      | ±100        |      | μA   |
| I <sub>CEX</sub>   |                | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V                                      |                       |      | 50    | 50         |      | 50          |      | μA   |
| I <sub>O</sub> ‡   |                | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V                                      | –50                   | –100 | –180  | –50        | –180 | –50         | –180 | mA   |
| I <sub>CC</sub>    |                | V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND |                       |      | 1     | 250        | 250  | 250         |      | μA   |
|                    |                |                                                                                      |                       |      | 24    | 30         | 30   | 30          |      | mA   |
|                    |                |                                                                                      |                       |      | 0.5   | 250        | 250  | 250         |      | μA   |
| ΔI <sub>CC</sub> § | Data inputs    | V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND  |                       |      | 1.5   | 1.5        |      | 1.5         |      | mA   |
|                    |                |                                                                                      |                       |      | 0.05  | 0.05       |      | 0.05        |      |      |
|                    | Control inputs | V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND  |                       |      | 1.5   | 1.5        |      | 1.5         |      |      |
| C <sub>i</sub>     |                | V <sub>I</sub> = 2.5 V or 0.5 V                                                      |                       |      | 4     |            |      |             |      | pF   |
| C <sub>o</sub>     |                | V <sub>O</sub> = 2.5 V or 0.5 V                                                      |                       |      | 7.5   |            |      |             |      | pF   |

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



# SN54ABT240, SN74ABT240A

## OCTAL BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

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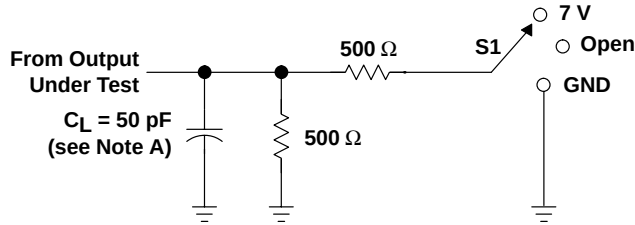
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | SN54ABT240                                      |     |     |     |     | UNIT |
|------------------|-----------------|----------------|-------------------------------------------------|-----|-----|-----|-----|------|
|                  |                 |                | V <sub>CC</sub> = 5 V,<br>T <sub>A</sub> = 25°C |     |     | MIN | MAX |      |
|                  |                 |                | MIN                                             | TYP | MAX |     |     |      |
| t <sub>PLH</sub> | A               | Y              | 1                                               | 2.9 | 4.3 | 0.8 | 5.5 | ns   |
| t <sub>PHL</sub> |                 |                | 1.6                                             | 3.1 | 4.5 | 1   | 5.5 |      |
| t <sub>PZH</sub> | $\overline{OE}$ | Y              | 1.1                                             | 3.1 | 5.8 | 0.8 | 7.5 | ns   |
| t <sub>PZL</sub> |                 |                | 1.1                                             | 2.7 | 6.2 | 0.8 | 7.7 |      |
| t <sub>PHZ</sub> | $\overline{OE}$ | Y              | 1.8                                             | 4.6 | 5.9 | 1.7 | 7   | ns   |
| t <sub>PLZ</sub> |                 |                | 1.6                                             | 4   | 5.9 | 1.3 | 7.2 |      |

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

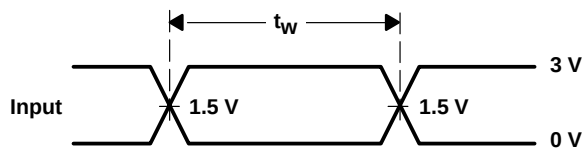
| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | SN74ABT240A                                     |     |     |     |     | UNIT |
|------------------|-----------------|----------------|-------------------------------------------------|-----|-----|-----|-----|------|
|                  |                 |                | V <sub>CC</sub> = 5 V,<br>T <sub>A</sub> = 25°C |     |     | MIN | MAX |      |
|                  |                 |                | MIN                                             | TYP | MAX |     |     |      |
| t <sub>PLH</sub> | A               | Y              | 1                                               | 2.9 | 4.1 | 1   | 4.8 | ns   |
| t <sub>PHL</sub> |                 |                | 1.6                                             | 3.1 | 4.6 | 1.6 | 4.8 |      |
| t <sub>PZH</sub> | $\overline{OE}$ | Y              | 1.1                                             | 3.1 | 4.7 | 1.1 | 5.2 | ns   |
| t <sub>PZL</sub> |                 |                | 1.1                                             | 2.7 | 5.8 | 1.1 | 6.2 |      |
| t <sub>PHZ</sub> | $\overline{OE}$ | Y              | 1.8                                             | 4.6 | 5.7 | 1.8 | 6.4 | ns   |
| t <sub>PLZ</sub> |                 |                | 1.6                                             | 4   | 5.4 | 1.6 | 5.8 |      |

## PARAMETER MEASUREMENT INFORMATION

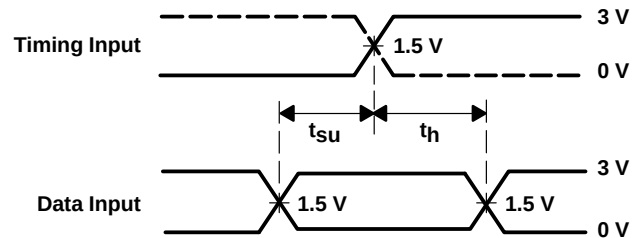


LOAD CIRCUIT

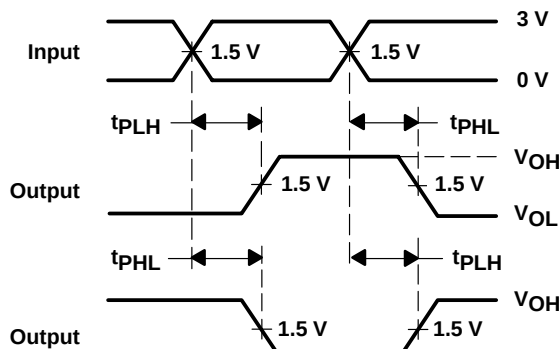
| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



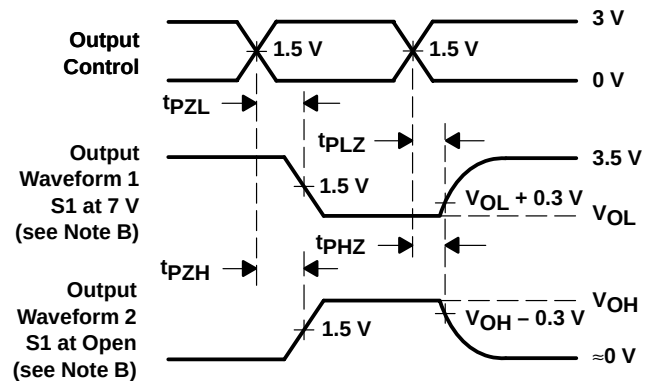
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                      |
|---------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------------------------|
| <a href="#">5962-9318801M2A</a> | Active        | Production           | LCCC (FK)   20  | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>9318801M2A<br>SNJ54ABT<br>240FK |
| <a href="#">5962-9318801MRA</a> | Active        | Production           | CDIP (J)   20   | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9318801MR<br>A<br>SNJ54ABT240J      |
| <a href="#">5962-9318801MSA</a> | Active        | Production           | CFP (W)   20    | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9318801MS<br>A<br>SNJ54ABT240W      |
| <a href="#">SN74ABT240ADBR</a>  | Active        | Production           | SSOP (DB)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AB240A                                   |
| SN74ABT240ADBR.B                | Active        | Production           | SSOP (DB)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AB240A                                   |
| SN74ABT240ADBR1G4               | Active        | Production           | SSOP (DB)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AB240A                                   |
| SN74ABT240ADBR1G4.B             | Active        | Production           | SSOP (DB)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AB240A                                   |
| <a href="#">SN74ABT240ADW</a>   | Active        | Production           | SOIC (DW)   20  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT240A                                  |
| SN74ABT240ADW.B                 | Active        | Production           | SOIC (DW)   20  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT240A                                  |
| <a href="#">SN74ABT240ADWR</a>  | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT240A                                  |
| SN74ABT240ADWR.B                | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT240A                                  |
| SN74ABT240ADWRG4                | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT240A                                  |
| SN74ABT240ADWRG4.B              | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT240A                                  |
| <a href="#">SN74ABT240AN</a>    | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74ABT240AN                             |
| SN74ABT240AN.B                  | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74ABT240AN                             |
| <a href="#">SN74ABT240ANSR</a>  | Active        | Production           | SOP (NS)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT240A                                  |
| SN74ABT240ANSR.B                | Active        | Production           | SOP (NS)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT240A                                  |
| SN74ABT240ANSRG4                | Active        | Production           | SOP (NS)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT240A                                  |
| SN74ABT240ANSRG4.B              | Active        | Production           | SOP (NS)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT240A                                  |
| <a href="#">SN74ABT240APW</a>   | Active        | Production           | TSSOP (PW)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AB240A                                   |
| SN74ABT240APW.B                 | Active        | Production           | TSSOP (PW)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AB240A                                   |
| <a href="#">SN74ABT240APWR</a>  | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AB240A                                   |
| SN74ABT240APWR.B                | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AB240A                                   |
| SN74ABT240APWRG4                | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AB240A                                   |

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                      |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------------------------|
| SN74ABT240APWRG4.B            | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AB240A                                   |
| <a href="#">SNJ54ABT240FK</a> | Active        | Production           | LCCC (FK)   20  | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>9318801M2A<br>SNJ54ABT<br>240FK |
| <a href="#">SNJ54ABT240J</a>  | Active        | Production           | CDIP (J)   20   | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9318801MR<br>A<br>SNJ54ABT240J      |
| <a href="#">SNJ54ABT240W</a>  | Active        | Production           | CFP (W)   20    | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9318801MS<br>A<br>SNJ54ABT240W      |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

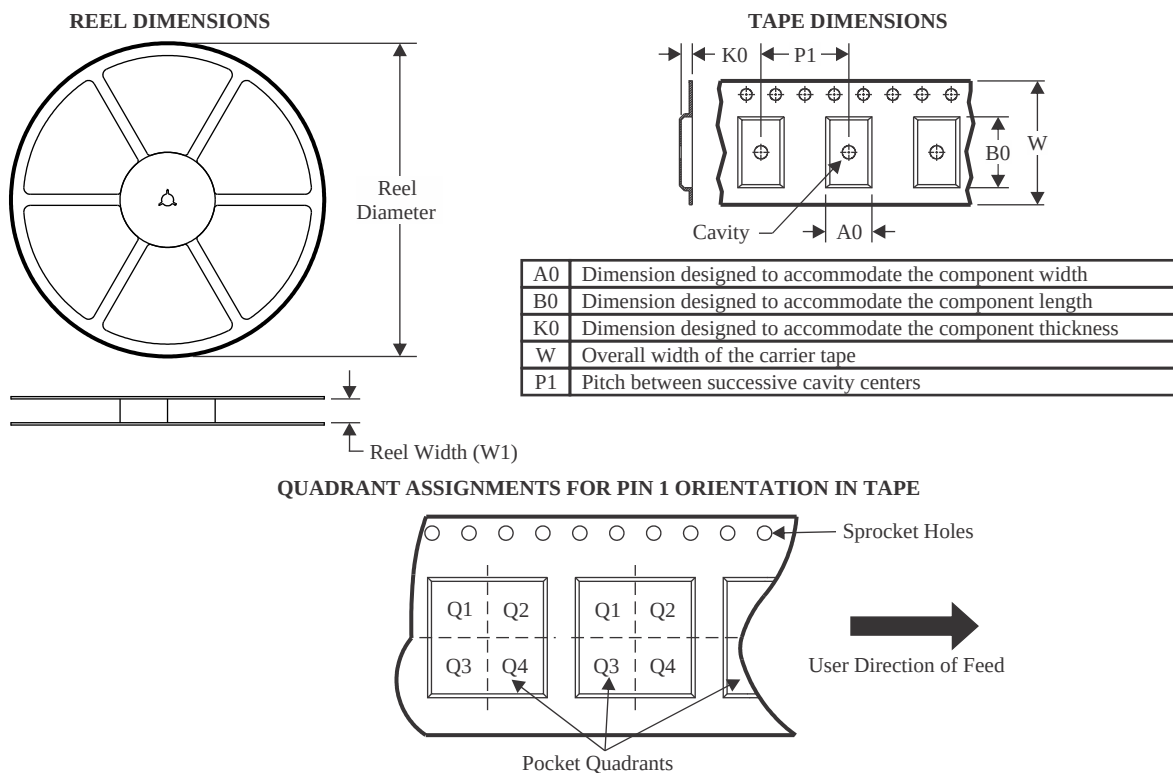
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT240ADBR    | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74ABT240ADBR1G4 | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74ABT240ADWR    | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74ABT240ADWRG4  | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74ABT240ANSR    | SOP          | NS              | 20   | 2000 | 330.0              | 24.4               | 8.4     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74ABT240ANSRG4  | SOP          | NS              | 20   | 2000 | 330.0              | 24.4               | 8.4     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74ABT240APWR    | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| SN74ABT240APWRG4  | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT240ADBR    | SSOP         | DB              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74ABT240ADBR1G4 | SSOP         | DB              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74ABT240ADWR    | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74ABT240ADWRG4  | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74ABT240ANSR    | SOP          | NS              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74ABT240ANSRG4  | SOP          | NS              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74ABT240APWR    | TSSOP        | PW              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74ABT240APWRG4  | TSSOP        | PW              | 20   | 2000 | 353.0       | 353.0      | 32.0        |

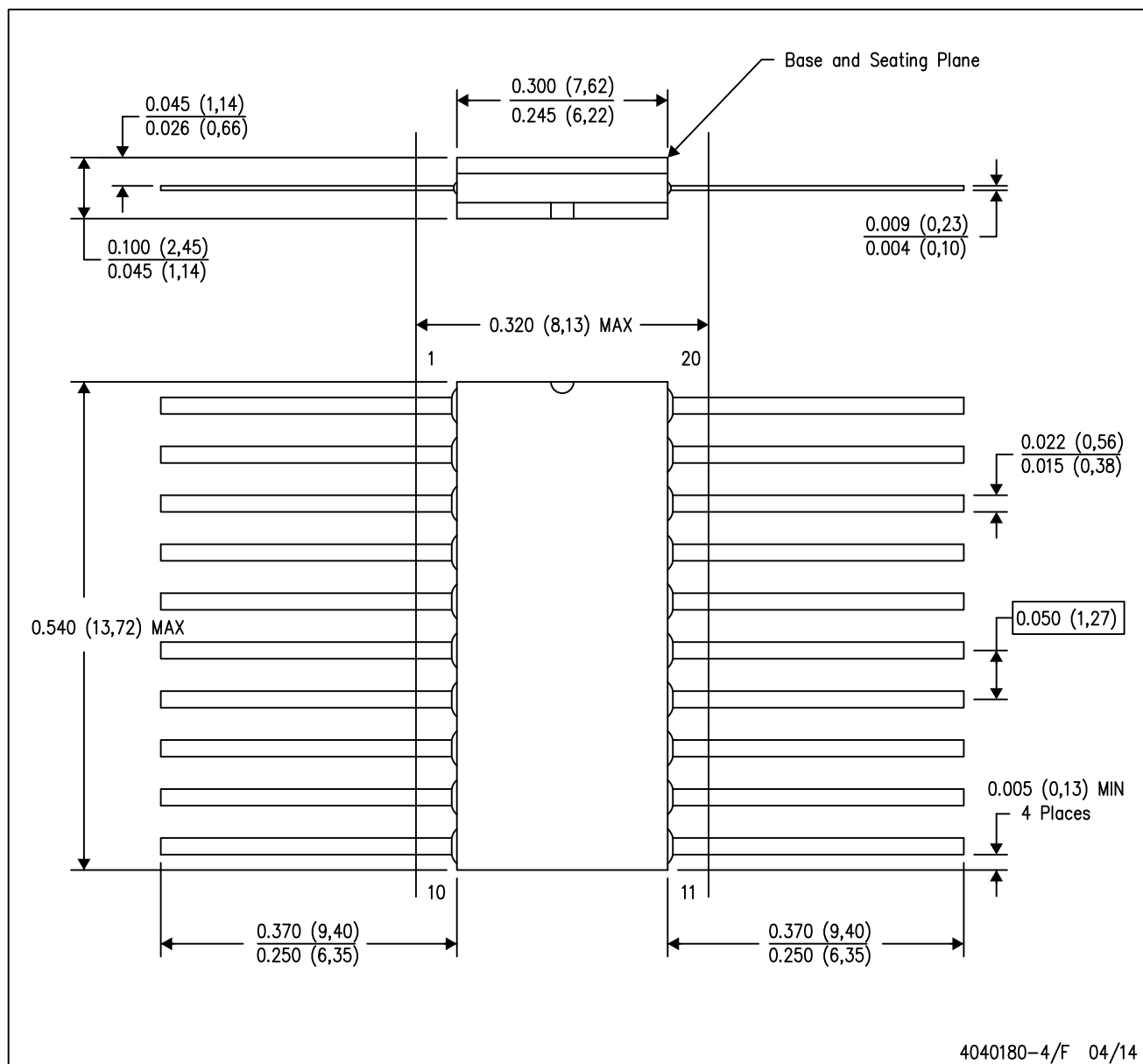
**TUBE**


\*All dimensions are nominal

| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9318801M2A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| 5962-9318801MSA | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |
| SN74ABT240ADW   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74ABT240ADW.B | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74ABT240AN    | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SN74ABT240AN.B  | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SN74ABT240APW   | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| SN74ABT240APW.B | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| SNJ54ABT240FK   | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54ABT240W    | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |

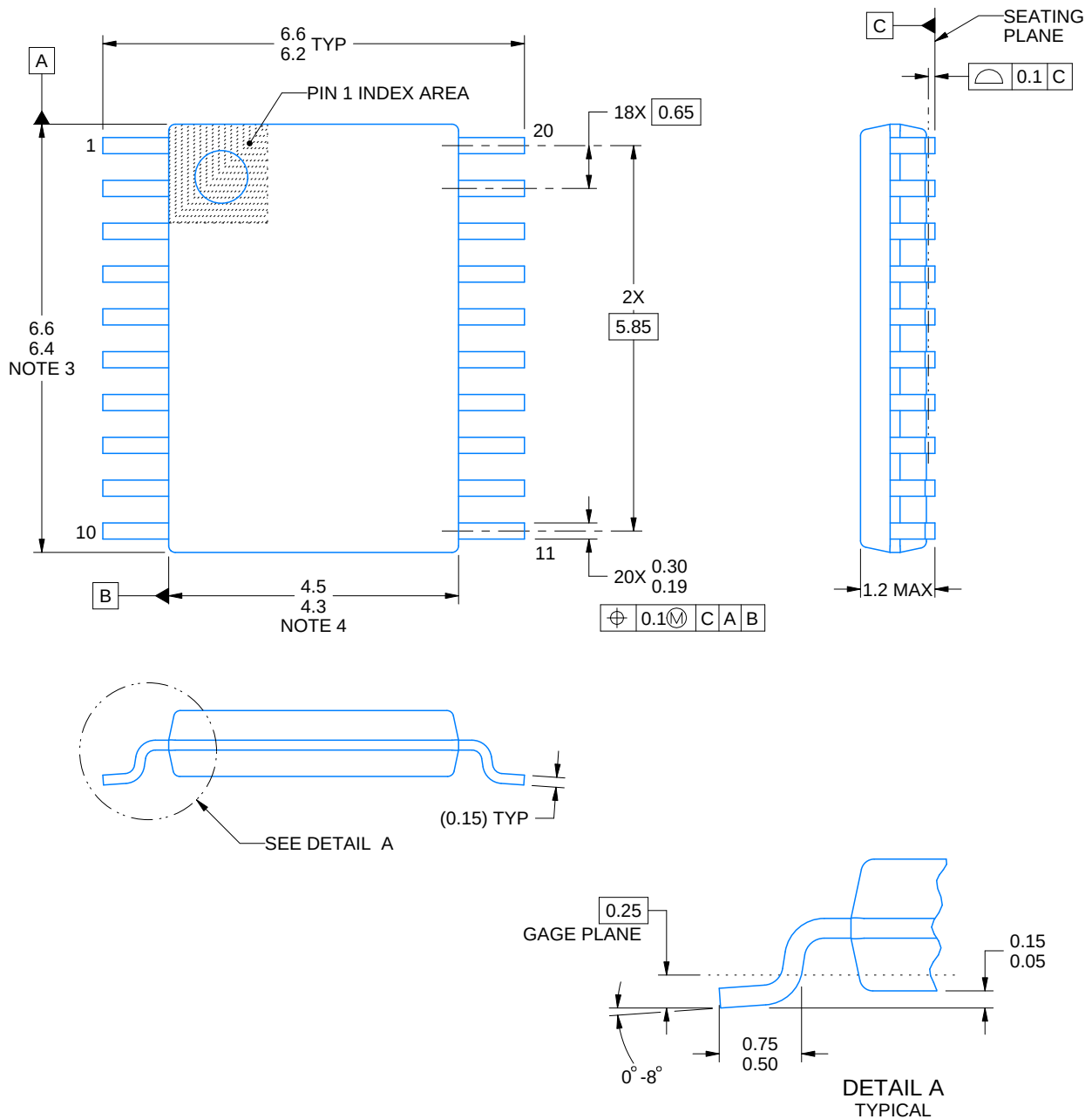
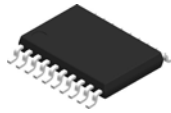
W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



4220206/A 02/2017

## NOTES:

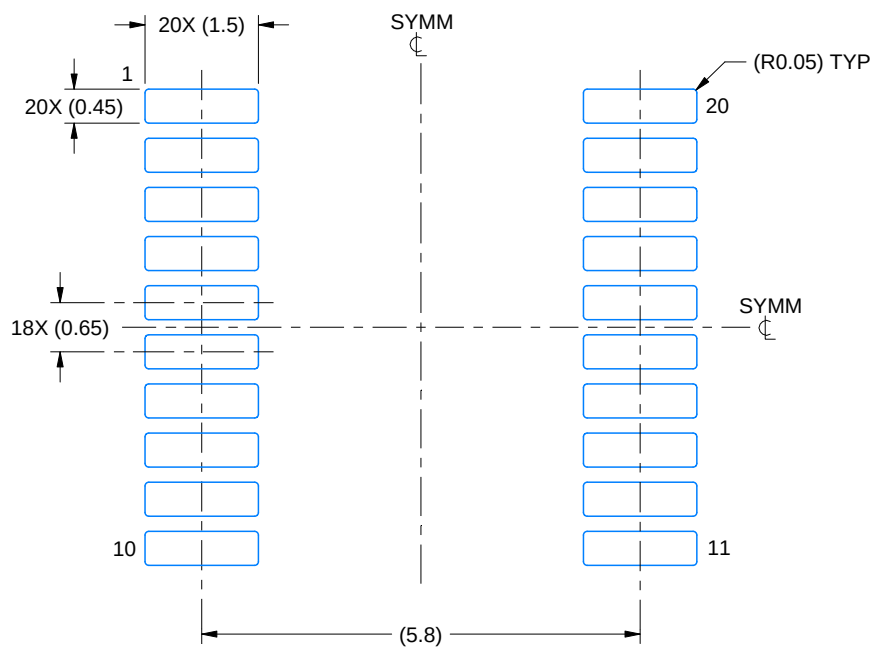
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

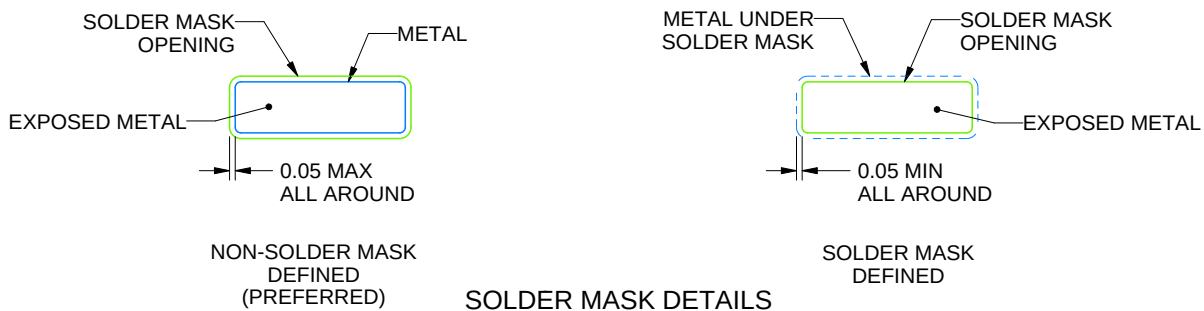
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

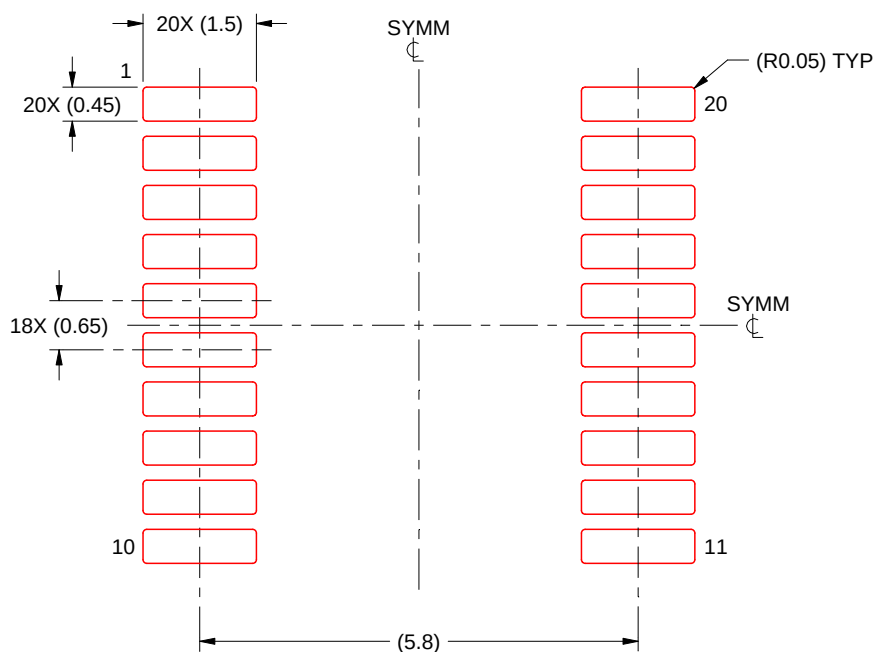
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

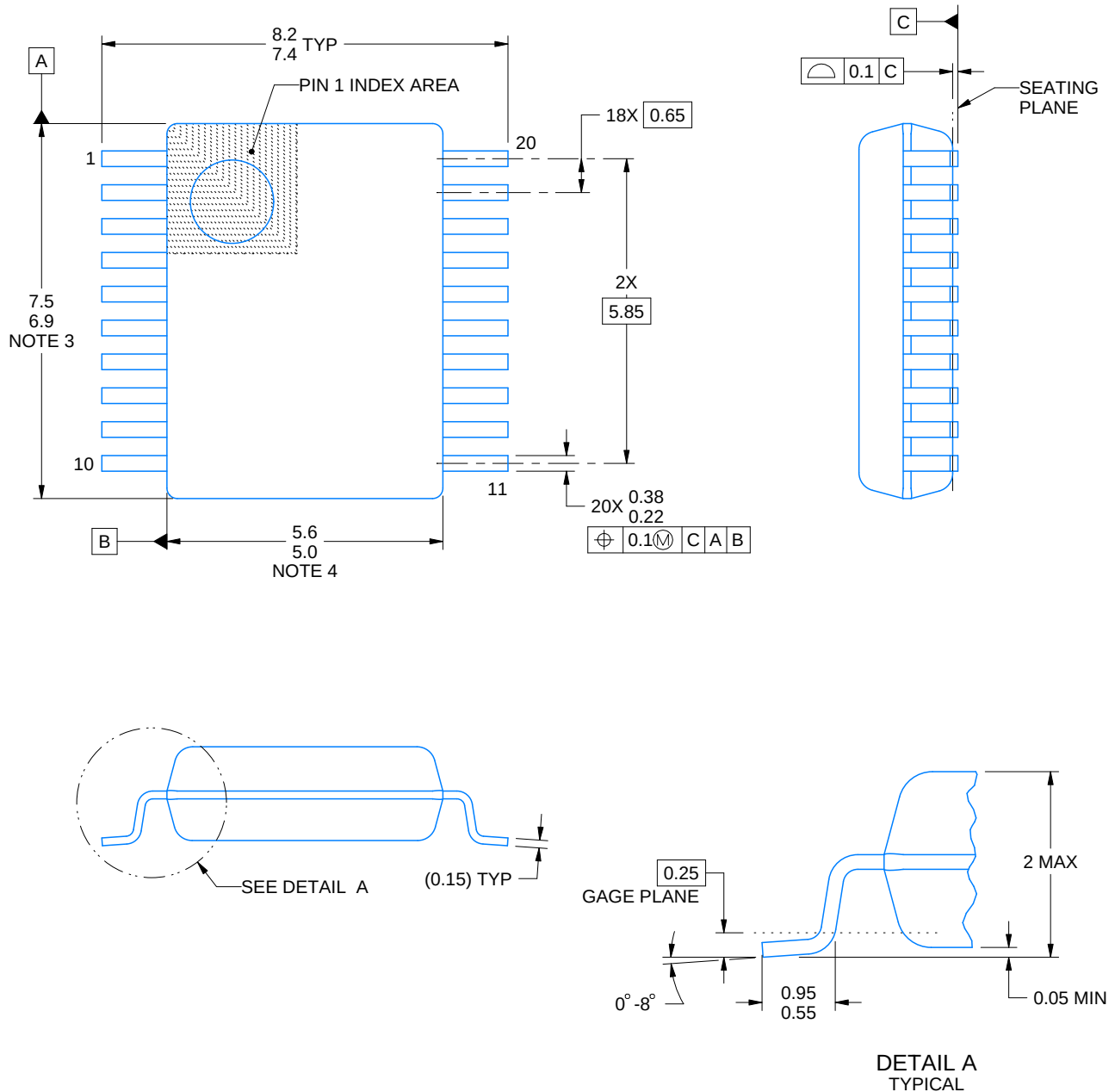
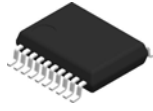


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4214851/B 08/2019

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

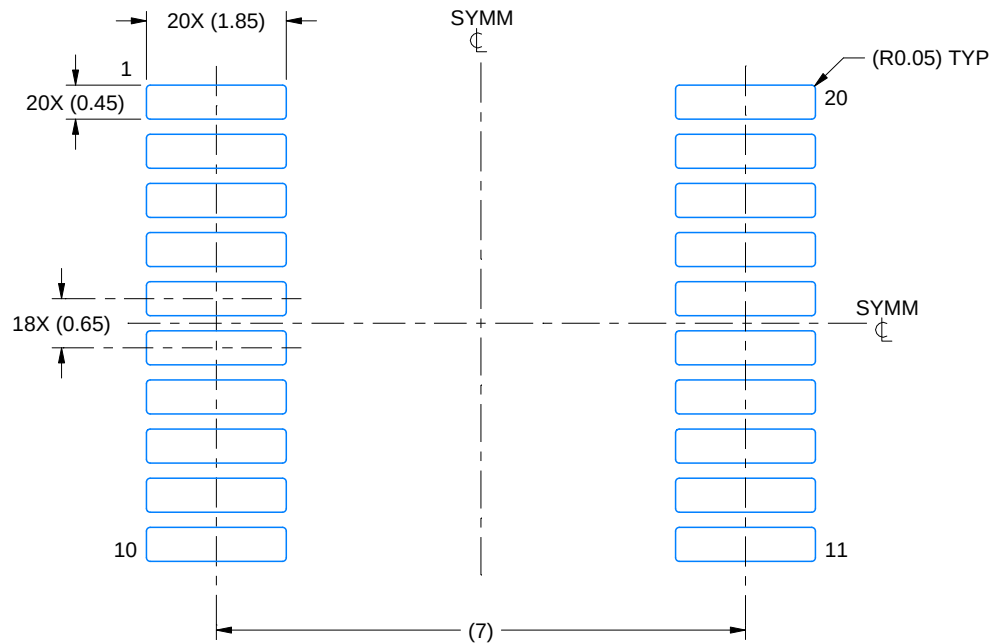


# EXAMPLE BOARD LAYOUT

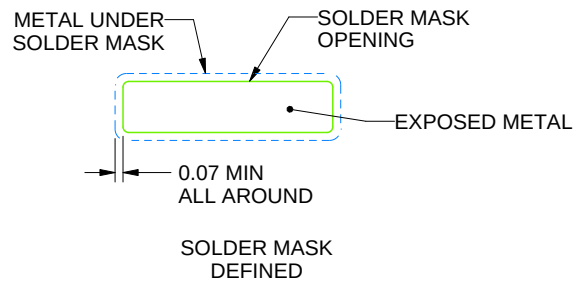
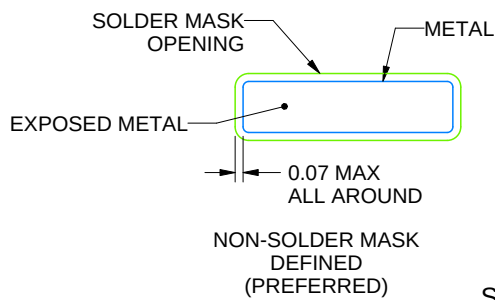
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

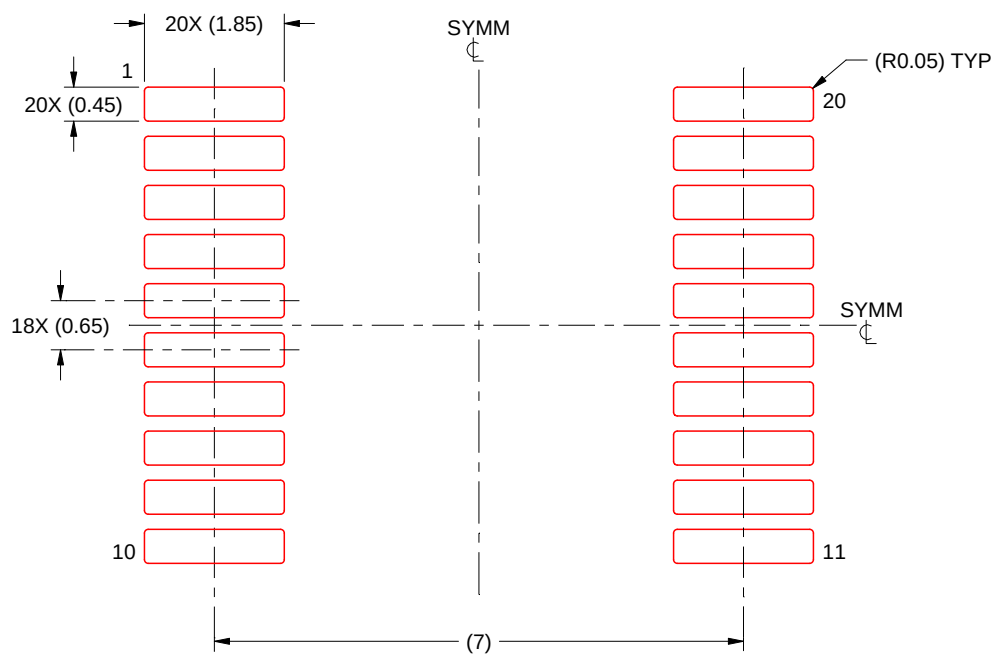
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

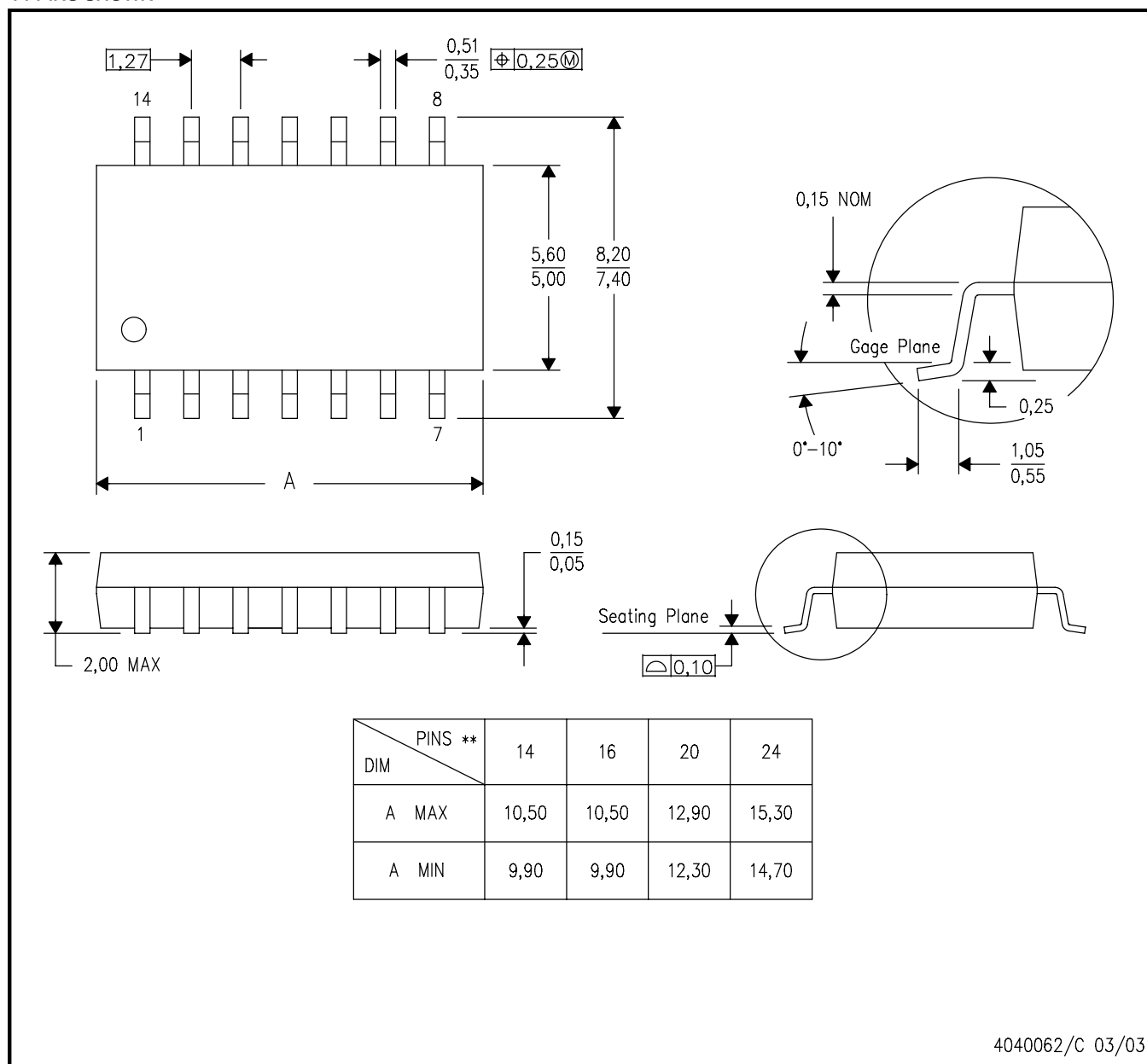
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## GENERIC PACKAGE VIEW

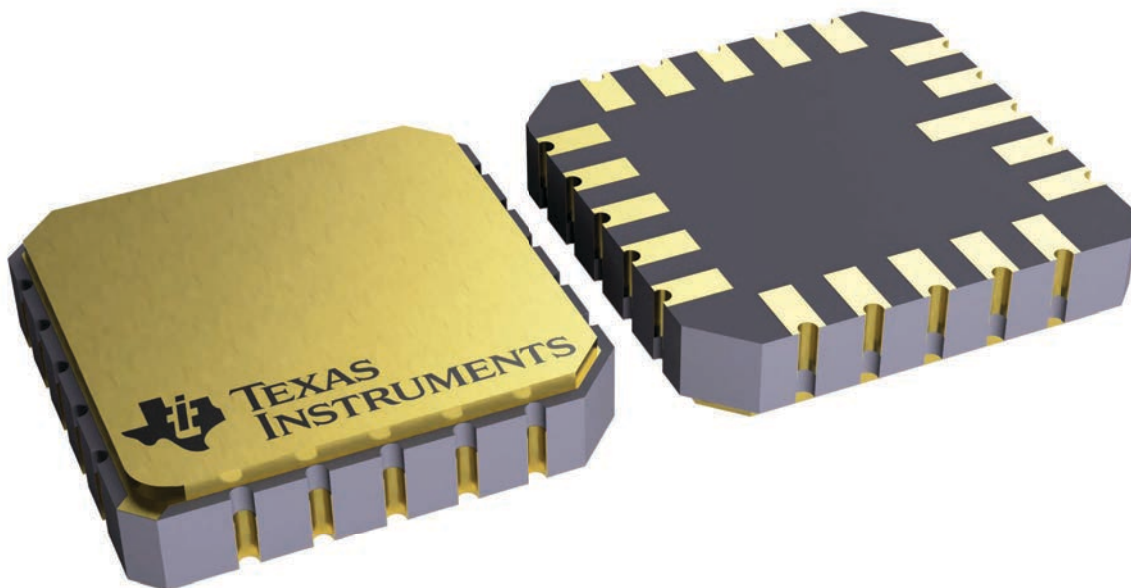
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

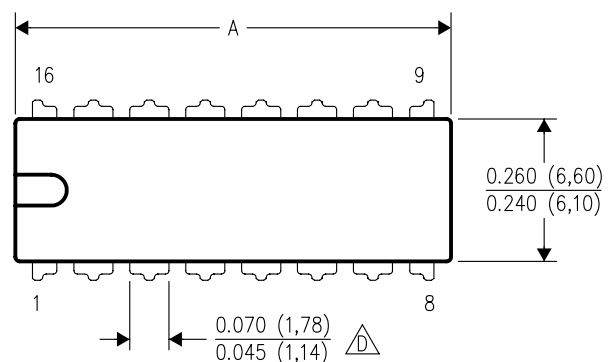


4229370VA\

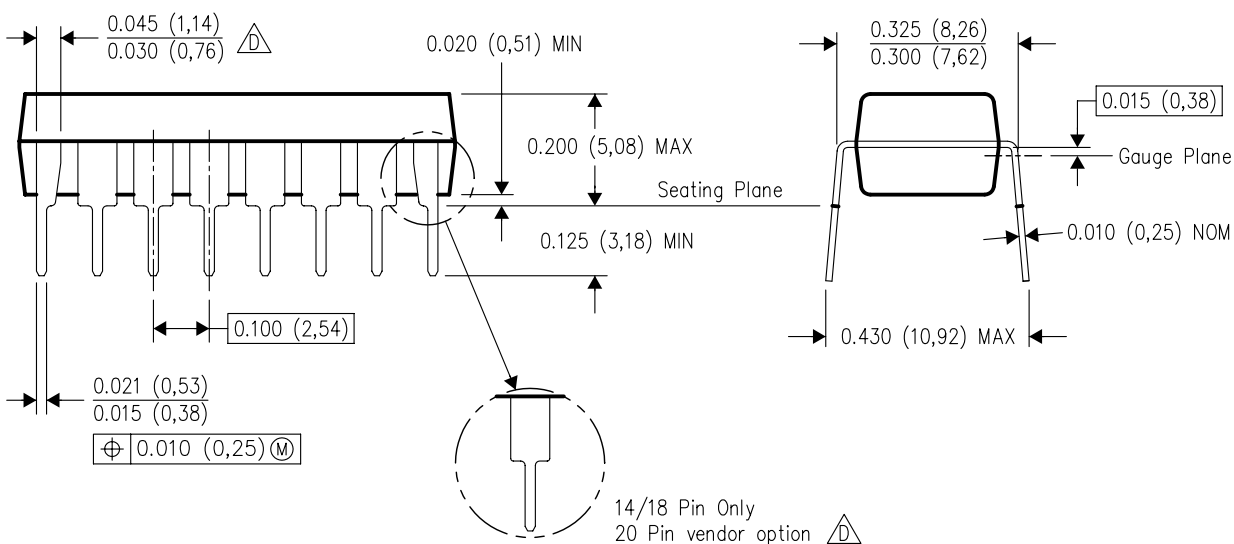
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



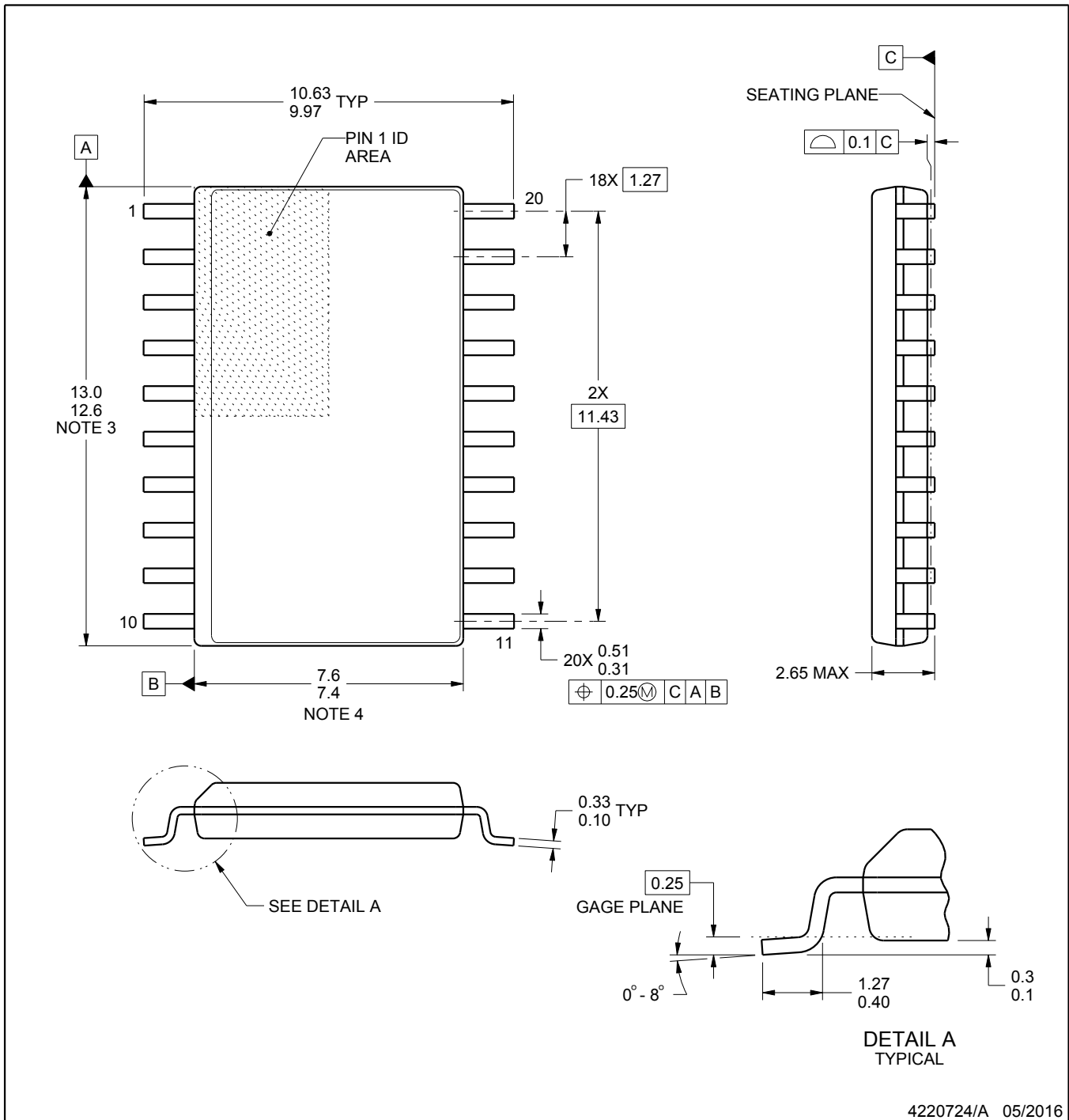
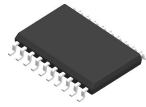
| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



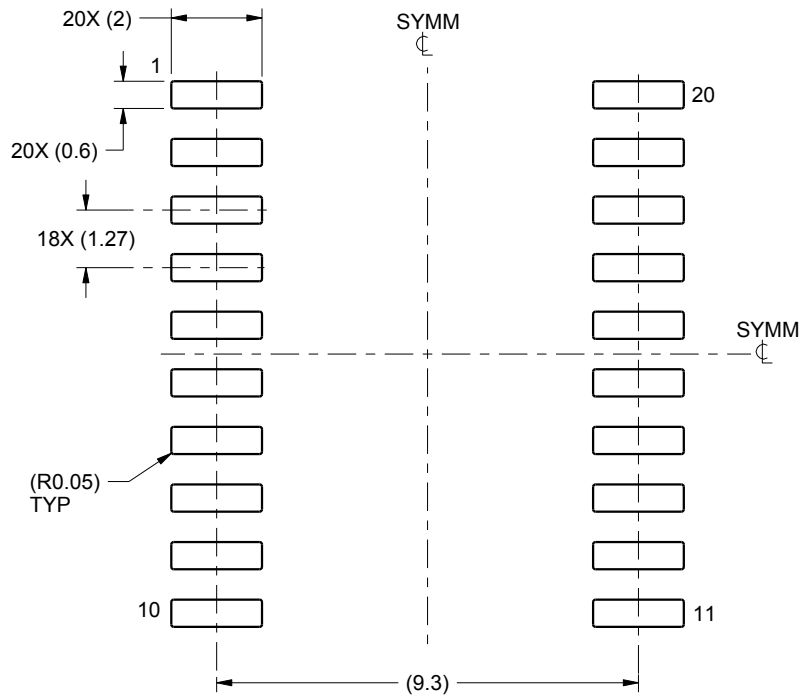
## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

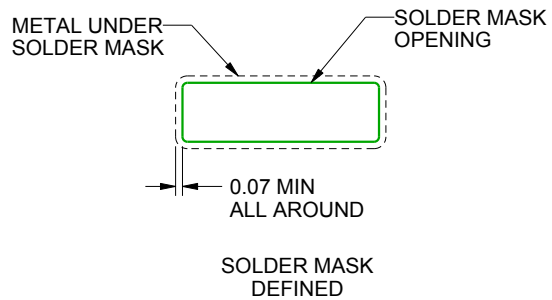
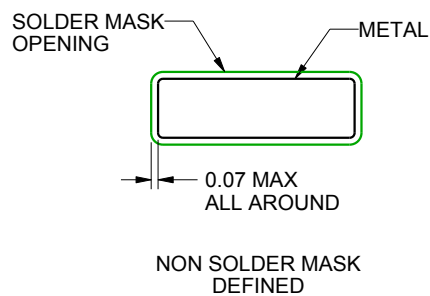
**DW0020A**

**SOIC - 2.65 mm max height**

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



## SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

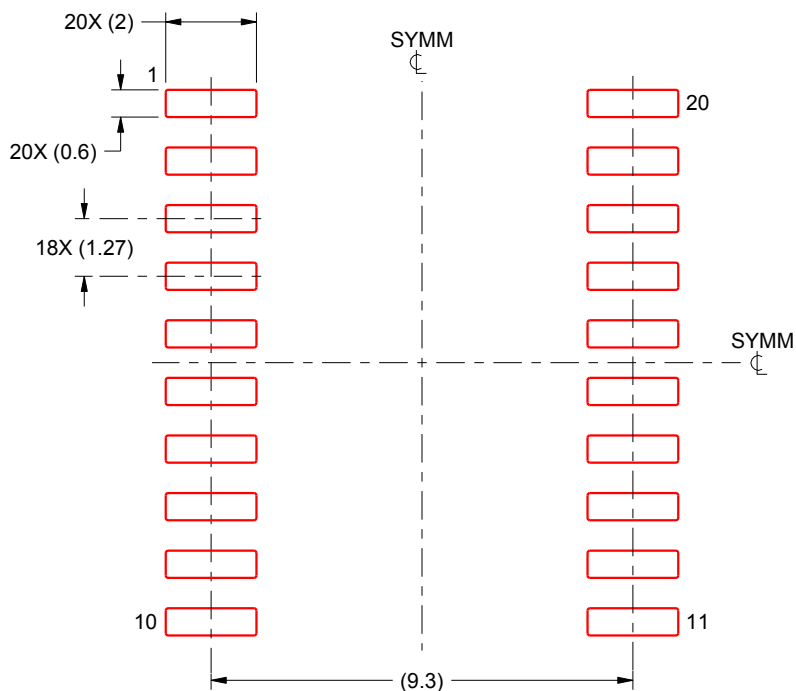
6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

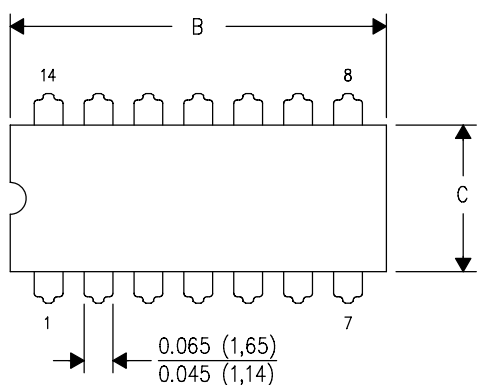
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



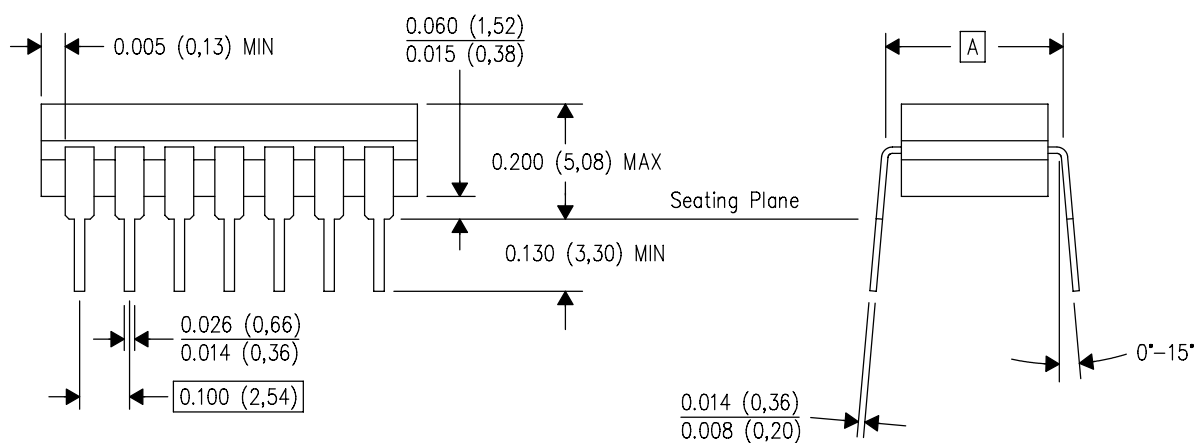
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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