SN54ABT2240A, SN74ABT2240A OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

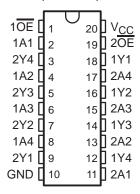
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- Output Ports Have Equivalent 25- Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- **Package Options Include Plastic** Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package

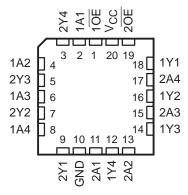
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the 'ABT2241 and 'ABT2244A, these devices provide combinations of inverting and noninverting outputs, symmetrical active-low output-enable (\overline{OE}) inputs, and complementary OE and OE inputs. These devices feature high fan-out and improved fan-in.

SN54ABT2240A . . . J OR W PACKAGE SN74ABT2240A . . . DB, DW, N, OR PW PACKAGE (TOP VIEW)



SN54ABT2240A . . . FK PACKAGE (TOP VIEW)



These devices are organized as two 4-bit line drivers with separate \overline{OE} inputs. When \overline{OE} is low, the devices pass inverted data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include equivalent $25-\Omega$ series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{\sf OE}$ should be tied to ${\sf V}_{\sf CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT2240A is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT2240A is characterized for operation from -40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-IIB is a trademark of Texas Instruments Incorporated

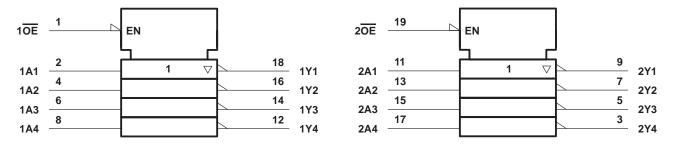


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FUNCTION TABLE (each buffer)

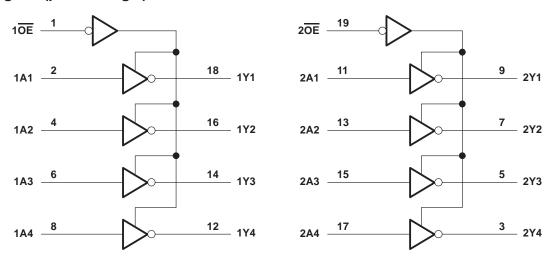
INPU	JTS	OUTPUT
OE	Α	Υ
L	Н	L
L	L	Н
Н	Χ	Z

logic symbol†



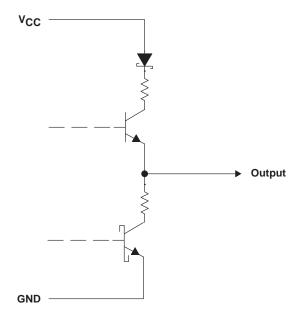
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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schematic of Y outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	or power-off state, V _O DB package DW package	-0.5 V to 7 V -0.5 V to 5.5 V 30 mA -18 mA -50 mA
	. •	
Storage temperature range, T _{stg}	. •	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.



SN54ABT2240A, SN74ABT2240A OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

			SN54ABT	2240A	SN74ABT	2240A	UNIT
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage		0.8		0.8	V	
٧ _I	Input voltage		0	VCC	0	VCC	V
ЮН	High-level output current			-24		-32	mA
loL	Low-level output current			12		12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAA	METER	TEST COL	UDITIONS	Т	A = 25°C	;	SN54AB1	Г2240A	SN74ABT	2240A	UNIT
PARA	MEIER	TEST COI	NDITIONS	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNII
VIK		$V_{CC} = 4.5 \text{ V}, \qquad I_{I} = -18 \text{ mA}$				-1.2		-1.2		-1.2	V
	V _{CC} = 4.5 V, V _{CC} = 5 V,		$I_{OH} = -3 \text{ mA}$	2.5			2.5		2.5		
\/a			$I_{OH} = -3 \text{ mA}$	3			3		3		V
VOH VCC = 4.5		V00 = 45 V	$I_{OH} = -24 \text{ mA}$	2			2				V
		VCC = 4.5 V	$I_{OH} = -32 \text{ mA}$	2*					2		
VOL		$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 12 \text{ mA}$			0.8		0.8		0.8	V
V _{hys}					100						mV
l _l		$V_{CC} = 5.5 \text{ V},$	$V_I = V_{CC}$ or GND			±1		±1		±1	μΑ
lozh		V _{CC} = 5.5 V,	V _O = 2.7 V			10*		10		10	μΑ
lozL		V _{CC} = 5.5 V,	V _O = 0.5 V			-10*		-10		-10	μΑ
l _{off}		$V_{CC} = 0$,	V_I or $V_O \le 4.5 \text{ V}$			±100				±100	μΑ
ICEX		V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high			50		50		50	μА
I _O ‡		$V_{CC} = 5.5 \text{ V},$	V _O = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA
			Outputs high		1	250		250		250	μΑ
Icc		$V_{CC} = 5.5 \text{ V}, I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low		24	30		30		30	mA
		V1 = VCC 01 GIVE	Outputs disabled		0.5	250		250		250	μΑ
	Data	V _{CC} = 5.5 V, One input at 3.4 V,	Outputs enabled			1.5		1.5		1.5	
ΔICC§	inputs	Other inputs at VCC or GND	Outputs disabled			0.05		0.05		0.05	mA
	Control $V_{CC} = 5.5 \text{ V}$, One input inputs of their inputs at V_{CC} of					1.5		1.5		1.5	
Ci	C _i V _I = 2.5 V or 0.5 V		·		4						pF
Co		V _O = 2.5 V or 0.5 V	_		7						pF

^{*} On products compliant to MIL-PRF-38535, this parameter does not apply.



[†] All typical values are at $V_{CC} = 5 \text{ V}$.

[‡] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54ABT2240A, SN74ABT2240A OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

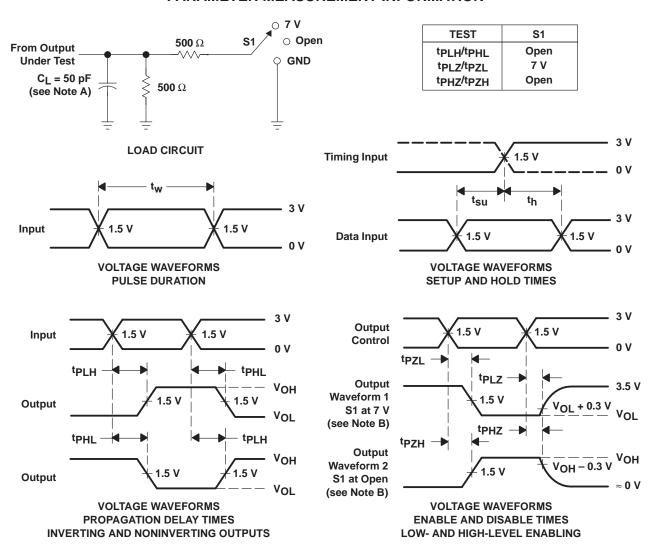
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V ₍	CC = 5 V A = 25°C	', ;	MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	A	V	1	3	4	1	5	ns
^t PHL		'	2.1	4.8	5.8	2.1	6.3	115
^t PZH	ŌĒ	~	1.5	3.7	4.7	1.5	6.1	ns
t _{PZL}		Ť	1.7	6.5	7.6	1.7	8.8	115
^t PHZ	<u> </u>	_	1.8	3.8	6.4	1.5	6.8	ns
^t PLZ	ŌĒ		1	4.7	5.8	1	6.9	115

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V ₍	CC = 5 V A = 25°C	/, ;	MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	A	V	1	3	4.1	1	4.8	ns
t _{PHL}		1	2.1	4.1	5.1	2.1	5.4	115
^t PZH	ŌĒ	V	1.1	3.1	4.7	1.1	5.2	ns
t _{PZL}	OE	ı	1.7	4.5	6.4	1.7	6.8	115
^t PHZ	ŌĒ	V	1.8	3.4	5.7	1.8	6.4	ns
t _{PLZ}	OE	l ' [1.9	3.6	6	1.9	6.2	115

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{Q} = 50 Ω , $t_{f} \leq$ 2.5 ns, $t_{f} \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9469701Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9469701Q2A SNJ54ABT 2240AFK
5962-9469701QRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9469701QR A SNJ54ABT2240AJ
SN74ABT2240ADBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA240A
SN74ABT2240ADBR.B	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA240A
SN74ABT2240ADW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2240A
SN74ABT2240ADW.B	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2240A
SN74ABT2240ADWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2240A
SN74ABT2240ADWR.B	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2240A
SN74ABT2240AN	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ABT2240AN
SN74ABT2240AN.B	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ABT2240AN
SN74ABT2240ANSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2240A
SN74ABT2240ANSR.B	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2240A
SN74ABT2240APW	Active	Production	TSSOP (PW) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA240A
SN74ABT2240APW.B	Active	Production	TSSOP (PW) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA240A
SN74ABT2240APWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA240A
SN74ABT2240APWR.B	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA240A
SNJ54ABT2240AFK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9469701Q2A SNJ54ABT 2240AFK
SNJ54ABT2240AJ	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9469701QR A SNJ54ABT2240AJ

⁽¹⁾ Status: For more details on status, see our product life cycle.

PACKAGE OPTION ADDENDUM

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(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54ABT2240A, SN74ABT2240A:

Catalog: SN74ABT2240A

Military: SN54ABT2240A

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT2240ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABT2240ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ABT2240ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ABT2240APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT2240ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74ABT2240ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ABT2240ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74ABT2240APWR	TSSOP	PW	20	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9469701Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74ABT2240ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ABT2240ADW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ABT2240AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ABT2240AN.B	N	PDIP	20	20	506	13.97	11230	4.32
SN74ABT2240APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74ABT2240APW.B	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54ABT2240AFK	FK	LCCC	20	55	506.98	12.06	2030	NA





- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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