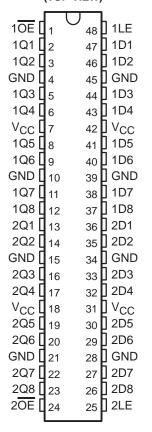
SCBS160C - DECEMBER 1992 - REVISED MAY 1997

- **Members of the Texas Instruments** Widebus™ Family
- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per **JEDEC Standard JESD-17**
- Typical V_{OLP} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$
- **High-Impedance State During Power Up** and Power Down
- Distributed V_{CC} and GND Pin Configuration **Minimizes High-Speed Switching Noise**
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I_{OH}, 64-mA I_{OI})
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package **Using 25-mil Center-to-Center Spacings**

description

The 'ABT16373A are 16-bit transparent D-type latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

SN54ABT16373A . . . WD PACKAGE SN74ABT16373A . . . DGG OR DL PACKAGE (TOP VIEW)



These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16373A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16373A is characterized for operation from -40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

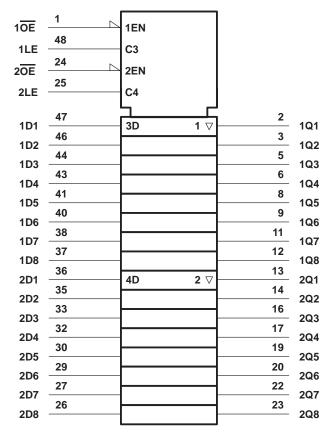
Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.



FUNCTION TABLE (each 8-bit section)

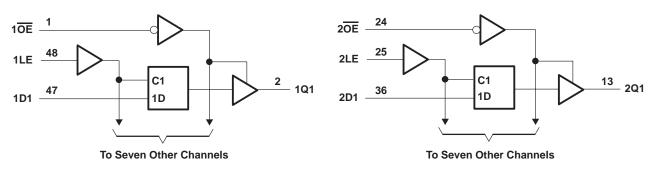
	INPUTS		OUTPUT
OE	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	Q ₀
Н	X	Χ	Z

logic symbol†



 $[\]ensuremath{^{\dagger}}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V _O	–0.5 V to 5.5 V
Current into any output in the low state, I _O : SN54ABT16373A	96 mA
SN74ABT16373A	128 mA
Input clamp current, I _{IK} (V _I < 0)	–18 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Package thermal impedance, θ _{JA} (see Note 2): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

			SN54ABT	16373A	SN74ABT	16373A	LINUT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2		2		V
V _{IL}	Low-level input voltage			0.8		0.8	V
٧ _I	Input voltage		0	Vcc	0	Vcc	V
ЮН	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
Δt/ΔVCC	Power-up ramp rate		200		200		μs/V
TA	Operating free-air temperature	·	-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CON	UDITIONS	Т	A = 25°C	;	SN54ABT1	16373A	SN74ABT1	6373A	UNIT
	ARAMETER	l lesi coi	ADITIONS	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$			-1.2		-1.2		-1.2	V
		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.5			2.5		2.5		
\/~		$V_{CC} = 5 V$,	$I_{OH} = -3 \text{ mA}$	3			3		3		V
VOH		V _{CC} = 4.5 V	$I_{OH} = -24 \text{ mA}$	2			2				V
		VCC = 4.5 V	$I_{OH} = -32 \text{ mA}$	2*					2		
\/a:		V _{CC} = 4.5 V				0.55		0.55			V
VOL		VCC = 4.5 V	I _{OL} = 64 mA			0.55*				0.55	V
V _{hys}					100						mV
ΙĮ		$V_{CC} = 0$ to 5.5 V $V_I = V_{CC}$ or GNI			±1		±1		±1	μА	
lozpu	_J ‡	$V_{CC} = 0 \text{ to } 2.1 \text{ V}$ $V_{O} = 0.5 \text{ V to } 2.7 \text{ V}$			±50		±50		±50	μА	
IOZPD	,‡	$V_{CC} = 2.1 \text{ V to } 0.5 \text{ V}$			±50		±50		±50	μΑ	
lozh		V _{CC} = 2.1 V to 5 V _O = 2.7 V, OE 2				10		10		10	μΑ
lozL		$V_{CC} = 2.1 \text{ V to } 5$ $V_{O} = 0.5 \text{ V}, \overline{\text{OE}} \ge 0.5 \text{ V}$				-10		-10		-10	μА
loff		$V_{CC} = 0$, V_I or V	O ≤ 4.5 V			±100				±100	μΑ
ICEX	Outputs high	$V_{CC} = 5.5 \text{ V},$	V _O = 5.5 V			50		50		50	μΑ
IO§		$V_{CC} = 5.5 \text{ V},$	V _O = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA
	Outputs high		•			2		2		2	
ICC	Outputs low	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND				85		85		85	mA
	Outputs disabled	1 100 31 011			2		2		2		
ΔICC¶		V _{CC} = 5.5 V, On Other inputs at V			1.5		1.5		1.5	mA	
Ci		V _I = 2.5 V or 0.5	V		3.5						pF
Co		V _O = 2.5 V or 0.5	5 V		9.5						pF

^{*} On products compliant to MIL-PRF-38535, this parameter does not apply.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V _{CC} = T _A = 2	$V_{CC} = 5 \text{ V},$ $T_{A} = 25^{\circ}C^{\#}$		16373A	SN74ABT	UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE high	3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE↓	1.5		2.4		1.5		ns
th	Hold time, data after LE↓	1		2.2		1		ns

[#]These values apply only to the SN74ABT16373A.



[†] All typical values are at $V_{CC} = 5 \text{ V}$.

[‡] This parameter is characterized, but not production tested.

[§] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

 $[\]P$ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

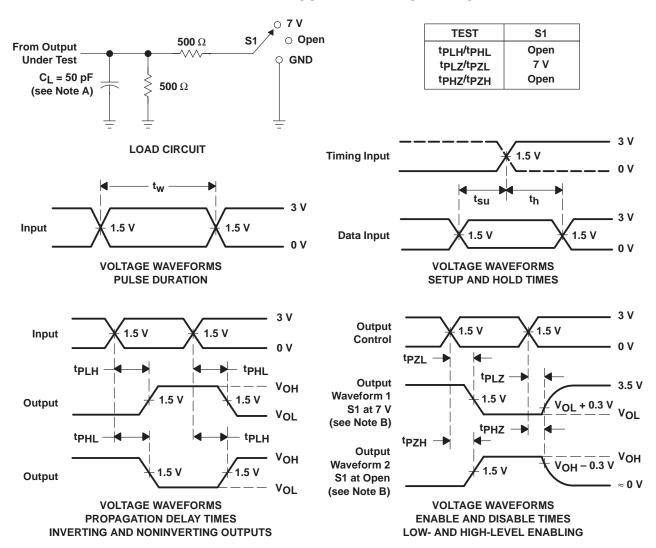
				SN54	ABT163	73A		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V ₍	CC = 5 V A = 25°C	<u>'</u> ,	MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	D	Q	1.4	3.7	5.3	1.4	6.5	ns
t _{PHL}	Б	Q	2	4	5.4	2	6.5	115
^t PLH	LE	Q	1.7	4.1	5.7	1.7	7	ns
t _{PHL}	LL	Q	2.3	4.3	5.6	2.3	6.3	115
^t PZH	ŌĒ	Q	1.1	3.4	5	1.1	6.4	no
t _{PZL}	OE	Q	1.5	3.5	4.9	1.5	5.8	ns
^t PHZ	ŌĒ	Q	2.4	5.1	7.1	2.4	8.3	ne
tPLZ	OE	l q	1.6	4.4	6.3	1.6	8	ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

				SN74	ABT163	73A		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V ₍	CC = 5 V 4 = 25°C	', ;	MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	D	Q	1.4	3.7	5.3	1.4	6.3	ns
t _{PHL}	U	Q	2	4	5.4	2	6.2	115
t _{PLH}	LE	Q	1.7	4.1	5.7	1.7	6.7	ns
^t PHL	LL	Q	2.3	4.3	5.6	2.3	6.1	115
^t PZH	ŌĒ	Q	1.1	3.4	5	1.1	6.1	ns
t _{PZL}	OE	Q	1.5	3.5	4.9	1.5	5.6	115
^t PHZ	ŌĒ	Q	2.4	5.1	7.1	2.4	8.1	nc
t _{PLZ}	OE	Q	1.6	4.4	5.8	1.6	6.5	ns

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{Q} = 50 Ω , t_{f} \leq 2.5 ns, t_{f} \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
5962-9320001QXA	Active	Production	CFP (WD) 48	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9320001QX A SNJ54ABT16373A WD
74ABT16373ADGGRE4	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
74ABT16373ADGGRG4	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
SN74ABT16373ADGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
SN74ABT16373ADGGR.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
SN74ABT16373ADL	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
SN74ABT16373ADL.B	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
SN74ABT16373ADLG4	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
SN74ABT16373ADLG4.B	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
SN74ABT16373ADLR	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
SN74ABT16373ADLR.B	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
SN74ABT16373ADLRG4	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
SNJ54ABT16373AWD	Active	Production	CFP (WD) 48	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9320001QX A SNJ54ABT16373A WD

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OPTION ADDENDUM

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(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54ABT16373A, SN74ABT16373A:

Catalog: SN74ABT16373A

Enhanced Product: SN74ABT16373A-EP, SN74ABT16373A-EP

Military: SN54ABT16373A

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16373ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ABT16373ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

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*All dimensions are nominal

Device	Package Type	e Type Package Drawing		SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16373ADGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74ABT16373ADLR	SSOP	DL	48	1000	356.0	356.0	53.0

PACKAGE MATERIALS INFORMATION

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TUBE



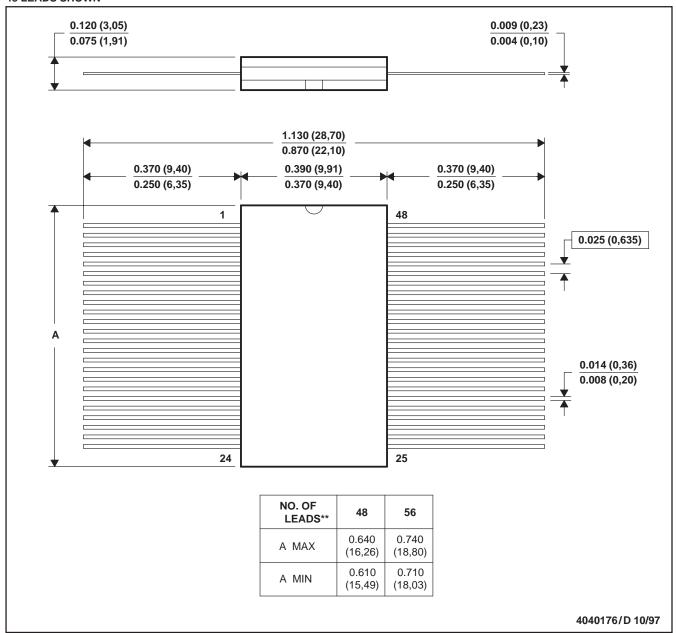
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ABT16373ADL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74ABT16373ADL.B	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74ABT16373ADLG4	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74ABT16373ADLG4.B	DL	SSOP	48	25	473.7	14.24	5110	7.87

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only
- E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA

GDFP1-F56 and JEDEC MO-146AB

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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