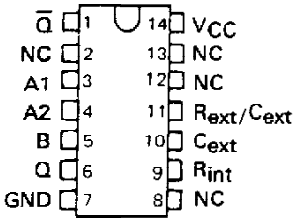
- Programmable Output Pulse Width
  With R_{int} . . . 35 ns Typ
  With R_{ext}/C_{ext} . . . 40 ns to 28 Seconds
- Internal Compensation for Virtual Temperature Independence
- Jitter-Free Operation up to 90% Duty Cycle
- Inhibit Capability

SN54121 . . . J OR W PACKAGE
SN74121 . . . N PACKAGE
(TOP VIEW)



NC - No internal connection.

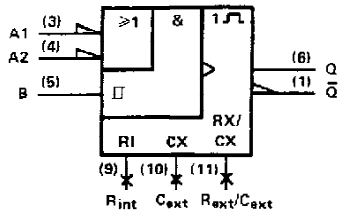
FUNCTION TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L†	H†
X	X	L	L†	H†
H	H	X	L†	H†
H	↓	H	⎍	⎍
↓	H	H	⎍	⎍
↓	↓	H	⎍	⎍
L	X	↑	⎍	⎍
X	L	↑	⎍	⎍

For explanation of function table symbols, see page

† These lines of the function table assume that the indicated steady-state conditions at the A and B inputs have been setup long enough to complete any pulse started before the setup.

logic symbol‡



‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

These multivibrators feature dual negative-transition-triggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

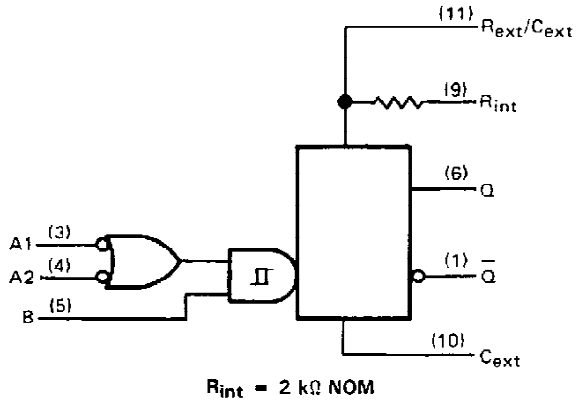
Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R_{int} connected to V_{CC}, C_{ext} and R_{ext}/C_{ext} open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 30 kΩ for the SN54121 and 2 kΩ to 40 kΩ for the SN74121). Throughout these ranges, pulse width is defined by the relationship $t_{w(out)} = C_{ext}R_T\ln 2 \approx 0.7\ C_{ext}R_T$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μF and timing resistance as low as 1.4 kΩ may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

logic diagram (positive logic)



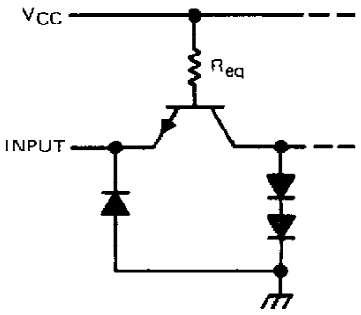
R_{int} = 2 kΩ NOM

Pin numbers shown on logic notation are for J or N packages.

NOTES: 1. An external capacitor may be connected between C_{ext} (positive) and R_{ext}/C_{ext}.
2. To use the internal timing resistor, connect R_{int} to V_{CC}. For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.

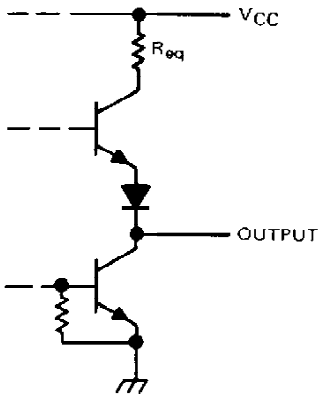
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



INPUT	R_{eq} NOM
A1	4 kΩ
A2	4 kΩ
B	2 kΩ

TYPICAL OF BOTH OUTPUTS



R_{eq} = 130 Ω NOM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 3) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54121 . . . . . −55°C to 125°C
SN74121 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 3: Voltage values are with respect to network ground terminal.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54 Family	4.5	5	5.5	V
			74 Family	4.75	5	5.25	
I_{OH}	High-level output current					−0.4	mA
I_{OL}	Low-level output current					16	mA
dv/dt	Rate of rise or fall of input pulse	Schmitt input, B		1			V/s
		Logic inputs, A1, A2		1			V/μs
$t_{w(in)}$	Input pulse width			50			ns
R_{ext}	External timing capacitance		54 Family	1.4		30	kΩ
			74 Family	1.4		40	
C_{ext}	External timing capacitance			0		1000	μF
	Duty cycle	R_T = 2 kΩ				67	%
		R_T = MAX R_{ext}				90	
T_A	Operating free-air temperature		54 Family	−55		125	°C
			74 Family	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage at A input	V_{CC} = MIN		2			V
V_{IL}	Low-level input voltage at A input	V_{CC} = MIN				0.8	V
V_{T+}	Positive-going threshold voltage at B input	V_{CC} = MIN			1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	V_{CC} = MIN		0.8	1.35		V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output voltage	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = MAX		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V	A1 or A2			40	μA
			B			80	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	A1 or A2			−1.6	mA
			B			−3.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX	54 Family	−20		−55	mA
			74 Family	−18		−55	
I_{CC}	Supply current	V_{CC} = MAX	Quiescent		13	25	mA
			Triggered		23	40	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level Q output from either A input	C_L = 15 pF, R_L = 400 Ω, See Note 4	C_{ext} = 80 pF, R_{int} to V_{CC}		45	70	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from B input				35	55	ns
t_{PHL}	Propagation delay time, high-to-low level $\overline{Q}$ output from either A input				50	80	ns
t_{PHL}	Propagation delay time, high-to-low level $\overline{Q}$ output from B input				40	65	ns
$t_{w(out)}$	Pulse width obtained using internal timing resistor		C_{ext} = 80 pF, R_{int} to V_{CC}	70	110	150	ns
$t_{w(out)}$	Pulse width obtained with zero timing capacitance		C_{ext} = 0, R_{int} to V_{CC}		30	50	ns
$t_{w(out)}$	Pulse width obtained using external timing resistor		C_{ext} = 100 pF, R_T = 10 kΩ	600	700	800	ns
			C_{ext} = 1 μF, R_T = 10 kΩ	6	7	8	ms

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF UNITS
for
OUTPUT PULSE WIDTH

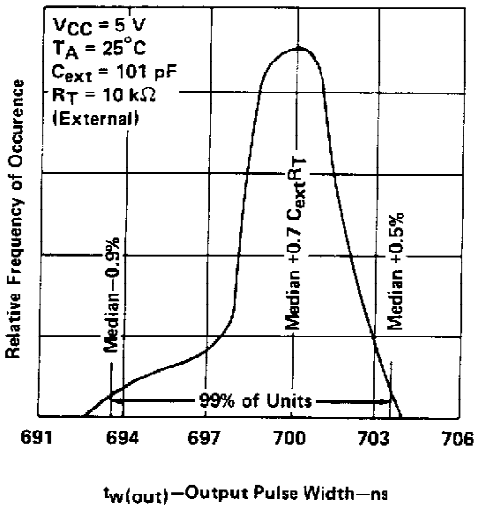


FIGURE 1

VARIATION IN INTERNAL TIMING RESISTOR VALUE
vs
FREE-AIR TEMPERATURE

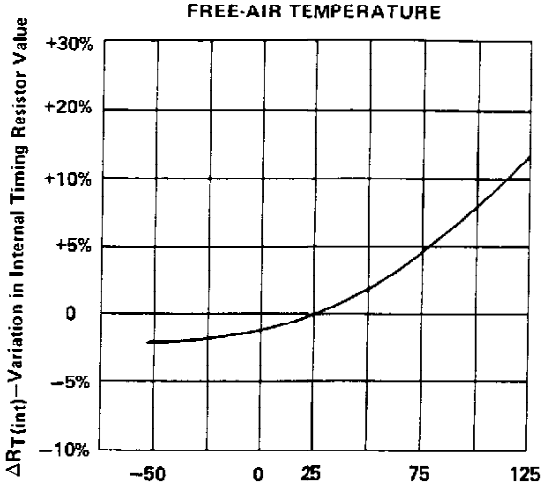


FIGURE 2

VARIATION IN OUTPUT PULSE WIDTH
vs
SUPPLY VOLTAGE

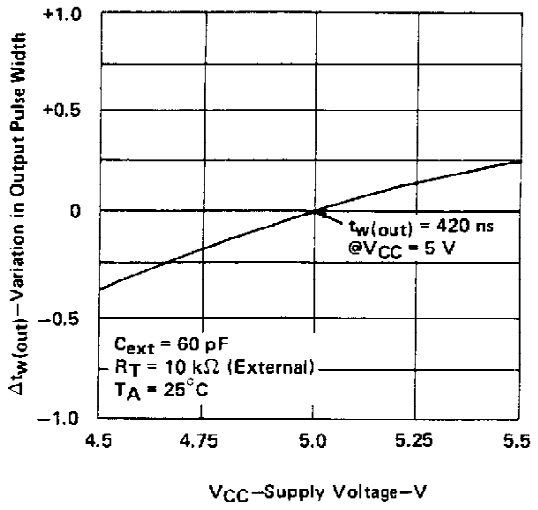


FIGURE 3

SCHMITT TRIGGER THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

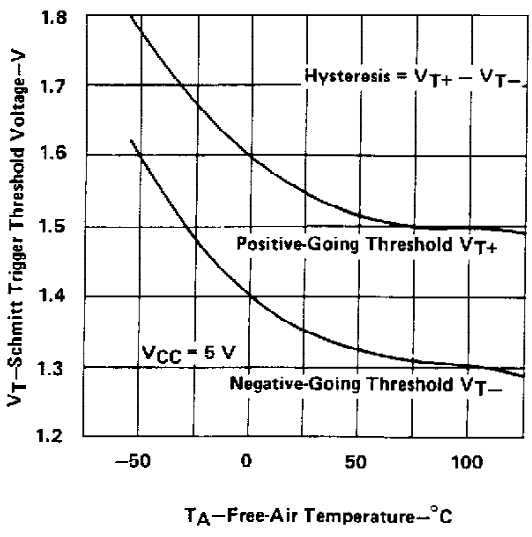


FIGURE 4

†Data for temperatures below 0°C and above 70°C are applicable for SN54121.

TYPICAL CHARACTERISTICS† (continued)

VARIATION IN OUTPUT PULSE WIDTH
vs
FREE-AIR TEMPERATURE

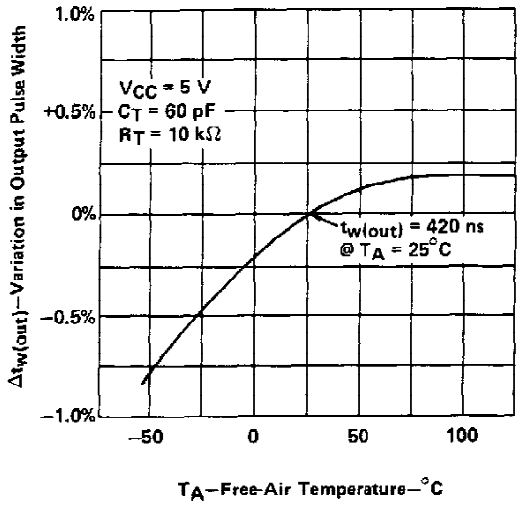


FIGURE 5

OUTPUT PULSE WIDTH
vs
TIMING RESISTOR VALUE

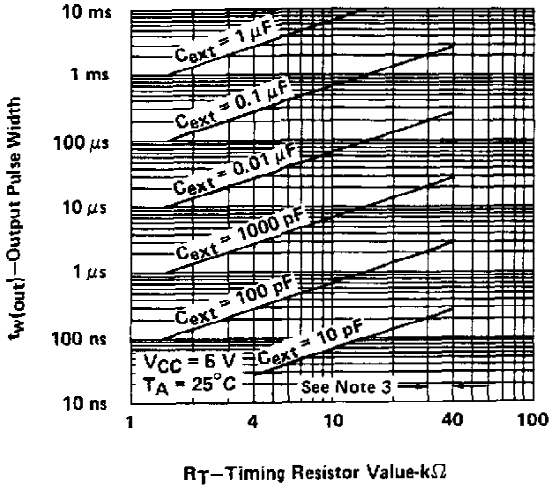


FIGURE 6

OUTPUT PULSE WIDTH
vs
EXTERNAL CAPACITANCE

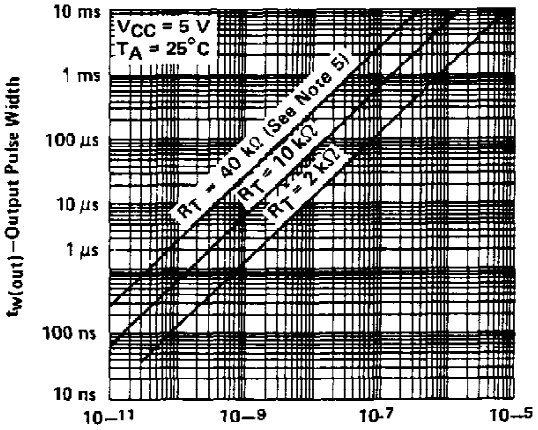


FIGURE 7

NOTE 5: These values of resistance exceed the maximum recommended use over the full temperature range of the SN54121.
†Data for temperatures below 0°C and above 70°C are applicable for SN54121.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-9755301QCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
5962-9755301QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
5962-9755301QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SN54121J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SN54121J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SN74121D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74121D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74121DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74121DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74121N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74121N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74121N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74121N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74121NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74121NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SNJ54121J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54121J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54121W	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54121W	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54121WA	ACTIVE	CFP	WA	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54121WA	ACTIVE	CFP	WA	14	1	TBD	Call TI	Level-NC-NC-NC

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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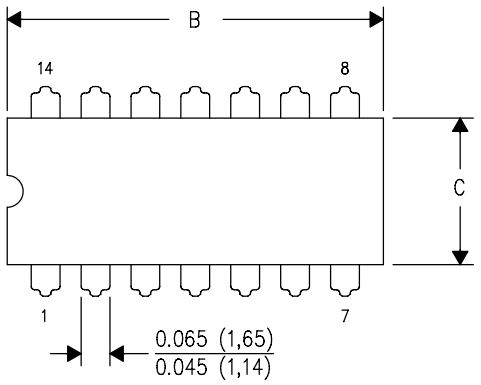
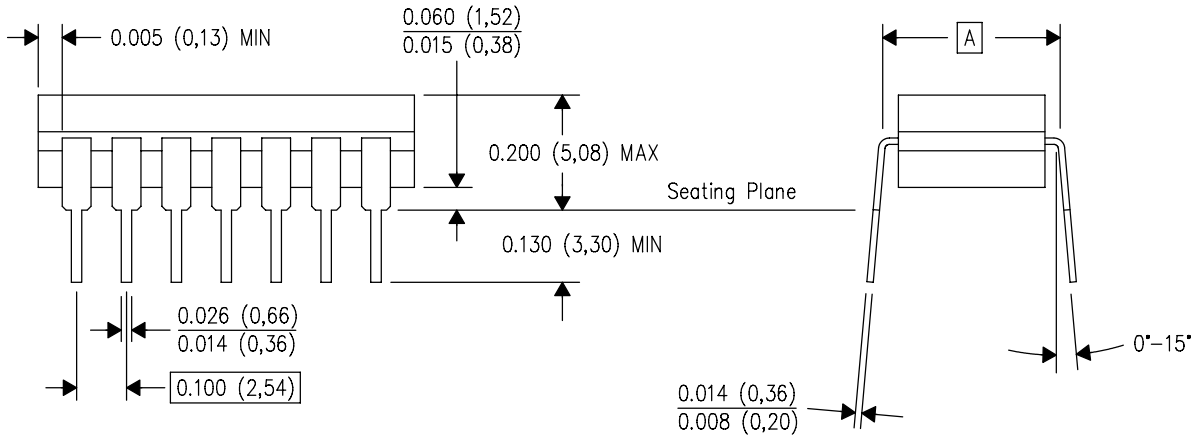
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



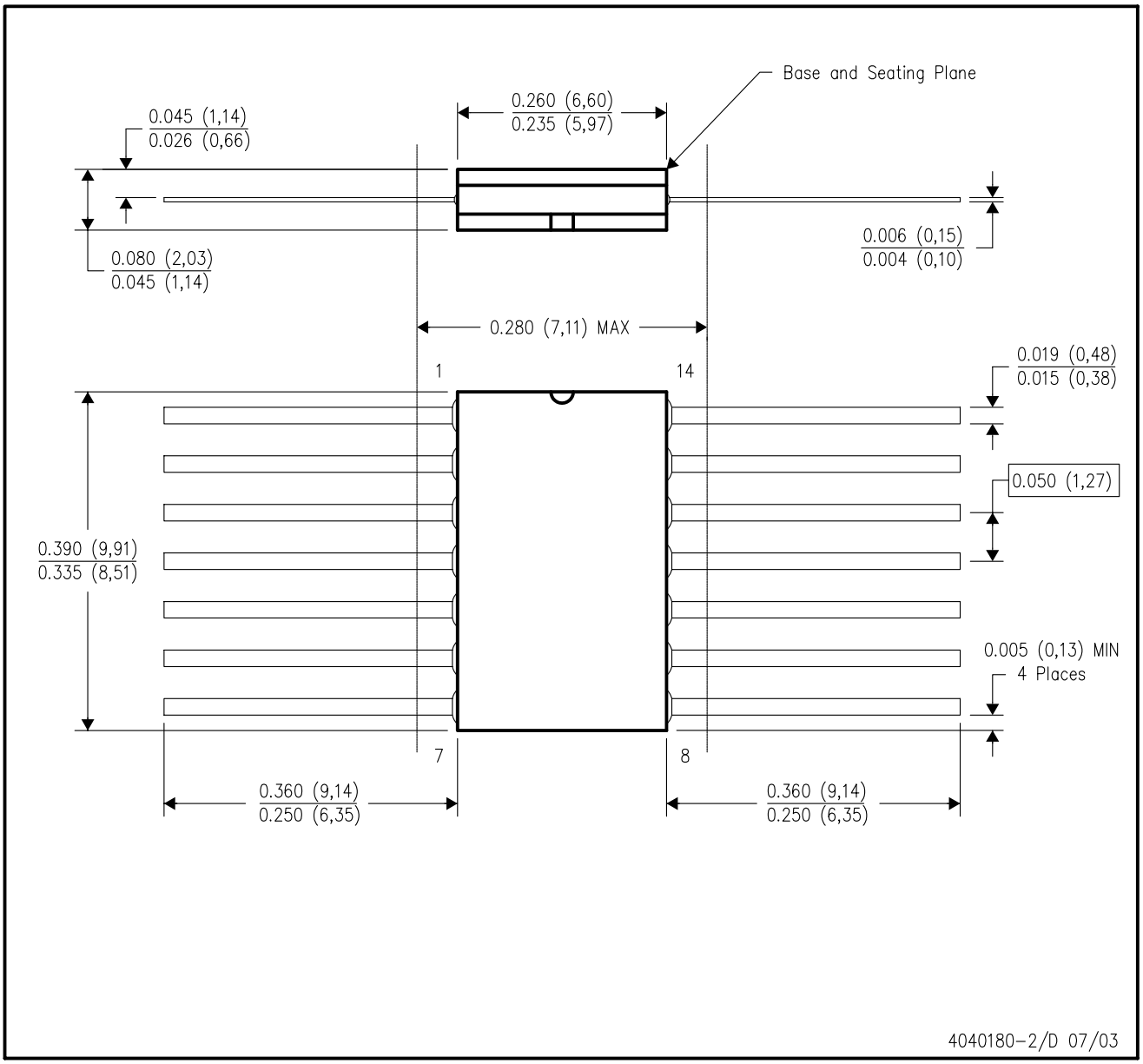
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

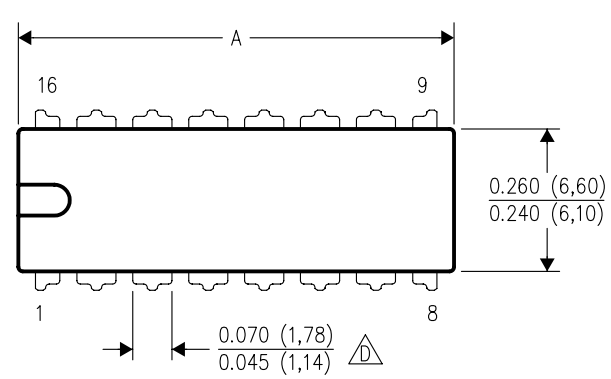


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

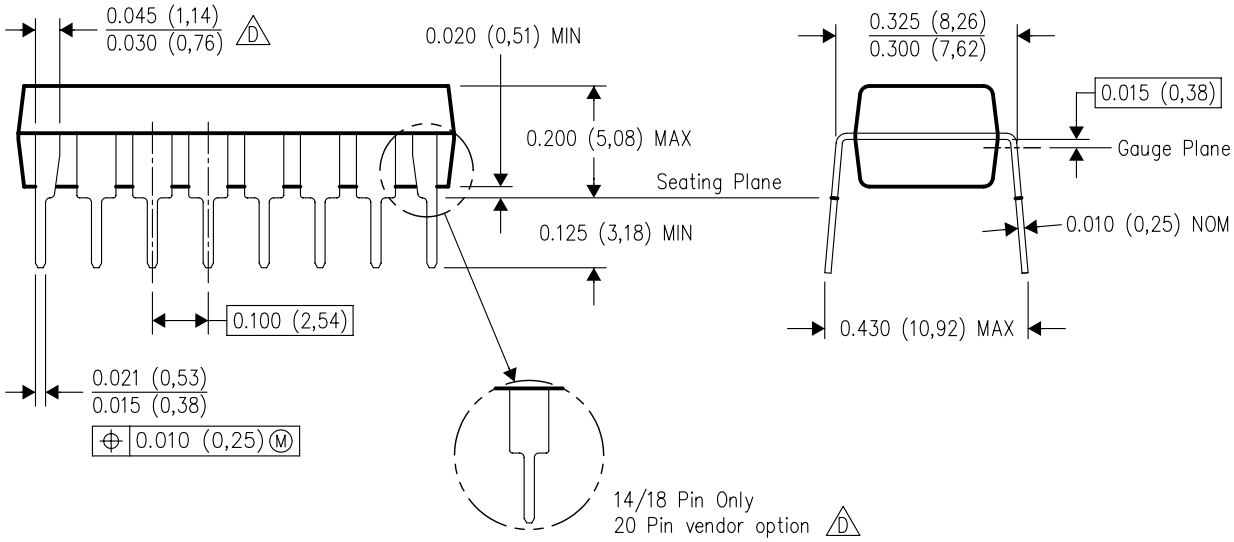
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



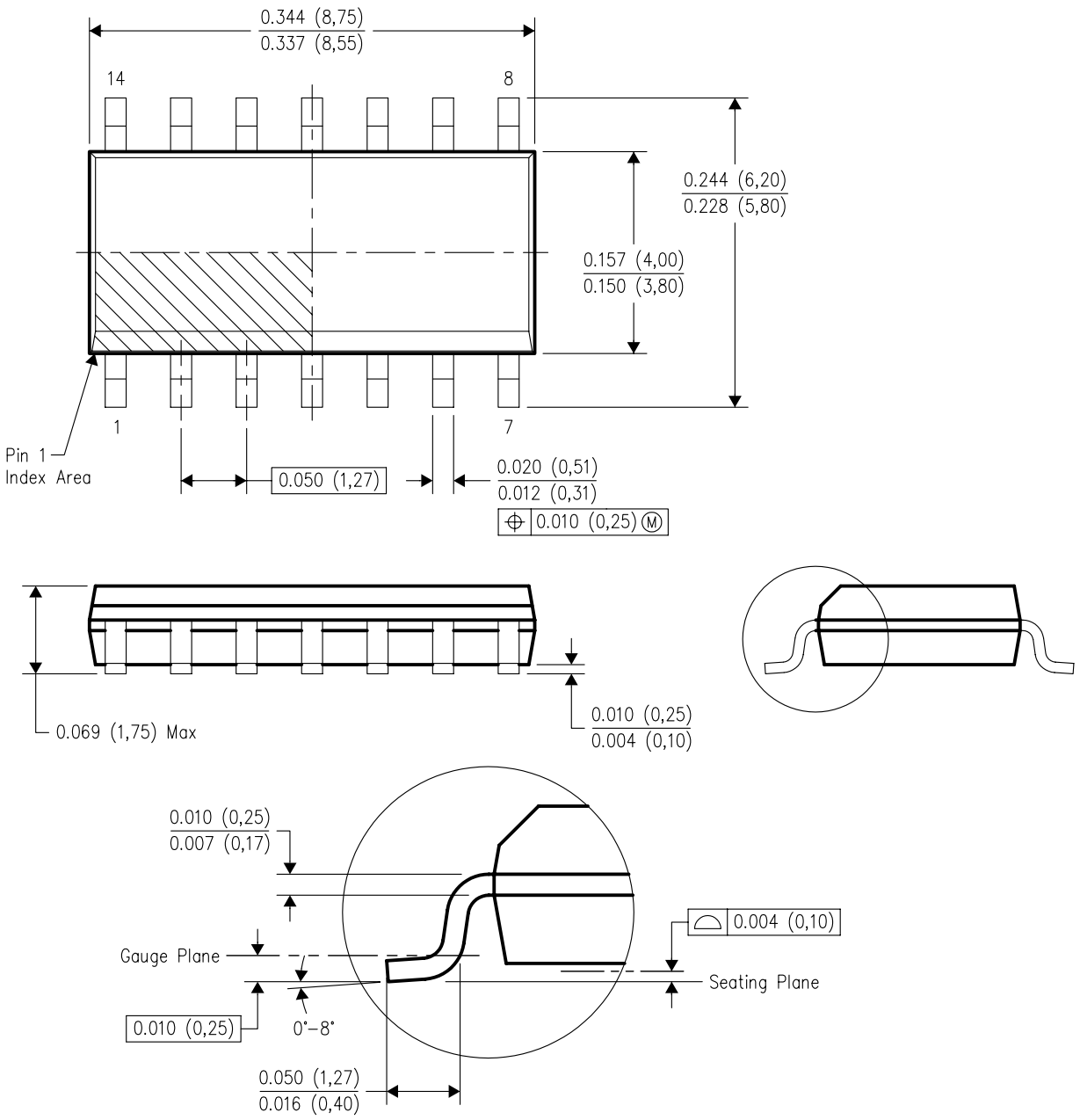
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE

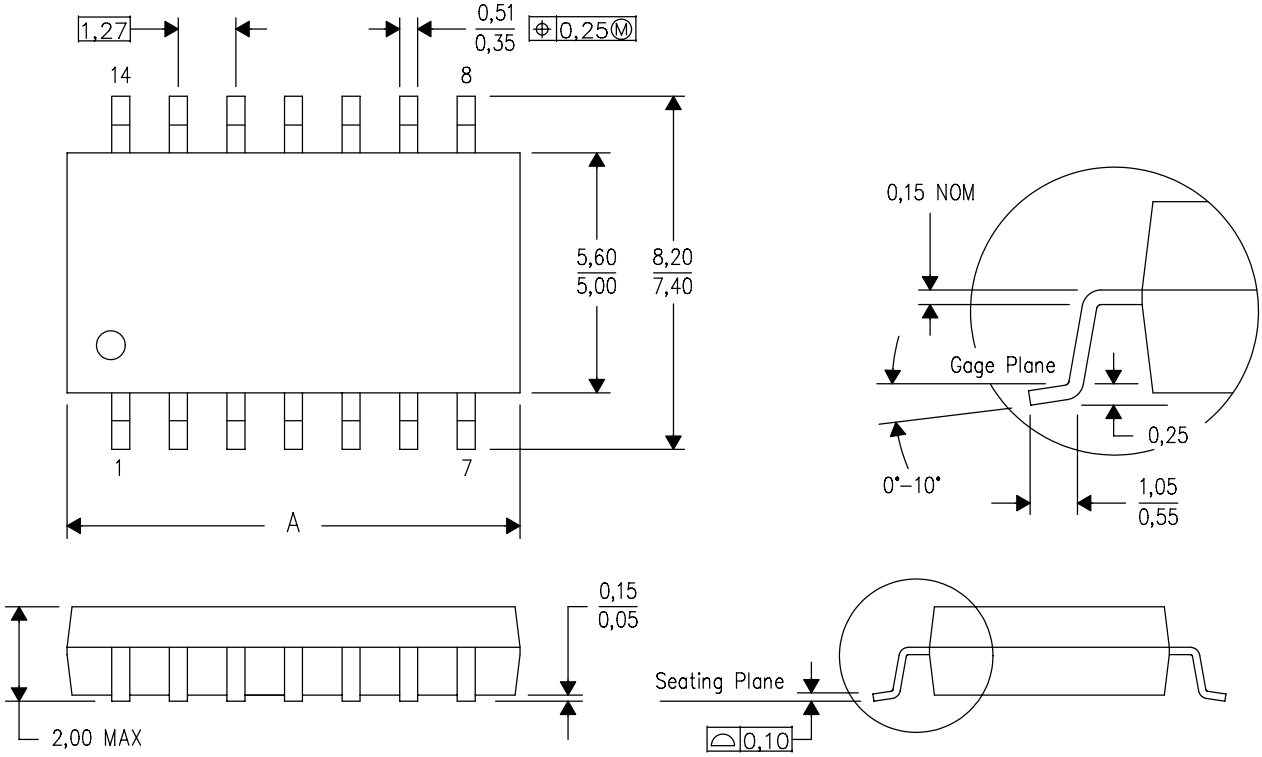


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9755301QCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9755301QC A SNJ54121J
5962-9755301QDA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9755301QD A SNJ54121W
SN54121J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54121J
SN54121J.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54121J
SN74121D	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74121
SN74121D.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74121
SN74121DE4	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74121
SN74121N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74121N
SN74121N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74121N
SNJ54121J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9755301QC A SNJ54121J
SNJ54121J.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9755301QC A SNJ54121J
SNJ54121W	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9755301QD A SNJ54121W
SNJ54121W.A	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9755301QD A SNJ54121W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

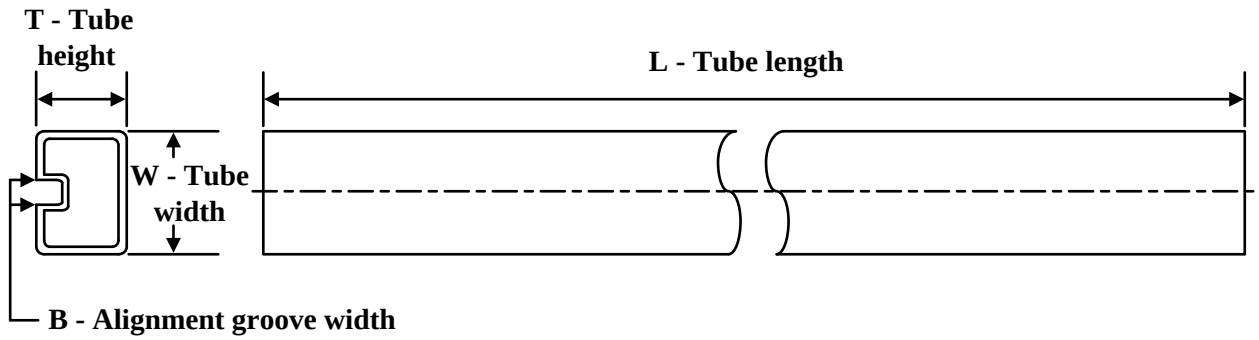
OTHER QUALIFIED VERSIONS OF SN54121, SN74121 :

- Catalog : SN74121
- Military : SN54121

NOTE: Qualified Version Definitions:

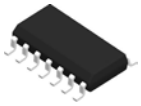
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9755301QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74121D	D	SOIC	14	50	506.6	8	3940	4.32
SN74121D.A	D	SOIC	14	50	506.6	8	3940	4.32
SN74121DE4	D	SOIC	14	50	506.6	8	3940	4.32
SN74121N	N	PDIP	14	25	506	13.97	11230	4.32
SN74121N	N	PDIP	14	25	506	13.97	11230	4.32
SN74121N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74121N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54121W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54121W.A	W	CFP	14	25	506.98	26.16	6220	NA

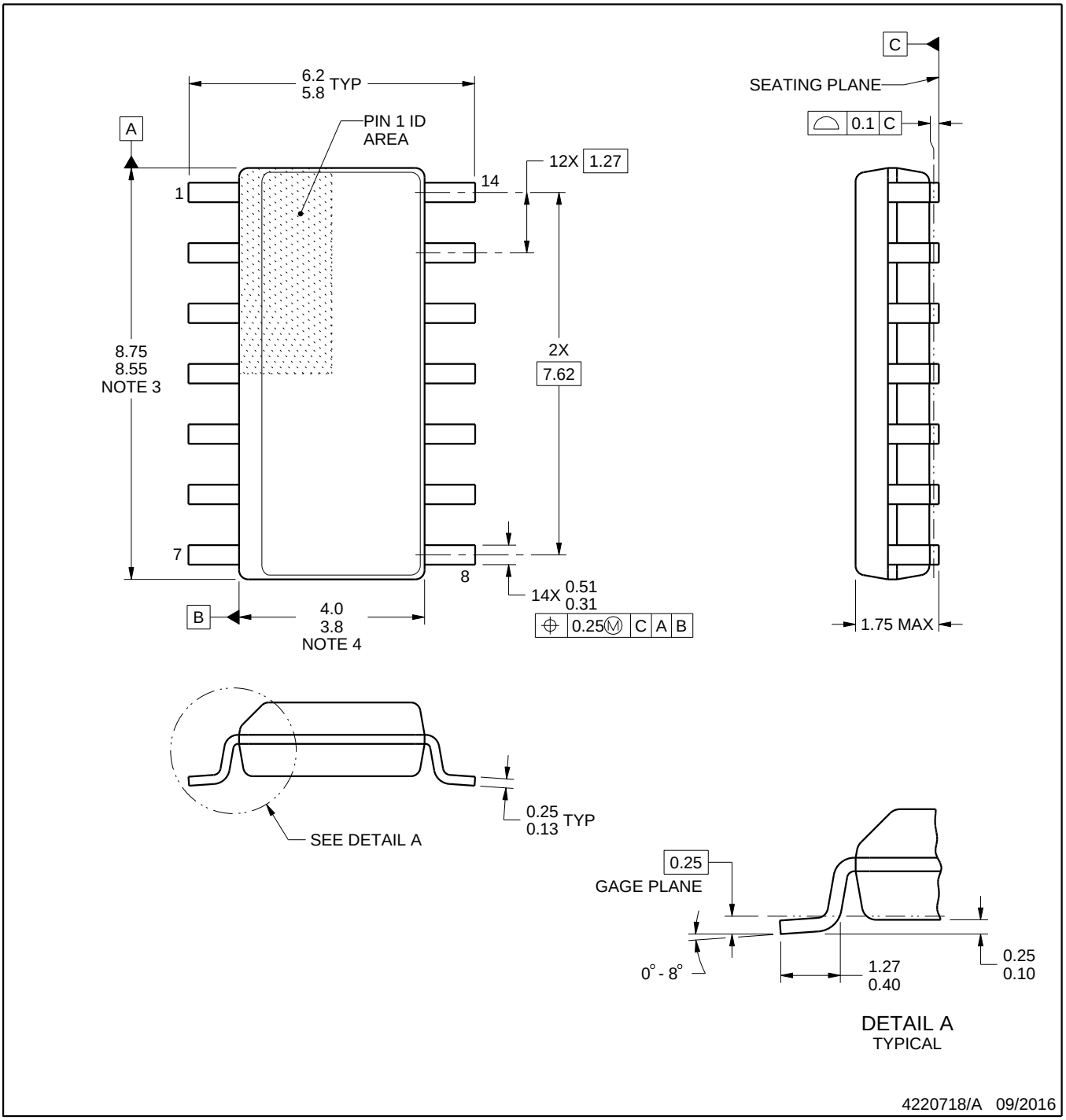


PACKAGE OUTLINE

D0014A

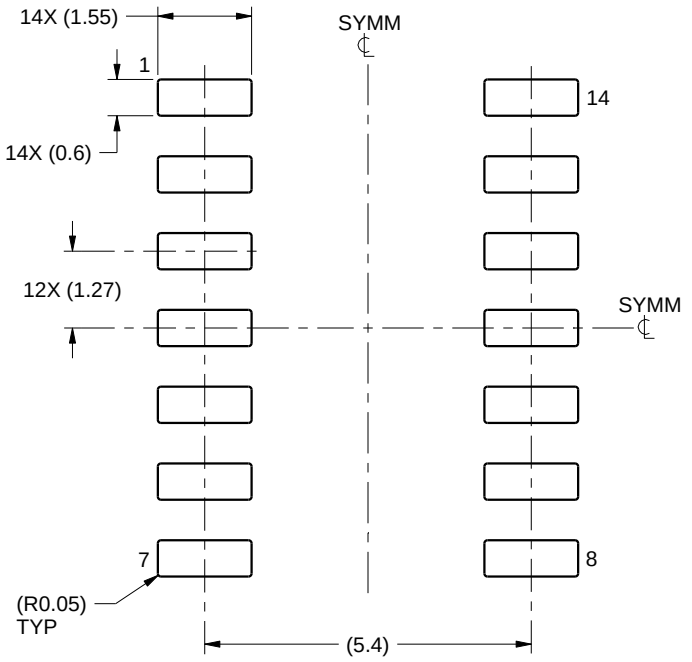
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

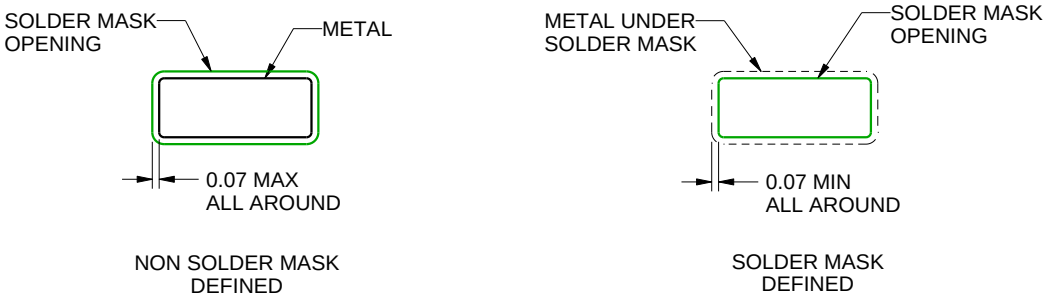


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

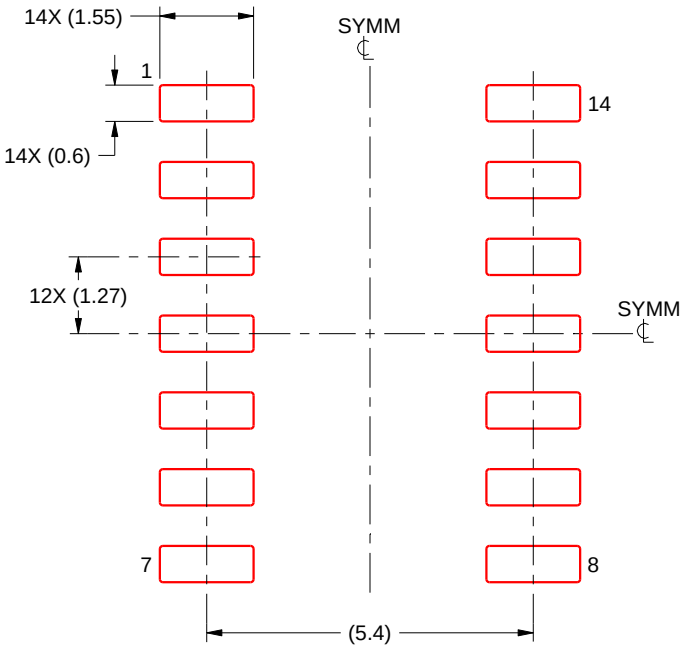
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



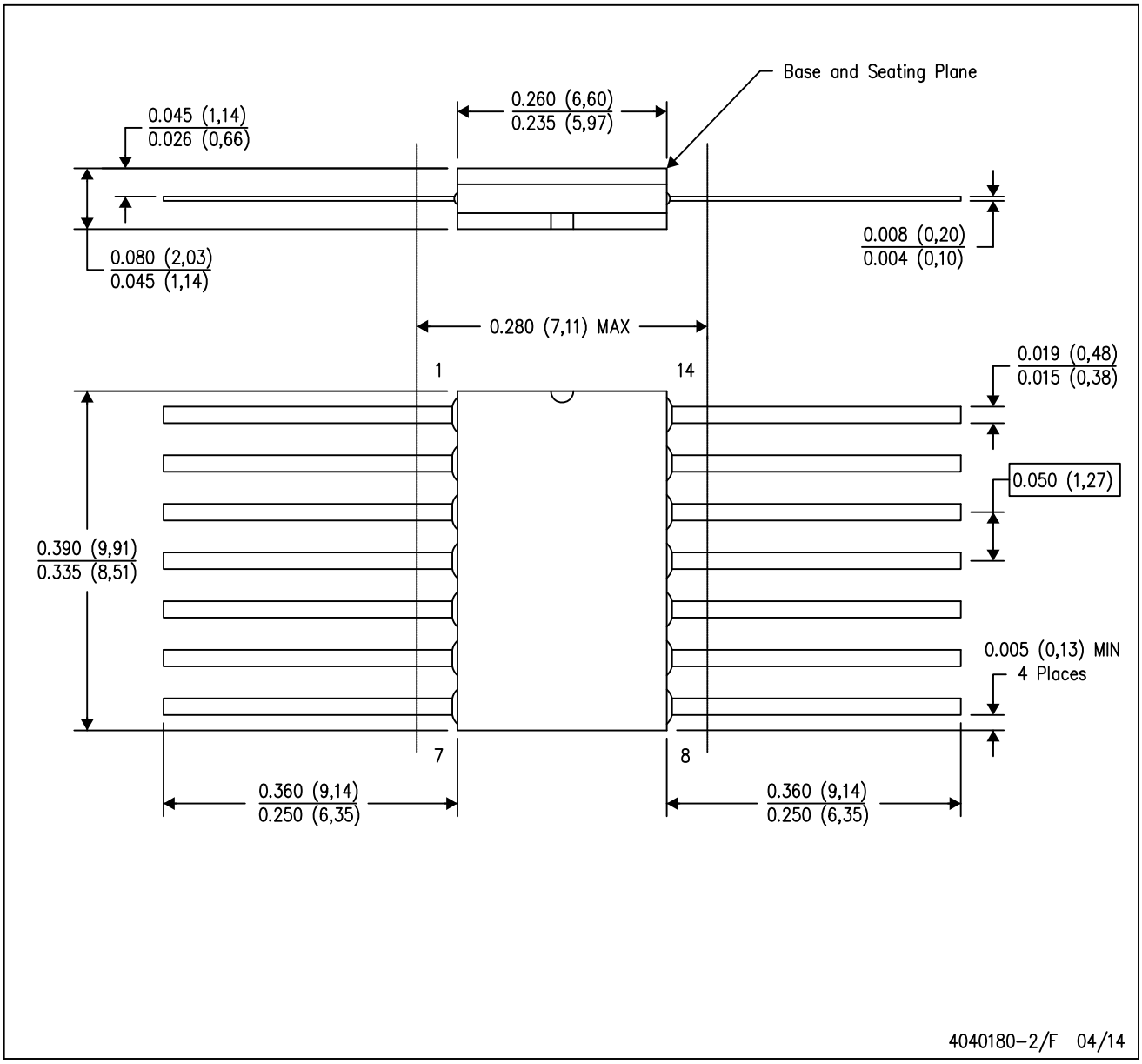
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

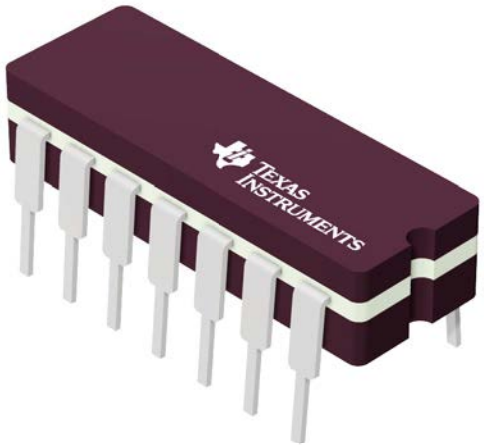


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

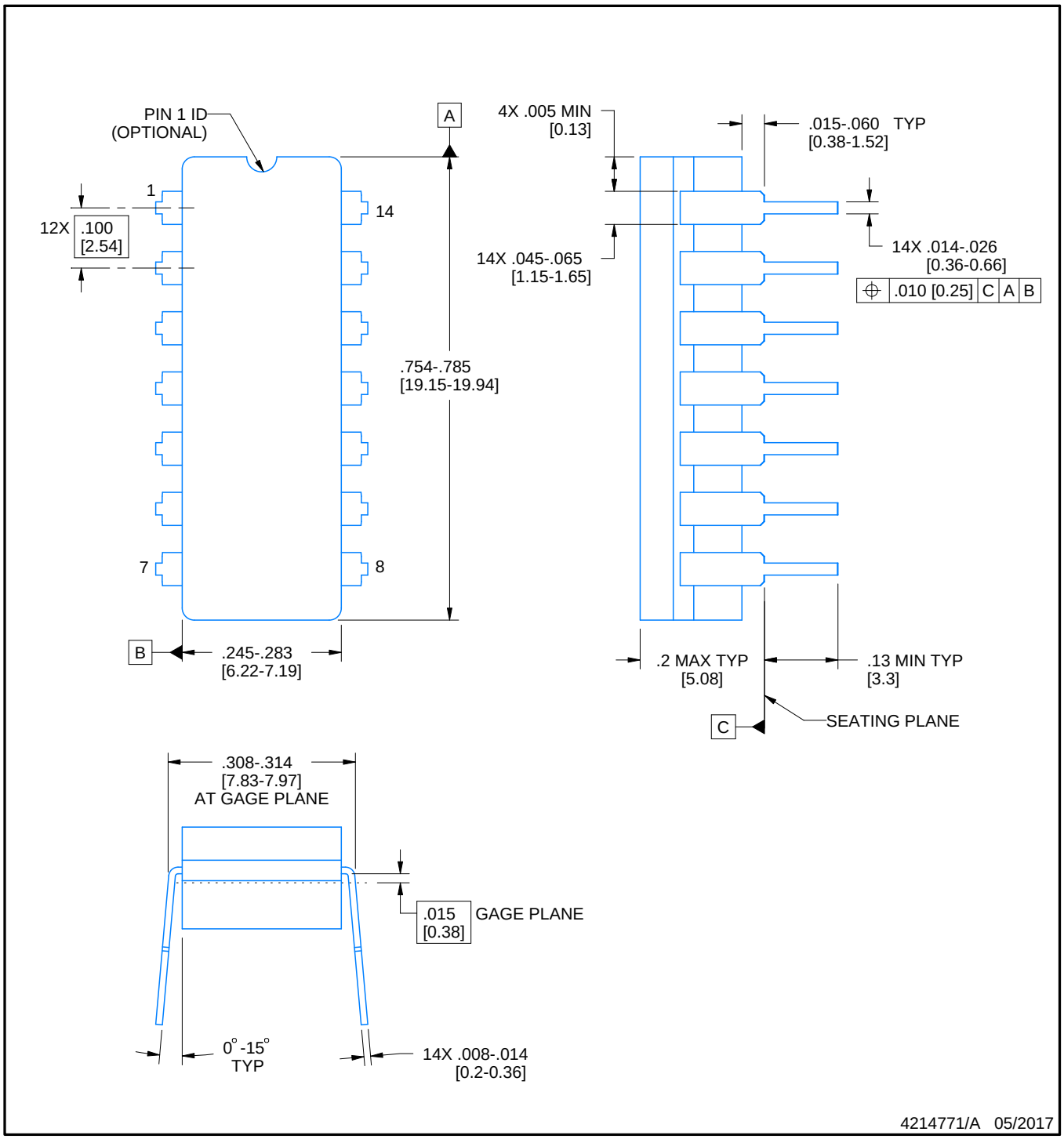
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

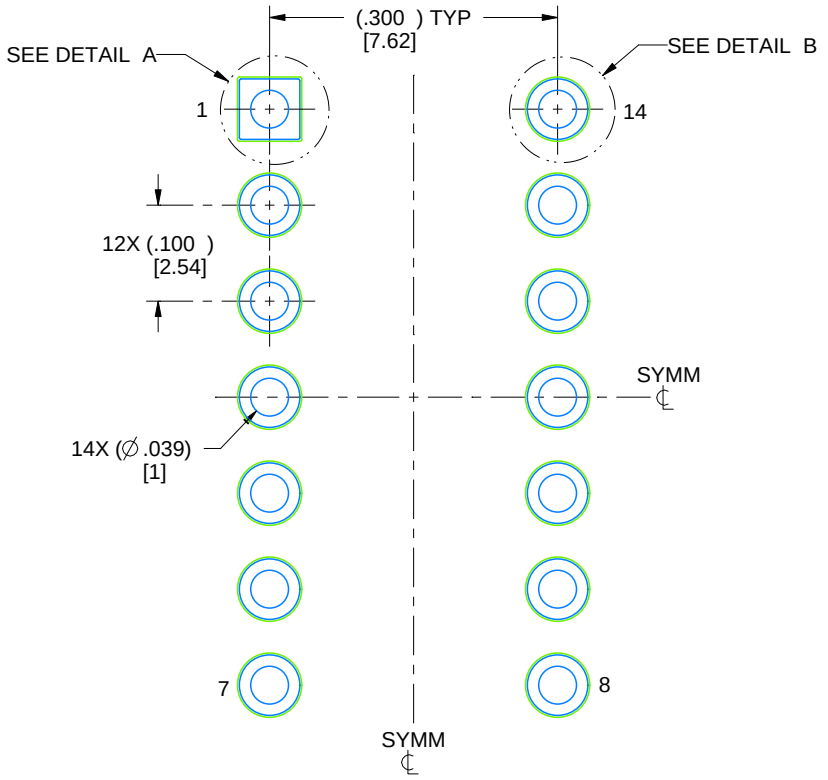
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

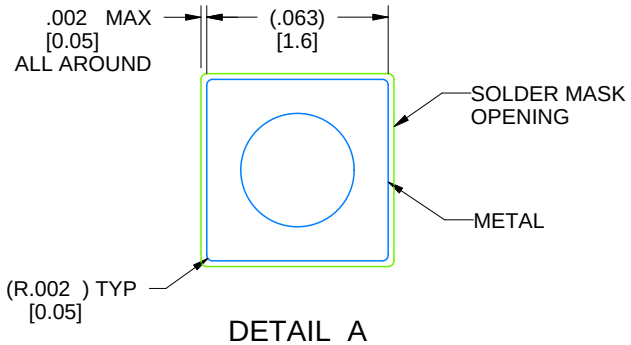
J0014A

CDIP - 5.08 mm max height

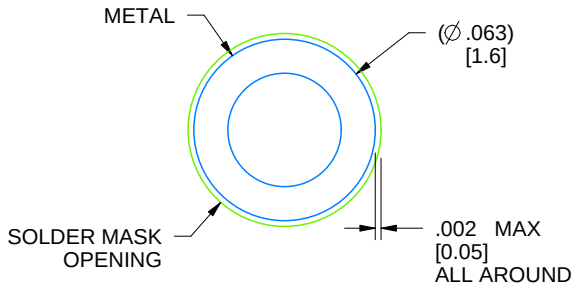
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



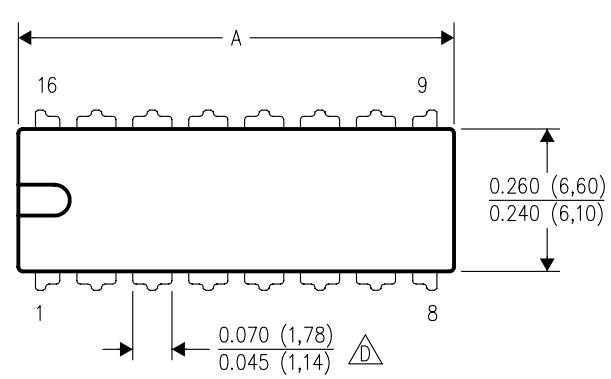
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

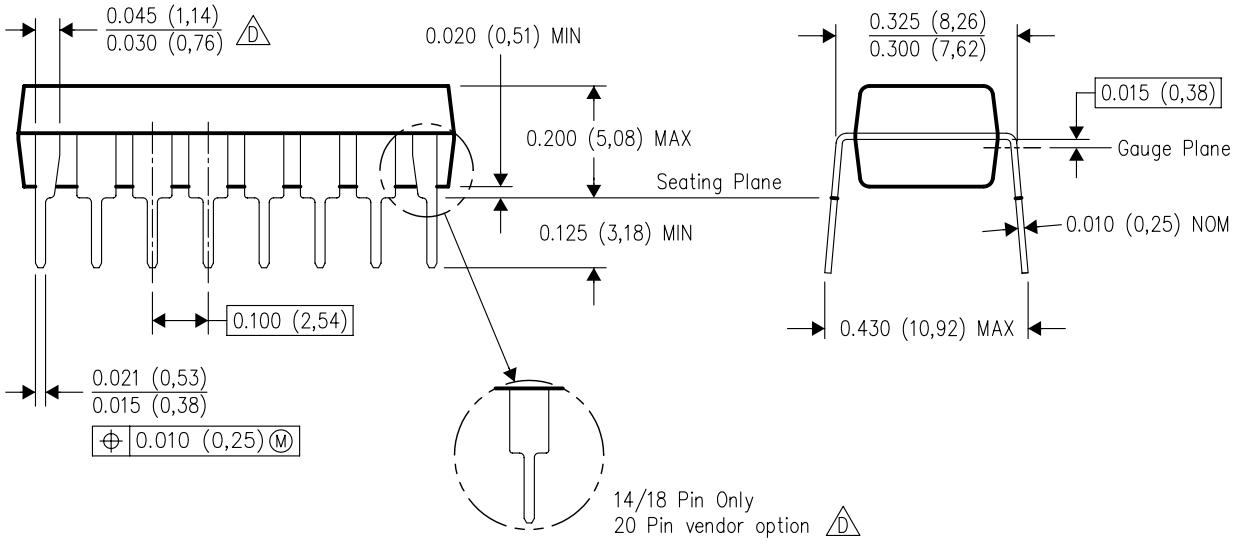
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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