

www.ti.com

HIGH-SPEED DIFFERENTIAL RECEIVER

FEATURES

- Controlled Baseline One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of Up to –55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree (1)
- 400-Mbps Signaling Rate (2) and 200-Mxfr/s Data Transfer Rate
- Operates With a Single 3.3-V Supply
- –4 V to 5 V Common-Mode Input Voltage Range
- Differential Input Thresholds < ±50 mV With 50 mV of Hysteresis Over Entire Common-Mode Input Voltage Range
- Integrated 110-Ω Line Termination Resistors On LVDT Products
- Complies With TIA/EIA-644 (LVDS)
- Active Failsafe Assures a High-Level Output With No Input
- Bus-Pin ESD Protection Exceeds 15-kV HBM
- Input Remains High-Impedance On Power Down
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.
- (2) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

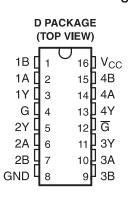
- TTL Inputs Are 5-V Tolerant
- Pin-Compatible With the AM26LS32, SN65LVDS32B, µA9637, SN65LVDS9637B

DESCRIPTION

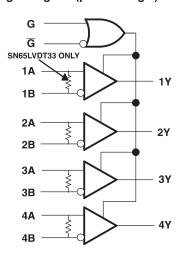
This family of four LVDS data line receivers offers the widest common-mode input voltage range in the industry. These receivers provide an input voltage range specification compatible with a 5-V PECL signal as well as an overall increased ground-noise tolerance. They are in industry standard footprints with integrated termination as an option.

Precise control of the differential input voltage thresholds allows for inclusion of 50 mV of input voltage hysteresis to improve noise rejection on slowly changing input signals. The input thresholds are still no more than +50 mV over the full input common-mode voltage range.

SN65LVDS33D



logic diagram (positive logic)



ORDERING INFORMATION(1)

T _A	PAC	TOP-SIDE MARKING		
–55°C to 125°C	SOIC - D	Reel of 2500	SN65LVDS33MDREP	LVDS33M
-55°C 10 125°C	SOIC - D	Reel of 2500	SN65LVDT33MDREP ⁽³⁾	LVDT33M

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (3) Product Preview



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



DESCRIPTION (CONTINUED)

The high-speed switching of LVDS signals usually necessitates the use of a line impedance matching resistor at the receiving-end of the cable or transmission media. The SN65LVDT series of receivers eliminates this external resistor by integrating it with the receiver. The nonterminated SN65LVDS series is also available for multidrop or other termination circuits.

The receivers can withstand ±15-kV human-body model (HBM) and ±600-V machine model (MM) electrostatic discharges to the receiver input pins with respect to ground without damage. This provides reliability in cabled and other connections where potentially damaging noise is always a threat.

The receivers also include a (patent pending) failsafe circuit that provides a high-level output within 600 ns after loss of the input signal. The most common causes of signal loss are disconnected cables, shorted lines, or powered-down transmitters. The failsafe circuit prevents noise from being received as valid data under these fault conditions. This feature may also be used for Wired-Or bus signaling. See *The Active Failsafe Feature of the SN65LVDS32B* application note.

The intended application and signaling technique of these devices is point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω . The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS33-EP is characterized for operation from -55°C to 125°C.

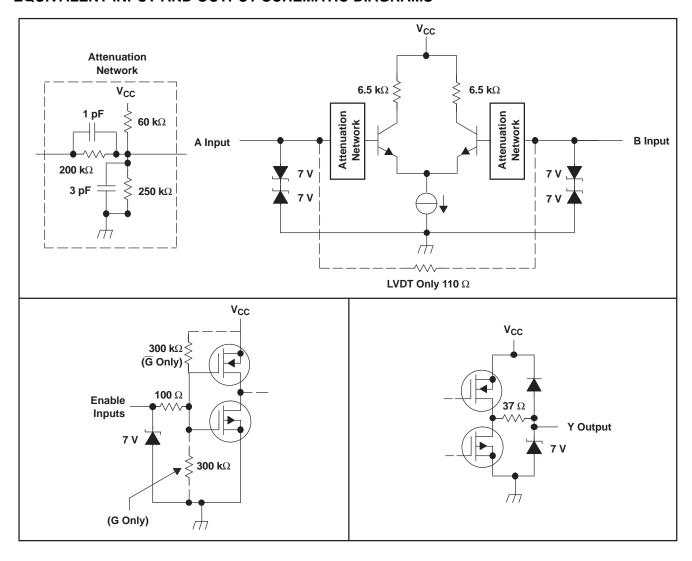
FUNCTION TABLE⁽¹⁾

SN65LVDS33	and SN65LVDT33			
DIFFERENTIAL INPUT	ENA	ENABLES		
$V_{ID} = V_A - V_B$	G	G	Υ	
\\ > 22 m\\	Н	Х	Н	
$V_{ID} \ge -32 \text{ mV}$	Х	L	Н	
400	Н	Х	?	
$-100 \text{ mV} < V_{\text{ID}} \le -32 \text{ mV}$	Х	L	?	
\/ < 400 m\/	Н	Х	L	
$V_{ID} \le -100 \text{ mV}$	Х	L	L	
X	L	Н	Z	
0	Н	Х	Н	
Open	X	L	Н	

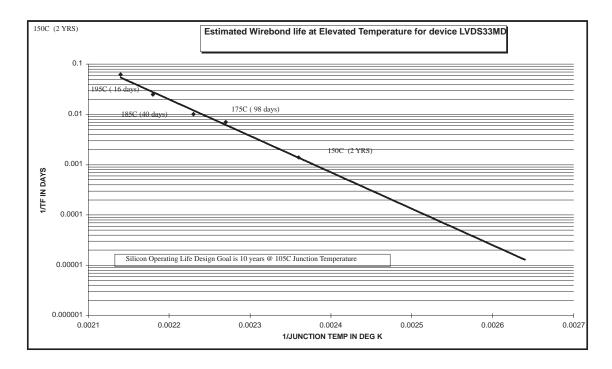
⁽¹⁾ H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate



EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS







ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE/UNIT
Supply voltage range, V _{CC}	(2)	-0.5 V to 4 V
	Enables or Y	-1 V to 6 V
Voltage range	A or B	−5 V to 6 V
	VA – VB (LVDT)	1 V
Electrostatic discharge	A, B, and GND ⁽³⁾	Class 3, A: 15 kV, B: 500 V
Charged-device mode	All pins (4)	±500 V
Continuous power dissipati	on	See Dissipation Rating Table
Storage temperature range		−65°C to 150°C
Lead temperature 1,6 mm	(1/16 inch) from case for 10 seconds	260°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATINGS

PACKAGE	$T_A \leq 25^{\circ}\text{C}$ POWER RATING	OPERATING FACTOR ⁽¹⁾ ABOVE T _A = 25°C	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D16	950 mW	7.6 mW/°C	494 mW	189 mW

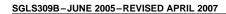
 This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.



SGLS309B-JUNE 2005-REVISED APRIL 2007

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		3	3.3	3.6	V
V _{IH}	High-level input voltage	Enables	2		5	V
V_{IL}	Low-level input voltage	Enables	0		8.0	V
IV 1	Magnitude of differential input valtage	LVDS	0.1		3	V
V _{ID}	Magnitude of differential input voltage				8.0	V
V _I or V _{IC}	Voltage at any bus terminal (separately	-4		5	°C	
T _A	Operating free-air temperature		- 55		125	C





ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER		TEST (CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT1}	Positive-going differential input	oing differential input voltage threshold		Fi 0			50	\/
V _{IT2}	Negative-going differential inp	ut voltage threshold	$V_{IB} = -4 \text{ V or 5 V, See}$	$V_{IB} = -4 \text{ V or 5 V}$, See Figure 2				mV
V _{IT3}	Differential input failsafe voltage	Differential input failsafe voltage threshold		e 5	-32		-100	mV
V _{ID(HYS)}	Differential input voltage hyste V _{IT1} – V _{IT2}	eresis,				50		V
V _{OH}	High-level output voltage		I _{OH} = -4 mA		2.4			V
V _{OL}	Low-level output voltage		I _{OL} = 4 mA				0.4	V
	Consult some st	CNICEL VID. 200	G at V _{CC} , No load,	Steady state		16	25	^
I _{CC}	Supply current	SN65LVDx33	G at GND			1.1	6	mA
			$V_I = 0 V$,	Other input open			±25	
		SN65LVDS	V _I = 2.4 V,	Other input open			±25	μΑ
l.	Input current (A or B inputs)	SINOSLVDS	$V_I = -4 V$,	Other input open			±80	
			V _I = 5 V,	Other input open			±45	
I ₁			V _I = 0 V,	Other input open			±50	
		SN65LVDT	V _I = 2.4 V,	Other input open			±50	
		SINOSEVDI	V₁ = −4 V,	Other input open			±180	μΑ
			V _I = 5 V,	Other input open			±95	
	Differential input current	SN65LVDS	V _{ID} = 100 mV,	V _{IC} = -4 V or 5 V			±5	μΑ
I _{IO}	$(I_{IA} - I_{IB})$	SN65LVDT	V _{ID} = 200 mV,	V _{IC} = -4 V or 5 V	1.55		2.4	mA
		CNICEL VIDO	V_A or $V_B = 0$ V or 2.4	/, V _{CC} = 0 V			±25	
	Power-off input current	SN65LVDS	V_A or $V_B = -4$ or 5 V, $V_{CC} = 0$ V				±60	
I _{I(OFF)}	(A or B inputs)	SN65LVDT	V_A or $V_B = 0$ V or 2.4 \	/, V _{CC} = 0 V			±35	μA
		SINOSLVDI	V_A or $V_B = -4$ V or 5 V, $V_{CC} = 0$ V				±120	
I _{IH}	High-level input current (enab	les)	V _{IH} = 2 V				12	μΑ
I _{IL}	Low-level input current (enable	es)	V _{IL} = 0.8 V				12	μA
l _{oz}	High-impedance output currer	nt			-10		12	μΑ
Cı	Input capacitance, A or B input	it to GND	$V_1 = 0.4 \sin (4E6\pi t) + 0.4 \sin (4E6\pi t)$	0.5 V		5		pF

⁽¹⁾ All typical values are at 25°C and with a 3.3-V supply.



SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH(1)}	Propagation delay time, low-to-high level output	Con Figure 2	1.8	4	8	ns
t _{PHL(1)}	Propagation delay time, high-to-low level output	See Figure 3	1.8	4	8	ns
t _{d1}	Delay time, failsafe deactivate time	C _L = 10 pF,			11	ns
t _{d2}	Delay time, failsafe activate time	See Figure 3 and Figure 6	0.2		2	μs
t _{sk(p)}	Pulse skew (t _{PHL(1)} - t _{PLH(1)})			200		ps
t _{sk(o)}	Output skew ⁽²⁾			150		ps
t _{sk(pp)}	Part-to-part skew ⁽³⁾	See Figure 3			1.2	ns
t _r	Output signal rise time			0.8		ns
t _f	Output signal fall time			0.8		ns
t _{PHZ}	Propagation delay time, high level-to-high impedance output			5.5	12	ns
t _{PLZ}	Propagation delay time, low level-to-high impedance output	Con Figure 4		4.4	12	ns
t _{PZH}	Propagation delay time, high impedance-to-high level output	See Figure 4		3.8	12	ns
t _{PZL}	Propagation delay time, high impedance-to-low level output			7	12	ns

- (1) All typical values are at 25°C and with a 3.3-V supply.
 (2) t_{sk(o)} is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all receivers of a single device with all of their inputs driven
- $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

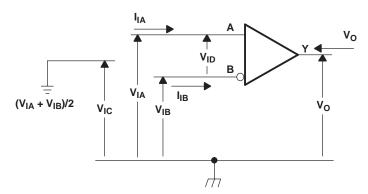
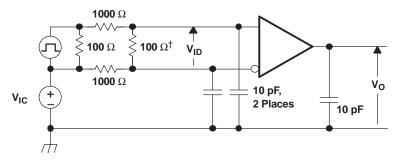
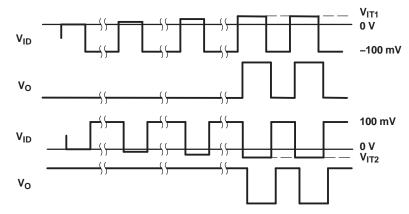


Figure 1. Voltage and Current Definitions





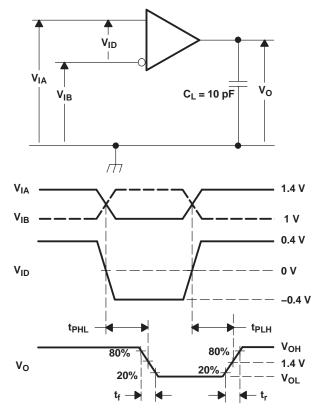
† Remove for testing LVDT device.



NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of <1 ns.

Figure 2. V_{IT1} and V_{IT2} Input Voltage Threshold Test Circuit and Definitions

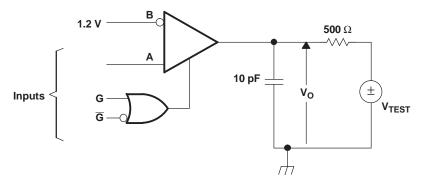




NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulsewidth = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 3. Timing Test Circuit and Waveforms





NOTE: All input pulses are supplied by a generator having the following characteristics: t_T or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

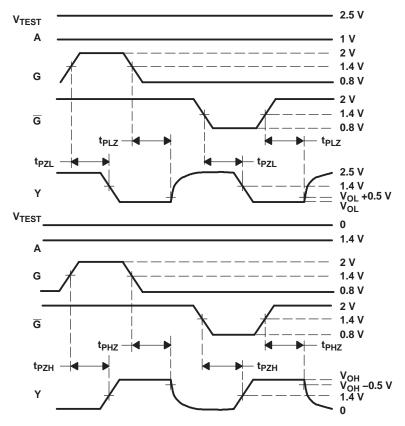


Figure 4. Enable/Disable Time Test Circuit and Waveforms



APPLIED V	OLTAGES ⁽¹⁾	RESULTANT INPUTS						
V _{IA} (mV)	V _{IB} (mV)	V _{ID} (mV)	V _{IC} (mV)	Output				
-4000	-3900	-100	-3950	L				
-4000	-3968	-32	-3984	Н				
4900	5000	-100	4950	L				
4968	5000	-32	4984	Н				

(1) These voltages are applied for a minimum of 1.5 μ s.

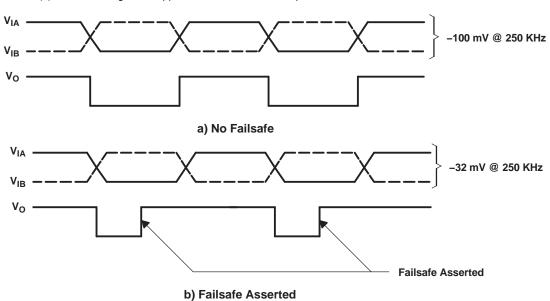


Figure 5. V_{IT3} Failsafe Threshold Test

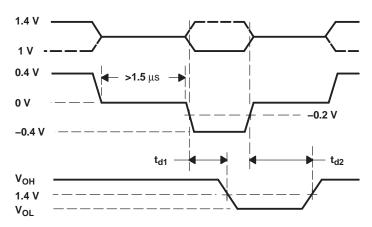
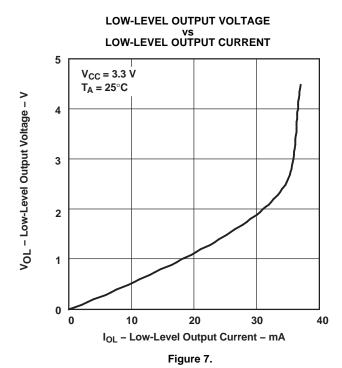


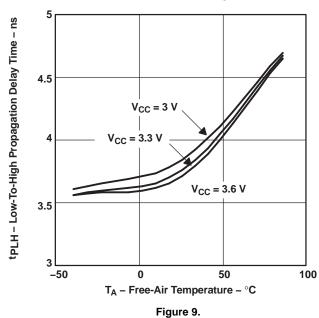
Figure 6. Waveforms for Failsafe Activate and Deactivate



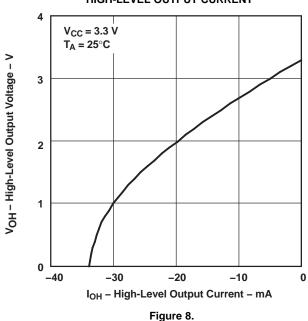
TYPICAL CHARACTERISTICS



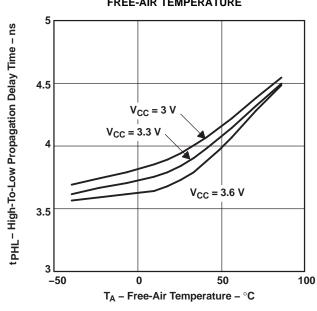
LOW-TO-HIGH PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE



HIGH-LEVEL OUTPUT VOLTAGE VS HIGH-LEVEL OUTPUT CURRENT

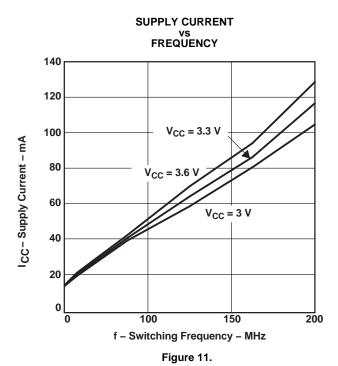


HIGH-TO-LOW PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE



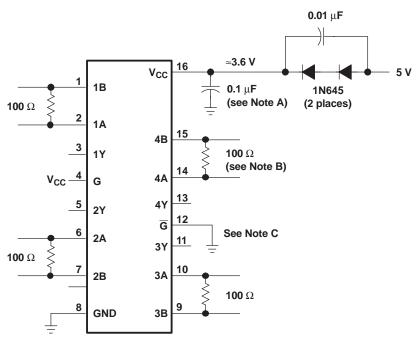


TYPICAL CHARACTERISTICS (continued)





APPLICATION INFORMATION



- A. Place a 0.1-μF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.
- B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.
- C. Unused enable inputs should be tied to V_{CC} or GND as appropriate.

Figure 12. Operation With 5-V Supply

RELATED INFORMATION

IBIS modeling is available for this device. Contact the local Texas Instruments sales office or the Texas Instruments Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- Low-Voltage Differential Signalling Design Notes (SLLA014)
- Interface Circuits for TIA/EIA-644 (LVDS) (SLLA038)
- Reducing EMI With LVDS (SLLA030)
- Slew Rate Control of LVDS Circuits (SLLA034)
- Using an LVDS Receiver With RS-422 Data (SLLA031)
- Evaluating the LVDS EVM (SLLA033)



APPLICATION INFORMATION (continued)

ACTIVE FAILSAFE FEATURE

A differential line receiver commonly has a failsafe circuit to prevent it from switching on input noise. Current LVDS failsafe solutions require either external components with subsequent reductions in signal quality or integrated solutions with limited application. This family of receivers has a new integrated failsafe that solves the limitations seen in present solutions. A detailed theory of operation is presented in application note, *The Active Failsafe Feature of the SN65LVDS32B* (SLLA082A).

Figure 13 shows one receiver channel with active failsafe. It consists of a main receiver that can respond to a high-speed input differential signal. Also connected to the input pair are two failsafe receivers that form a window comparator. The window comparator has a much slower response than the main receiver and it detects when the input differential falls below 80 mV. A 600-ns failsafe timer filters the window comparator outputs. When failsafe is asserted, the failsafe logic drives the main receiver output to logic high.

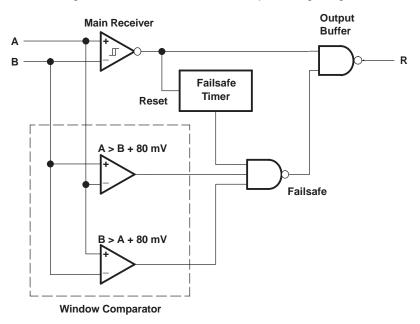


Figure 13. Receiver With Active Failsafe



APPLICATION INFORMATION (continued)

ECL/PECL-to-LVTTL CONVERSION WITH TI'S LVDS RECEIVER

The various versions of emitter-coupled logic (i.e., ECL, PECL and LVPECL) are often the physical layer of choice for system designers. Designers know of the established technology and that it is capable of high-speed data transmission. In the past, system requirements often forced the selection of ECL. Now technologies like LVDS provide designers with another alternative. While the total exchange of ECL for LVDS may not be a design option, designers have been able to take advantage of LVDS by implementing a small resistor divider network at the input of the LVDS receiver. Texas Instruments has taken the next step by introducing a wide common-mode LVDS receiver (no divider network required) which can be connected directly to an ECL driver with only the termination bias voltage required for ECL termination ($V_{CC} - 2 V$).

Figure 14 and Figure 15 show the use of an LV/PECL driver driving five meters of CAT-5 cable and being received by Texas Instruments wide common-mode receiver and the resulting eye-pattern. The values for R3 are required in order to provide a resistor path to ground for the LV/PECL driver. With no resistor divider, R1 simply needs to match the characteristic load impedance of 50 Ω . The R2 resistor is a small value and is intended to minimize any possible common-mode current reflections.

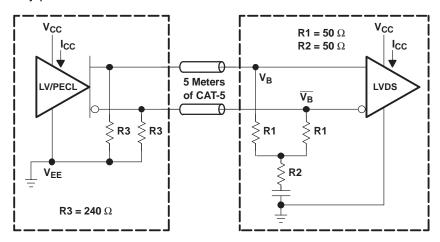


Figure 14. LVPECL or PECL to Remote Wide Common-Mode LVDS Receiver

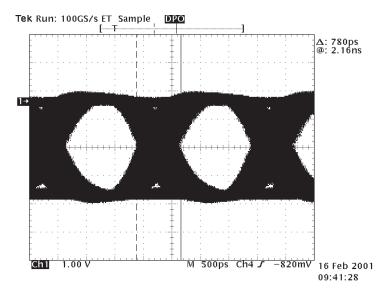


Figure 15. LV/PECL to Remote SN65LVDS33 at 500 Mbps Receiver Output (CH1)



APPLICATION INFORMATION (continued)

TEST CONDITIONS

- V_{CC} = 3.3 V
- T_A = 25°C (ambient temperature)
- All four channels switching simultaneously with NRZ data. The scope is pulse-triggered simultaneously with NRZ data.

EQUIPMENT

- Tektronix PS25216 programmable power supply
- Tektronix HFS 9003 stimulus system
- Tektronix TDS 784D 4-channel digital phosphor oscilloscope DPO

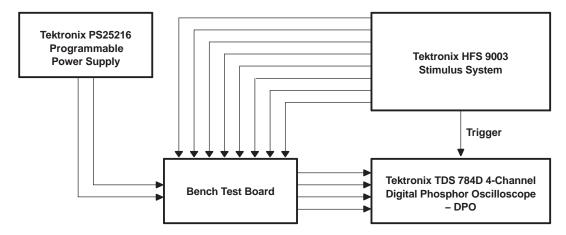


Figure 16. Equipment Setup

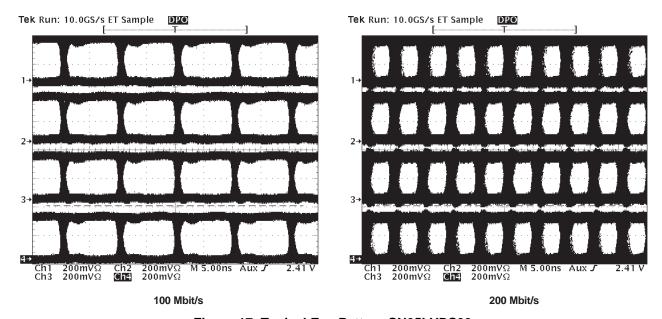


Figure 17. Typical Eye Pattern SN65LVDS33

www.ti.com 10-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN65LVDS33MDREP	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVDS33M
V62/05614-01XE	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVDS33M

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65LVDS33-EP:

Catalog: SN65LVDS33

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 10-Nov-2025

NOTE: Qualified Version Definitions:

 $_{\bullet}$ Catalog - TI's standard catalog product

PACKAGE MATERIALS INFORMATION

www.ti.com 5-Dec-2023

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS33MDREP	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 5-Dec-2023



*All dimensions are nominal

Ì	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ı	SN65LVDS33MDREP	SOIC	D	16	2500	350.0	350.0	43.0

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025