

HIGH-SPEED DIFFERENTIAL LINE DRIVER

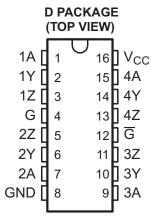
Check for Samples: SN65LVDS31-EP

FEATURES

- Meet or Exceed the Requirements of ANSI TIA/EIA-644 Standard
- Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and 100-Ω Load
- Typical Output Voltage Rise and Fall Times of 500 ps (400 Mbps)
- · Typical Propagation Delay Times of 1.7 ns
- Operate From a Single 3.3-V Supply
- Power Dissipation 25 mW Typical Per Driver at 200 MHz
- Driver at High Impedance When Disabled or With V_{CC} = 0
- Bus-Terminal ESD Protection Exceeds 8 kV
- · Low-Voltage TTL (LVTTL) Logic Input Levels
- Pin Compatible With AM26LS31, MC3487, and µA9638
- Cold Sparing for Space and High Reliability Applications Requiring Redundancy

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- · Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military (–55°C/125°C)
 Temperature Range
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability



DESCRIPTION

The SN65LVDS31 is a differential line driver that implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as TIA/EIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. This driver will deliver a minimum differential output voltage magnitude of 247 mV into a $100-\Omega$ load when enabled.

The intended application of this device and signaling technique is both point-to-point and multidrop (one driver and multiple receivers) data transmission over controlled impedance media of approximately 100 Ω . The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS31 is characterized for operation from -55°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





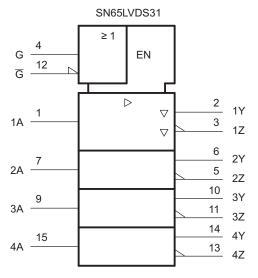
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	SOIC-D	SN65LVDS31MDREP	LVDS31EP	V62/07627-01XE

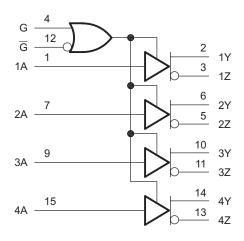
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Logic Symbol



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN65LVDS31 Logic Diagram (Positive Logic)



STRUMENTS

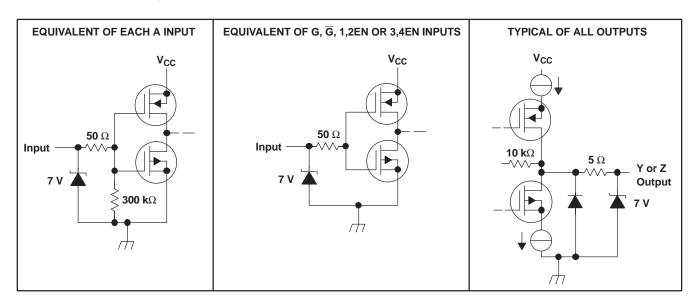
FUNCTION TABLE

Table 1. SN65LVDS31(1)

INPUT	ENA	BLES	OUTPUTS		
Α	G	G	Υ	Z	
Н	Н	Χ	Н	L	
L	Н	Χ	L	Н	
Н	X	L	Н	L	
L	Х	L	L	Н	
X	L	Н	Z	Z	
Open	Н	Χ	L	Н	
Open Open	Х	L	L	Н	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



TEXAS INSTRUMENTS

SLLSE91 – SEPTEMBER 2011 www.ti.com

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		UNIT
V_{CC}	Supply voltage range (2)	–0.5 V to 4 V
V_{I}	Input voltage range	–0.5 V to V _{CC} + 0.5 V
	Continuous total power dissipation	See Dissipation Rating Table
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
θ_{JA}	Thermal resistance, junction-to-ambient	73°C/W
θ_{JC}	Thermal resistance, junction-to-case	36.9°C/W
T _{stg}	Storage temperature range	–65°C to 150°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C	DERATING FACTOR ⁽¹⁾	T _A = 70°C	T _A = 85°C	T _A = 125°C
	POWER RATING	ABOVE T _A = 25°C	POWER RATING	POWER RATING	POWER RATING
D (16)	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW

⁽¹⁾ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
T _A	Operating free-air temperature	– 55		125	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST (MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{OD}	Differential output voltage magnitude	$R_L = 100 \Omega$,	See Figure 2	247	340	454	mV
ΔV_{OD}	Change in differential output voltage magnitude between logic states	$R_L = 100 \Omega$,	See Figure 2	-50		50	mV
V _{OC(SS)}	Steady-state common-mode output voltage	See Figure 3		1.125	1.2	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 3		-50		50	mV
V _{OC(PP)}	Peak-to-peak common-mode output voltage	See Figure 3			50		mV
	Supply current	$V_I = 0.8 \text{ V or 2 V},$	Enabled, No load		9	20	
I _{CC}		$V_I = 0.8 \text{ or } 2 \text{ V},$	$R_L = 100 \Omega$, Enabled		25	35	mA
		$V_I = 0$ or V_{CC} ,	Disabled		0.25	1	
I _{IH}	High-level input current	V _{IH} = 2			4	20	μΑ
I _{IL}	Low-level input current	V _{IL} = 0.8 V			0.1	10	μΑ
	Chart aircuit autout aureant	$V_{O(Y)}$ or $V_{O(Z)} = 0$			-4	-24	mA
los	Short-circuit output current	V _{OD} = 0				±12	mA
I _{OZ}	High-impedance output current	V _O = 0 or 2.4 V				±1	μΑ
I _{O(OFF)}	Power-off output current	V _{CC} = 0,	V _O = 2.4 V			±4	μΑ
Ci	Input capacitance				3		pF

⁽¹⁾ All typical values are at $T_A = 25^{\circ}C$ and with $V_{CC} = 3.3 \text{ V}$.

Submit Documentation Feedback

⁽²⁾ All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output		0.5	1.4	4	ns
t _{PHL}	Propagation delay time, high-to-low-level output		1	1.7	4.5	ns
t _r	Differential output signal rise time (20% to 80%)	$R_L = 100 \Omega, C_L = 10 pF,$		0.5		ns
t _f	Differential output signal fall time (80% to 20%)	See Figure 2		0.5		ns
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})			0.3	0.6	ns
t _{sk(o)}	Channel-to-channel output skew ⁽²⁾			0.3	0.8	ns
t _{PZH}	Propagation delay time, high-impedance-to-high-level output			5.4	17	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	Coo Figure 4		2.5	17	ns
t _{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 4		8.1	18	ns
t _{PLZ}	Propagation delay time, low-level-to-high-impedance output			7.3	17	ns

- (1) All typical values are at $T_A = 25^{\circ}C$ and with $V_{CC} = 3.3 \text{ V}$. (2) $t_{sk(o)}$ is the maximum delay time difference between drivers on the same device.

PARAMETER MEASUREMENT INFORMATION

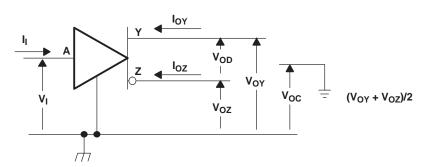
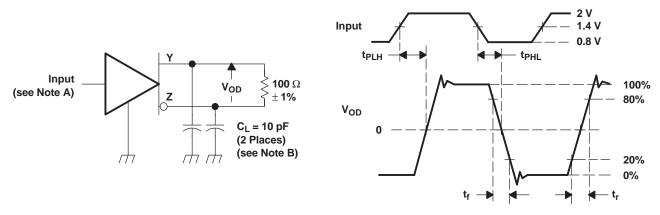


Figure 1. Voltage and Current Definitions

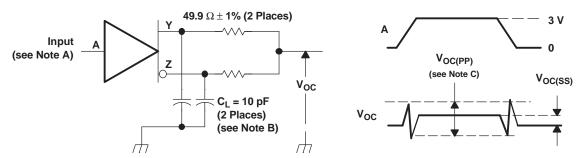


- NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
 - B. C_I includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

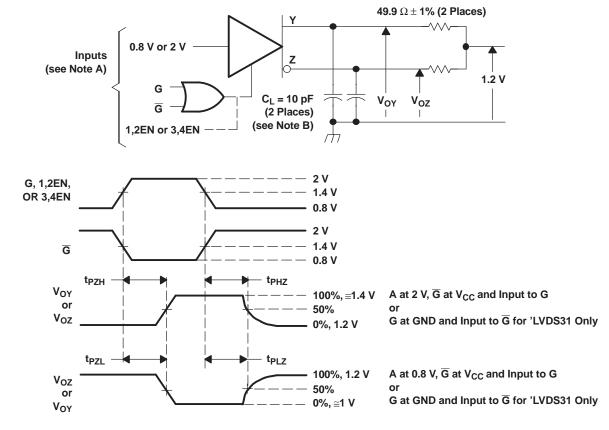


PARAMETER MEASUREMENT INFORMATION (continued)



- NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
 - B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.
 - C. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3-dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

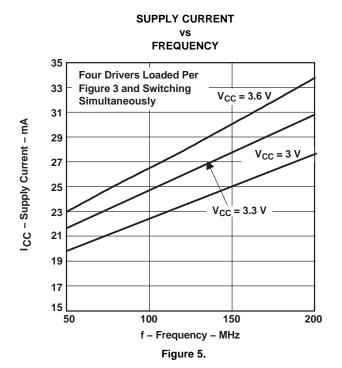


- NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f < 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns.
 - B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 4. Enable-/Disable-Time Circuit and Definitions



TYPICAL CHARACTERISTICS



FREE-AIR TEMPERATURE 2.8 t_{PLH} - Low-to-High Propagation Delay Time - ns 2.6 V_{CC} = 3.3 V V_{CC} = 3.6 V 2.4 2.2 $V_{CC} = 3 V$ 2 1.8

-40

 $\mathbf{T}_{\mathbf{A}}$ - Free-Air Temperature - °C

Figure 6.

25

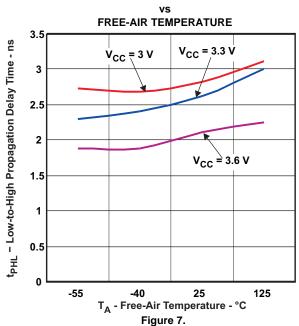
125

LOW-TO-HIGH PROPAGATION DELAY TIME

HIGH-TO-LOW PROPAGATION DELAY TIME

1.6

-55



SLLSE91 – SEPTEMBER 2011 www.ti.com

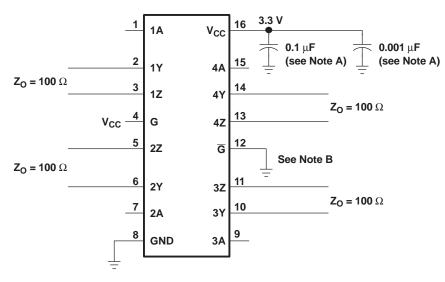
APPLICATION INFORMATION

The SN65LVDS31 is generally used as a building block for high-speed point-to-point data transmission where ground differences are less than 1 V. The SN65LVDS31 can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers approach ECL speeds without the power and dual supply requirements.

TRANSMISSION DISTANCE VS SIGNALING RATE 100 30% Jitter Transmission Distance - m (see Note A) 10 5% Jitter (see Note A) 24 AWG UTP 96 Ω (PVC Dielectric) 0.1 1000 10 100 Signaling Rate - Mbps

A. This parameter is the percentage of distortion of the unit interval (UI) with a pseudorandom data pattern.

Figure 8. Typical Transmission Distance Versus Signaling Rate



NOTES: A. Place a 0.1-μF and a 0.001-μF Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitors should be located as close as possible to the device terminals.

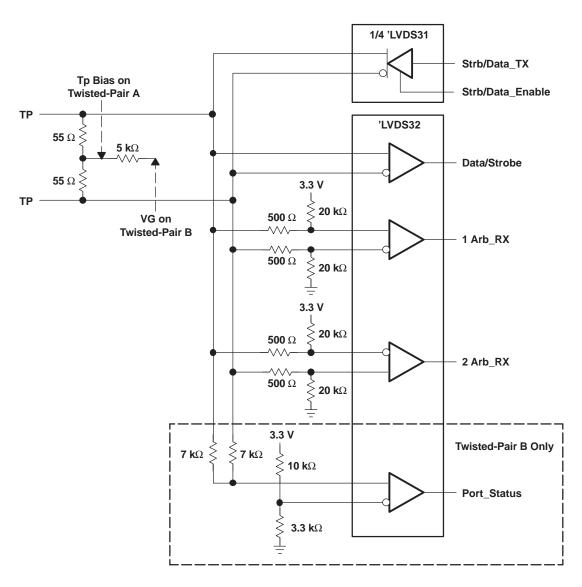
B. Unused enable inputs should be tied to $V_{\mbox{\footnotesize{CC}}}$ or GND, as appropriate.

Figure 9. Typical Application Circuit Schematic

Submit Documentation Feedback

NSTRUMENTS

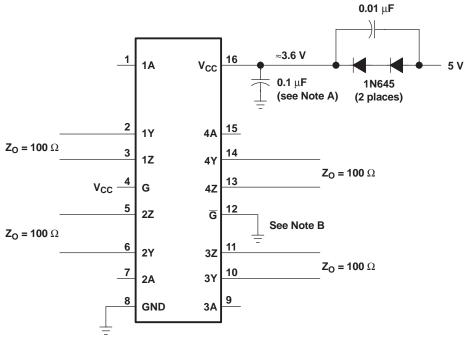




- NOTES: A. Resistors are leadless, thick film (0603), 5% tolerance.
 - B. Decoupling capacitance is not shown, but recommended.
 - C. V_{CC} is 3 V to 3.6 V.
 - D. The differential output voltage of the 'LVDS31 can exceed that specified by IEEE1394.

Figure 10. 100-Mbps IEEE 1394 Transceiver





- A. Place a 0.1-μF Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.
- B. Unused enable inputs should be tied to V_{CC} or GND, as appropriate.

Figure 11. Operation With 5-V Supply

COLD SPARING

Systems using cold sparing have a redundant device electrically connected without power supplied. To support this configuration, the spare must present a high-input impedance to the system so that it does not draw appreciable power. In cold sparing, voltage may be applied to an I/O before and during power up of a device. When the device is powered off, V_{CC} must be clamped to ground and the I/O voltages applied must be within the specified recommended operating conditions.

RELATED INFORMATION

IBIS modeling is available for this device. Contact the local TI sales office or the TI Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- Low-Voltage Differential Signaling Design Notes (SLLA014)
- Interface Circuits for TIA/EIA-644 (LVDS) (SLLA038)
- Reducing EMI With LVDS (SLLA030)
- Slew Rate Control of LVDS Circuits (SLLA034)
- Using an LVDS Receiver With RS-422 Data (SLLA031)
- Evaluating the LVDS EVM (SLLA033)

www.ti.com 11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN65LVDS31MDREP	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVDS31EP
V62/07627-01XE	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVDS31EP

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65LVDS31-EP:

Catalog: SN65LVDS31

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2025

NOTE: Qualified Version Definitions:

 $_{\bullet}$ Catalog - TI's standard catalog product

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025