













SN65HVD233-HT

SLLS933G -NOVEMBER 2008-REVISED JANUARY 2015

SN65HVD233-HT 3.3-V CAN Transceiver

Features

- Bus-Pin Fault Protection Exceeds ±36 V
- Bus-Pin ESD Protection Exceeds 16-kV Human Body Model (HBM)
- Compatible With ISO 11898
- Signaling Rates⁽¹⁾ up to 1 Mbps
- Extended -7-V to 12-V Common-Mode Range
- High-Input Impedance Allows for 120 Nodes
- LVTTL I/Os Are 5-V Tolerant
- Adjustable Driver Transition Times for Improved Signal Quality
- Unpowered Node Does Not Disturb the Bus
- Low-Current Standby Mode: 200 µA Typical
- Power-Up and Power-Down Glitch-Free Bus Inputs and Outputs
 - High-Input Impedance With Low V_{CC}
 - Monolithic Output During Power Cycling
- Loopback for Diagnostic Functions Available
- DeviceNet™ Vendor ID #806
- The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

2 Applications

- Down-Hole Drilling
- **High-Temperature Environments**
- **Industrial Automation**
 - DeviceNet Data Buses
 - Smart Distributed Systems (SDS™)
- SAE J1939 Data Bus Interfaces
- NMEA 2000 Data Bus Interfaces
- ISO 11783 Data Bus Interfaces
- **CAN Data Bus Interfaces**
- Controlled Baseline
- One Assembly or Test Site
- One Fabrication Site
- Available in Extreme (-55°C to 210°C) Temperature Range (1)
- Extended Product Life Cycle
- **Extended Product-Change Notification**
- **Product Traceability**
- Texas Instruments high-temperature products use highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.
- (1) Custom temperature ranges available

3 Description

The SN65HVD233 is used in applications employing controller area network (CAN) serial communication physical layer in accordance with the ISO 11898 standard, with the exception that the thermal shutdown is removed. As a CAN transceiver, the device provides transmit and receive capability between the differential CAN bus and a CAN controller, with signaling rates up to 1 Mbps.

Designed operation for in especially harsh environments, the device features cross wire, overvoltage, and loss-of-ground protection to ±36 V. with common-mode transient protection of ±100 V. This device operates over a -7-V to 12-V commonmode range with a maximum of 60 nodes on a bus.

If the common-mode range is restricted to the ISO 11898 standard range of -2 V to 7 V, up to 120 nodes may be connected on a bus. This transceiver interfaces the single-ended CAN controller with the differential CAN bus found in industrial, building automation, and automotive applications.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)				
	SOIC (8)	4.90 mm x 3.91 mm				
SN65HVD233-HT	CFP-HKJ (8)	6.90 mm x 5.65 mm				
SN05HVD233-H1	CFP-HKQ (8)	6.90 mm x 5.65 mm				
	CDIP SB (8)	40.64 mm x 10.04 mm				

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Functional Block Diagram

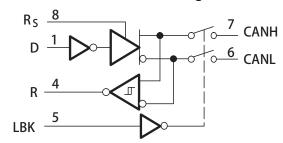




Table of Contents

1	Features 1	9	Detailed Description	20
2	Applications 1		9.1 Overview	20
3	Description 1		9.2 Functional Block Diagram	20
4	Revision History2		9.3 Feature Description	20
5	Description (Continued)3		9.4 Device Functional Modes	<mark>22</mark>
6	Pin Configuration and Functions	10	Application and Implementation	24
7	Specifications6		10.1 Application Information	24
•	7.1 Absolute Maximum Ratings		10.2 Typical Application	24
	7.2 ESD Ratings	11	Power Supply Recommendations	26
	7.3 Recommended Operating Conditions	12	Layout	26
	7.4 Thermal Information		12.1 Layout Guidelines	26
	7.5 Driver Electrical Characteristics		12.2 Layout Example	27
	7.6 Receiver Electrical Characteristics	13	Device and Documentation Support	28
	7.7 Driver Switching Characteristics		13.1 Trademarks	28
	7.8 Receiver Switching Characteristics		13.2 Electrostatic Discharge Caution	28
	7.9 Device Switching Characteristics		13.3 Glossary	28
	7.10 Typical Characteristics	14	Mechanical, Packaging, and Orderable	
8	Parameter Measurement Information 15		Information	28

4 Revision History

Changes from Revision F (August 2012) to Revision G

Page

Added Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation



5 Description (Continued)

 R_S (pin 8) provides for three modes of operation: high-speed, slope control, or low-power standby mode. The high-speed mode of operation is selected by connecting R_S directly to ground, thus allowing the driver output transistors to switch on and off as fast as possible with no limitation on the rise and fall slope. The rise and fall slope can be adjusted by connecting a resistor to ground at R_S , because the slope is proportional to the output current of the pin. Slope control is implemented with a resistor value of 10 k Ω to achieve a slew rate of

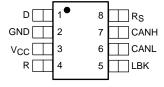
≉ 15 V/µs, and a value of 100 kΩ to achieve ≉ 2 V/µs slew rate. For more information about slope control, refer to the *Application and Implementation* section.

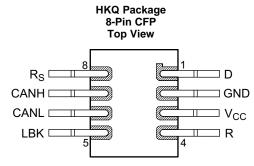
The SN65HVD233 enters a low-current standby mode, during which the driver is switched off and the receiver remains active if a high logic level is applied to R_S . The local protocol controller reverses this low-current standby mode when it needs to transmit to the bus.

A logic high on the loopback (LBK, pin 5) of the SN65HVD233 places the bus output and bus input in a high-impedance state. The remaining circuit remains active and available for the driver to receiver loopback, self-diagnostic node functions without disturbing the bus.

6 Pin Configuration and Functions







HKQ as formed or HKJ mounted dead bug.

Pin Functions

	PIN	TYPE	DESCRIPTION
NO.	NAME	ITPE	DESCRIPTION
1	D	I	CAN Transmit Data input (Low for dominant and HIGH for recessive bus states)
2	GND	Power	Ground connection
3	VCC	Power	VCC
4	R	0	CAN Receive data output
5	LBK	1	LoopBack (Active high to enable controller loopback mode)
6	CFANL	I/O	Low level CAN bus line
7	CANH	I/O	High level CAN bus line
8	Rs	I	High Speed, Slope control, and standby enable mode input.

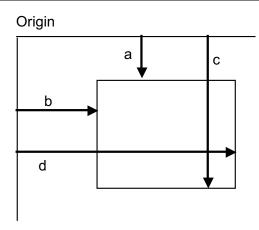
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Bare Die Information

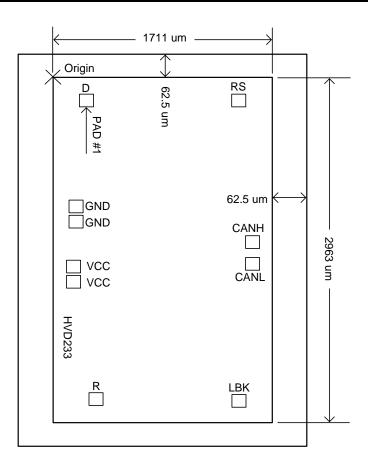
DIE THICKNESS	THICKNESS BACKSIDE FINISH		BOND PAD METALLIZATION COMPOSITION
15 mils.	Silicon with backgrind	GND	Al-Si-Cu (0.5%)



Bond Pad Coordinates In Microns - Rev A

DESCRIPTION	PAD NUMBER	Α	В	С	D
D	1	86.40	157.85	203.40	274.85
GND	2	1035.05	69.75	1150.05	184.75
GND	3	1168.15	69.75	1283.15	184.75
VCC	4	1572.05	51.85	1687.05	166.85
VCC	5	1711.95	51.85	1826.95	166.85
R	6	2758.85	237.65	2873.85	352.65
LBK	7	2774.25	1429.985	2889.25	1544.95
CANL	8	1549.90	1544.95	1664.90	1659.95
CANH	9	1351.45	1544.95	1466.45	1659.95
RS	10	83.50	1429.95	198.50	1544.95







7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.3	7	V
	Voltage range at any bus terminal (CANH or CANL)	-36	36	V
	Voltage input range, transient pulse (CANH and CANL) through 100 Ω (see Figure 19)	-100	100	V
V_{I}	Input voltage range (D, R, R _S , LBK)	-0.5	7	V
Io	Receiver output current	-10	10	mA
T _{stg}	Storage temperature	-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC	CANH, CANL, and GND	±16000	
V(500)	discharge	JS-001, all pins ⁽¹⁾	All pins	±3000	V
		Charged device model (CDM), per JEDEC specification	n JESD22-C101, all pins ⁽²⁾	±1000	

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

 $T_{\Delta} = -55^{\circ}C$ to 210°C

			MIN	MAX	UNIT
V _{CC}	Supply voltage		3	3.6	V
	Voltage at any bus terminal (separat	ely or common mode)	-7		V
V _{IH}	High-level input voltage	D, LBK	2	5.5	V
V_{IL}	Low-level input voltage	D, LBK	0	0.8	V
V _{ID}	Differential input voltage		-6	6	V
	Resistance from R _S to ground		0	100	kΩ
V _{I(Rs)}	Input voltage at R _S for standby		0.75 V _{CC}	5.5	V
	High level systems symmet	Driver	-50		^
I _{OH}	High-level output current	Receiver	-10	12 5.5 0.8 6 100 5.5	mA
	Lauren and and an annual	Driver		50	1
I _{OL}	Low-level output current	Receiver		10	mA
T _J	Operating junction temperature			212	°C
T _A	Operating free-air temperature ⁽¹⁾		-55	210	°C

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

⁽²⁾ All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



7.4 Thermal Information

			SN65HVD233-HT					
	THERMAL METRIC ⁽¹⁾	D	HJK/HKQ	JDJ	UNIT			
		8 PINS	8 PINS	8 PINS				
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.4	146.1	72.7				
R ₀ JC(top)	Junction-to-case (top) thermal resistance	55.8	23.7	3.1				
$R_{\theta JB}$	Junction-to-board thermal resistance	46.5	152.0	38.3	°C/W			
Ψ_{JT}	Junction-to-top characterization parameter	10.7	20.7	6.0				
ΨЈВ	Junction-to-board characterization parameter	45.9	93.1	26.9				

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.



7.5 Driver Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

	DADAME	TED		TEST CONDITIONS	T _A = -	55°C to	125°C	$T_A = 175^{\circ}C^{(1)}$			$T_A = 210^{\circ}C^{(2)}$			UNIT
	PARAME	IEK		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNII
.,	Bus outp	ut	CANH	$D = 0 V, R_S = 0 V,$	2.45		V_{CC}	2.45		V_{CC}	2.45		V_{CC}	.,
$V_{O(D)}$	voltage (dominar	nt)	CANL	See Figure 13 and Figure 14	0.5		1.25	0.5		1.25	0.5		1.25	V
	Bus outp	ut	CANH	D = 3 V, R _S = 0 V,		2.3			2.3			2.3		
Vo	voltage (recessiv	e)	CANL	See Figure 13 and Figure 14		2.3			2.3			2.3		V
V	Differenti	al ou	ıtput	D = 0 V, R _S = 0 V, See Figure 13 and Figure 14	1.5	2	3	1.4	1.75	3	1.4	1.75	3	V
$V_{OD(D)}$	voltage (l	Dom	inant)	D = 0 V, R _S = 0 V, See Figure 14 and Figure 15	1.1	2	3	1.1	1.47	3	1.1	1.47	3	V
V_{OD}	Differential output			D = 3 V, R _S = 0 V, See Figure 13 and Figure 14	-120		12	-120		12	-120		12	mV
	voltage (voltage (Recessive)		$D = 3 \text{ V}, R_S = 0 \text{ V}, \text{No}$ load	-0.5		0.05	-0.5		0.8	-0.5		1.2	V
V _{OC(pp)}	Peak-to-peak common-mode output voltage			See Figure 21		1			1			1		V
I _{IH}	High-leve		D, LBK	D = 2 V	-30		30	-30		30	-30		30	μΑ
I _{IL}	Low-leve		D, LBK	D = 0.8 V	-30		30	-30		30	-30		30	μΑ
	-	,		V _{CANH} = -7 V, CANL open, See Figure 24	-250			-250			-250			
laa	Short-circ	cuit c	output	V _{CANH} = 12 V, CANL open, See Figure 24			1			1			1	mA
los	current			V _{CANL} = -7 V, CANH open, See Figure 24	-1			-1			-1			ША
				V _{CANL} = 12 V, CANH open, See Figure 24			250			250			250	
Co	Output ca	apac	itance	See receiver input capacitance										
I _{IRs(s)}	R _S input current for standby		ent for	R _S = 0.75 V _{CC}	-10			-10			-10			μΑ
		Sta	ndby	$R_S = V_{CC}$, $D = V_{CC}$, LBK = 0 V		200	600		400	600		400	600	μΑ
I _{CC}	Supply current	Dor	minant	D = 0 V, No load, LBK = 0 V, R _S = 0 V			6			6			6	mA
		Red	cessive	D =t V_{CC} , No load, LBK = 0 V, R_S = 0 V			6			6			6	ША

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Minimum and maximum parameters are characterized for operation at T_A = 175°C and production tested at T_A = 125°C. Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.



7.6 Receiver Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

	DADAM		TEST 06	NETIONS	T _A = -	55°C to	125°C	T _A	= 175°	C ⁽¹⁾	$T_A = 210^{\circ}C^{(2)}$			LINIT
	PARAME	EIEK	TEST CC	NDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V _{IT+}	Positive- threshold	going input d voltage				620	900		600	900		600	900	mV
V _{IT}	Negative input thre voltage		LBK = 0 V, See Table 1		500	715		500	725		500	725		mV
V _{hys}	Hysteres (V _{IT+} – V	sis voltage ′ _{IT} _)				100			140			140		mV
V _{OH}	High-leve voltage	el output	$I_O = -4$ mA, See	e Figure 18	2.4			2.4			2.4			V
V _{OL}	Low-level output voltage		I _O = 4 mA, See	Figure 18			0.4			0.4			0.4	V
			CANH or CANL = 12 V		140		500	140		500	140		500	
	Puo innu	t current	CANH or CANL = 12 V, V _{CC} = 0 V	Other bus pin = 0 V, D = 3 V, LBK = 0 V, R _S = 0 V,	200		600	200		700	200		800	μA
I _I	Bus Iripu	it current	CANH or CANL = -7 V		-610		-150	-610		-150	-610		-150	μ/ (
			CANH or CANL = -7 V, V _{CC} = 0 V		-450		-130	-450		-130	-450		-130	
Cı		pacitance or CANL)	Pin to ground, V _I = 0.4 sin (4E D = 3 V, LBK =			45			55			55		pF
C _{ID}	Different capacita		Pin to pin, V _I = 0.4 sin (4E D = 3 V, LBK =			15			15			15		pF
R _{ID}	Different resistance		D 2V I DK	0.1/	40		110	40		110	40		110	kΩ
R _{IN}	Input res (CANH o	istance or CANL)	D = 3 V, LBK = 0 V		20		51	19		51	18		51	kΩ
		Standby	$R_S = V_{CC}, D = V_{CC}$	V _{CC} , LBK = 0 V		200	600		400	600		400	600	μΑ
I _{CC}	Supply	Dominant	D = 0 V, No loa LBK = 0 V	d, R _S = 0 V,			6			6			6	m ^
	current	Recessive	D = V _{CC} , No loa LBK = 0 V	ad, $R_S = 0 \text{ V}$,			6			6			6	mA

⁽¹⁾ Minimum and maximum parameters are characterized for operation at $T_A = 210^{\circ}$ C and are not chacterized or production tested at $T_A = 175^{\circ}$ C.

⁽²⁾ Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.



7.7 Driver Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

	DADAMETED	TEST CONDITIONS	T _A = -	55°C to	125°C	T _A	= 175°(C ⁽¹⁾	T _A :	= 210°C	C ⁽²⁾	UNIT
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNII
		R _S = 0 V, See Figure 16		35	85		50			50		
t _{PLH}	Propagation delay time, low-to-high-level	R_S with 10 k Ω to ground, See Figure 16		70	125		75			75		ns
	output	R_S with 100 k Ω to ground, See Figure 16		500	870		500			500		
	Propagation delay	R _S = 0 V, See Figure 16		70	120		70			70		
t _{PHL}	time, high-to-low-level	R_S with 10 k Ω to ground, See Figure 16		130	180		130			130		ns
	output	R_S with 100 k Ω to ground, See Figure 16		870	1200		870			870		
	Pulse skew $_{sk(p)}$ $(t_{PHL} - t_{PLH})$	R _S = 0 V, See Figure 16		35			9			9		
t _{sk(p)}		R_S with 10 k Ω to ground, See Figure 16		60			35			35		ns
		R_S with 100 k Ω to ground, See Figure 16		370			475			475		
t _r	Differential output signal rise time	R _S = 0 V, See Figure 16	20		70	20		75	20		75	20
t _f	Differential output signal fall time	R _S = 0 V, See Figure 16	18		70	20		75	20		75	ns
t _r	Differential output signal rise time	R_S with 10 k Ω to ground,	30		135	30		140	30		140	
t _f	Differential output signal fall time	See Figure 16	30		135	30		140	30		140	ns
t _r	Differential output signal rise time	R_S with 100 k Ω to ground,	250		1400	250		1400	250		1400	
t _f	Differential output signal fall time	See Figure 16	350		1400	350		1400	350		1400	ns
t _{en(s)}	Enable time from standby to dominant	See Figure 20		0.6	1.5		0.6	1.5		0.6	1.5	μs

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Minimum and maximum parameters are characterized for operation at T_A = 210°C but not production tested at T_A = 175°C or 210°C. Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.



7.8 Receiver Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A = -55°C to 125°C			$T_A = 175^{\circ}C^{(1)}$			$T_A = 210^{\circ}C^{(2)}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNII
t _{PLH}	Propagation delay time, low-to- high-level output			35	60		50	60		50	60	ns
t _{PHL}	Propagation delay time, high- to-low-level output	See Figure 18		35	60		45	60		45	60	ns
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})	Goo i iguio io		7			5			5		ns
t _r	Output signal rise time			2	6.5		6.5	8		6.5	8	ns
t _f	Output signal fall time			2	6.5		6.5	9		6.5	9	ns

7.9 Device Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

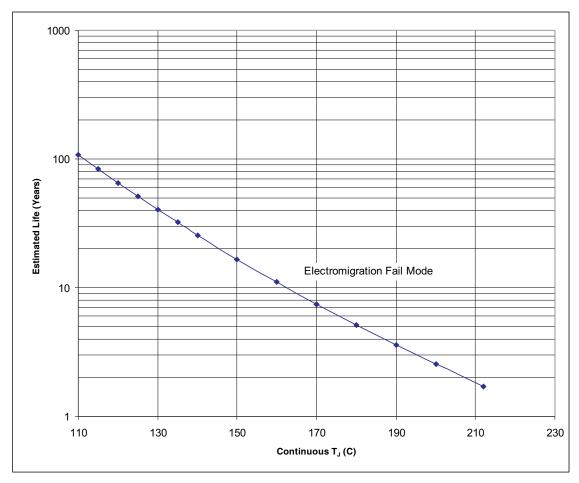
PARAMETER		TEST COMPITIONS	T _A = -55°C to 125°C			$T_A = 175^{\circ}C^{(1)}$			$T_A = 210^{\circ}C^{(2)}$			UNIT	
		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNII	
t _(LBK)	Loopback delay, driver input to receiver output	See Figure 23		7.5	15		12	15		12	15	ns	
Total loop delay, driver input to receiver output, recessive to dominant	Total loop delay	R _S = 0 V, See Figure 22		70	135		90	135		90	135		
	driver input to	R_S with 10 k Ω to ground, See Figure 22		105	190		115	190		115	190	ns	
	R_S with 100 k Ω to ground, See Figure 22		535	1000		430	1000		430	1000			
	Total loop delay,	R _S = 0 V, See Figure 22		70	135		98	135		98	135		
t _(loop2)	driver input to receiver output, dominant to recessive	R_S with 10 k Ω to ground, See Figure 22		105	190		150	190		150	190	ns	
		R_S with 100 k Ω to ground, See Figure 22		535	1100		880	1200		880	1200		

Product Folder Links: SN65HVD233-HT

Minimum and maximum parameters are characterized for operation at $T_A = 210^{\circ}\text{C}$ but not production tested at $T_A = 175^{\circ}\text{C}$ or 210°C . Minimum and maximum parameters are characterized for operation at $T_A = 210^{\circ}\text{C}$ but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.

Minimum and maximum parameters are characterized for operation at $T_A = 210^{\circ}\text{C}$ but not production tested at $T_A = 175^{\circ}\text{C}$ or 210°C . Minimum and maximum parameters are characterized for operation at $T_A = 210^{\circ}\text{C}$ but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.



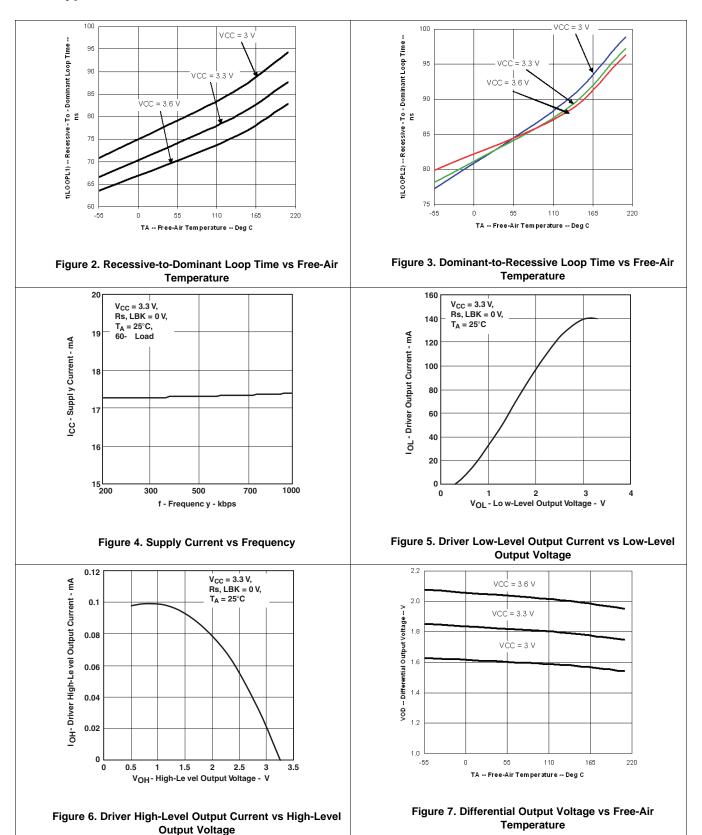


- A. See the Specifications for absolute maximum and minimum recommended operating conditions.
- B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

Figure 1. Operating Life Derating Chart SN65HVD233HD, SN65HVD233SJD, SN65HVD233SKGDA, SN65HVD233SHKJ, SN65HVD233SHKQ



7.10 Typical Characteristics



TEXAS INSTRUMENTS

Typical Characteristics (continued)

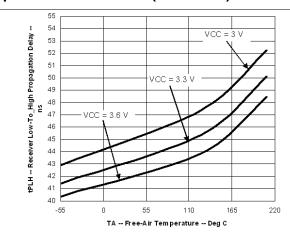


Figure 8. Receiver Low-to-High Propagation Delay vs Free-Air Temperature

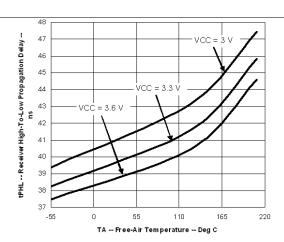


Figure 9. Receiver High-to-Low Propagation Delay vs Free-Air Temperature

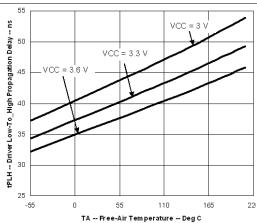


Figure 10. Driver Low-to-High Propagation Delay vs Free-Air Temperature

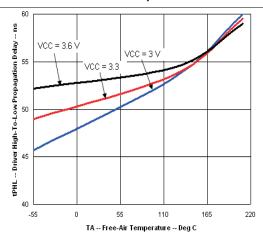


Figure 11. Driver High-to-Low Propagation Delay vs Free-Air Temperature

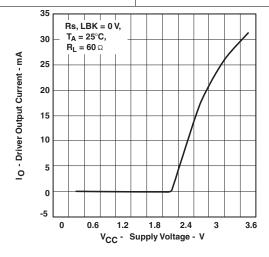


Figure 12. Driver Output Current vs Supply Voltage



Parameter Measurement Information

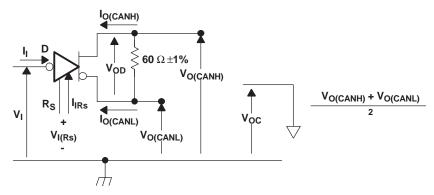


Figure 13. Driver Voltage, Current, and Test Definition

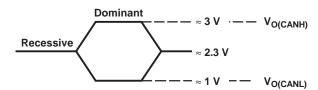


Figure 14. Bus Logic State Voltage Definitions

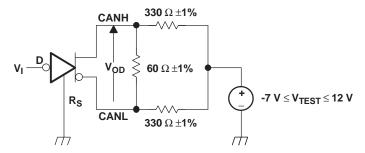
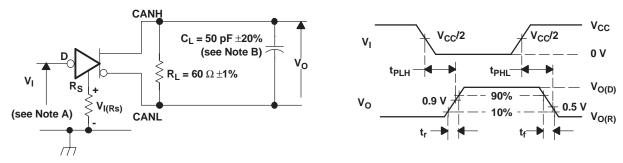


Figure 15. Driver V_{OD}



- The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50 \Omega$.
- C_L includes fixture and instrumentation capacitance.

Figure 16. Driver Test Circuit and Voltage Waveforms

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Parameter Measurement Information (continued)

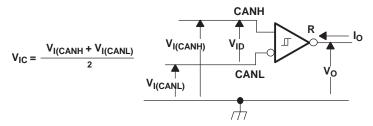
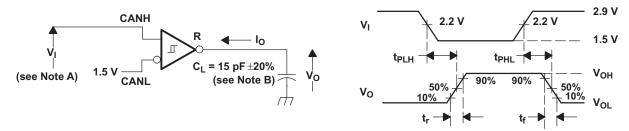


Figure 17. Receiver Voltage and Current Definitions

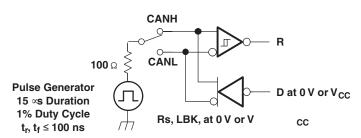


- A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) \leq 125 kHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O =$ 50 Ω .
- B. C_L includes fixture and instrumentation capacitance.

Figure 18. Receiver Test Circuit and Voltage Waveforms

INPUT OUTPUT **MEASURED** R **V_{CANH} V_{CANL}** |V_{ID}| 900 mV –6.1 V -7 V L 12 V 11.1 V L 900 mV V_{OL} -1 V -7 V 6 V L 6 V 12 V 6 V L -7 V Н -6.5 V 500 mV 12 V 11.5 V Н 500 mV -7 V -1 V Η 6 V V_{OH} 6 V 12 V 6 V Н Н Χ Open Open

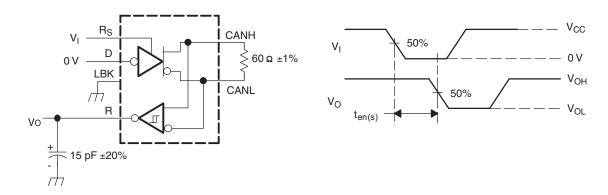
Table 1. Differential Input Voltage Threshold Test



NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

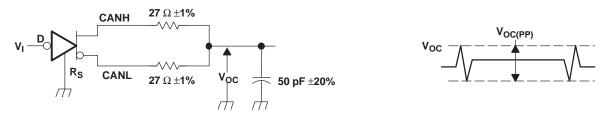
Figure 19. Test Circuit, Transient Overvoltage Test





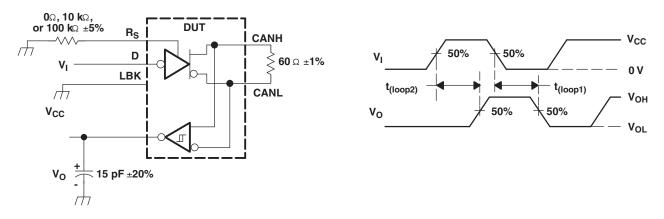
NOTE: All VI input pulses are supplied by a generator having the following characteristics: tr or tf ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 20. T_{en(s)} Test Circuit and Voltage Waveforms



NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

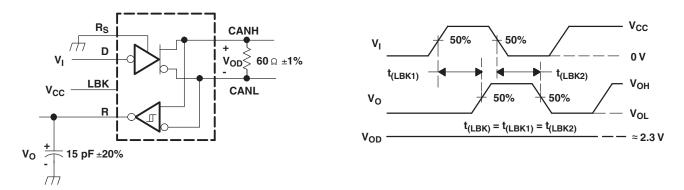
Figure 21. V_{OC(pp)} Test Circuit and Voltage Waveforms



NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 22. T_(loop) Test Circuit and Voltage Waveforms





NOTE: All V_I input pulses are supplied by agenerator having the following characteristics: t_r or $t_f \le 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 23. T_(LBK) Test Circuit and Voltage Waveforms

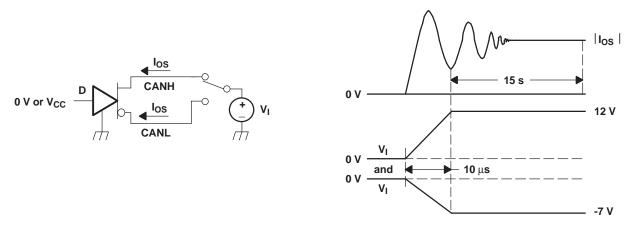
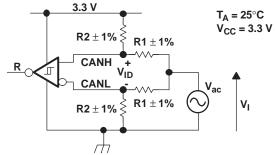


Figure 24. I_{OS} Test Circuit and Waveforms





The R Output State Does Not Change During Application of the Input Waveform.

V _{ID}	R1	R2		
500 mV	50 Ω	280 Ω		
900 mV	50 Ω	130 Ω		



NOTE: All input pulses are supplied by a generator with $f \le 1.5$ MHz.

Figure 25. Common-Mode Voltage Rejection



9 Detailed Description

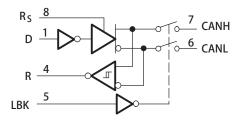
9.1 Overview

Controller Area Network (CAN) is a robust multi master-master, differential signaling, serial communications bus specified by the ISO 11898 family of standards. TI's SSN65HVD23x family of transceivers solve specialized networking requirements for various applications.

Table 2. Available Options

ORDERABLE PART NUMBER	LOW-POWER MODE	SLOPE CONTROL	DIAGNOSTIC LOOPBACK	AUTOBAUD LOOPBACK
SN65HVD233HD				
SN65HVD233SJD				
SN65HVD233SKGDA	200-µA standby mode	Adjustable	Yes	No
SN65HVD233SHKJ				
SN65HVD233SHKQ				

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 ISO 11898 Compliance of SN65HVD23x Family of 3.3-V CAN Transceivers

Many users value the low power consumption of operating CAN transceivers from a 3.3-V supply. However, some are concerned about the interoperability with 5-V supplied transceivers on the same bus. This section analyzes this situation to address those concerns.

9.3.1.1 Differential Signal

CAN is a differential bus where complementary signals are sent over two wires, and the voltage difference between the two wires defines the logical state of the bus. The differential CAN receiver monitors this voltage difference and outputs the bus state with a single-ended output signal.



Feature Description (continued)

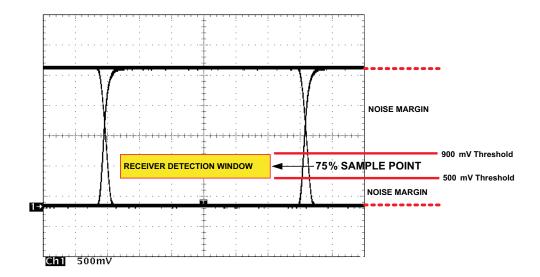


Figure 26. Typical SN65HVD23x Differential Output Voltage Waveform

The CAN driver creates the difference voltage between CANH and CANL in the dominant state. The dominant differential output of the SN65HVD23x is greater than 1.5 V and less than 3 V across a $60-\Omega$ load. The minimum required by ISO 11898 is 1.5 V and the maximum is 3 V. These are the same limiting values for 5-V supplied CAN transceivers. The bus termination resistors drive the recessive bus state and not the CAN driver.

A CAN receiver is required to output a recessive state with less than 500 mV and a dominant state with more than 900-mV difference voltage on its bus inputs. The CAN receiver must do this with common-mode input voltages from -2 V to 7 V. The SN65HVD23x family receivers meet these same input specifications as 5-V supplied receivers.

9.3.1.1.1 Common-Mode Signal

A common-mode signal is an average voltage of the two signal wires that the differential receiver rejects. The common-mode signal comes from the CAN driver, ground noise, and coupled bus noise. Obviously, the supply voltage of the CAN transceiver has nothing to do with noise. The SN65HVD23x family driver lowers the common-mode output in a dominant bit by a couple hundred millivolts from that of most 5-V drivers. While this does not fully comply with ISO 11898, this small variation in the driver common-mode output is rejected by differential receivers and does not affect data, signal noise margins, or error rates.

9.3.1.2 Interoperability Of 3.3-V CAN in 5-V CAN Systems

The 3.3-V-supplied SN65HVD23x family of CAN transceivers are electrically interchangeable with 5-V CAN transceivers. The differential output is the same. The recessive common-mode output is the same. The dominant common-mode output voltage is a couple hundred millivolts lower than 5-V-supplied drivers, while the receivers exhibit identical specifications as 5-V devices.

Electrical interoperability does not assure interchangeability however. Most implementers of CAN buses recognize that ISO 11898 does not sufficiently specify the electrical layer and that strict standard compliance alone does not ensure interchangeability. This comes only with thorough equipment testing.



9.4 Device Functional Modes

9.4.1 Function Tables

Table 3. Function Table (Driver)(1)

DRIVER									
	INPUTS		OUTPUTS						
D	LBK	R_s	CANH CANL BUS STATE						
X	X	>0.75 V _{CC}	Z	Z	Recessive				
L	L or open	<0.22.1/	Н	L	Dominant				
H or open	Х	≤0.33 V _{CC}	Z	Z	Recessive				
X	Н	≤0.33 V _{CC}	Z	Z	Recessive				

(1) H = high level, L = low level, Z = high impedance, X = irrelevant, ? = indeterminate

Table 4. Function Table (Receiver)

	RECEIVER									
	OUTPUT									
BUS STATE	BUS STATE V _{ID} = V _(CANH) – V _(CANL) LBK D									
Dominant	V _{ID} ≥ 0.9 V	L or open	Х	L						
Recessive	V _{ID} ≤ 0.5 V or open	L or open	H or open	Н						
?	0.5 V < V _{ID} < 0.9 V	L or open	H or open							
Х	X	11	L	L						
Х	X	- H	Н	Н						

9.4.2 Equivalent Input and Output Schematic Diagrams

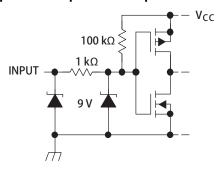


Figure 27. D Input

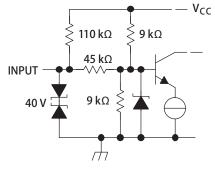


Figure 29. CANH Input

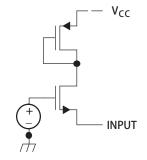


Figure 28. R_S Input

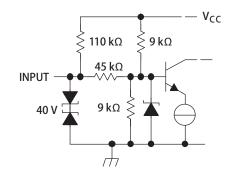


Figure 30. CANL Input



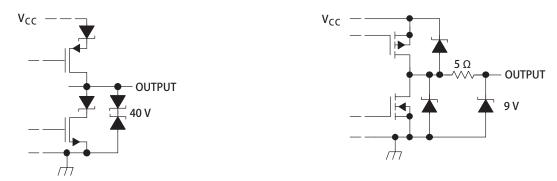
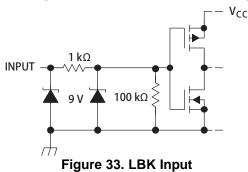


Figure 31. CANH and CANL Outputs

Figure 32. R Output





10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Diagnostic Loopback

The loopback (LBK) function of the SN65HVD233 is enabled with a high-level input to pin 5. This forces the driver into a recessive state and redirects the data (D) input at pin 1 to the received-data (R) output at pin 4. This allows the host controller to input and read back a bit sequence to perform diagnostic routines without disturbing the CAN bus. A typical CAN bus application is displayed in Figure 34.

If the LBK pin is not used, it may be tied to ground (GND). However, it is pulled low internally (defaults to a low-level input) and may be left open if not in use.

10.2 Typical Application

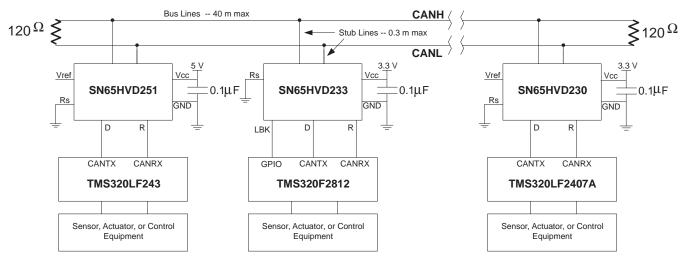


Figure 34. Typical SN65HVD233 Application

10.2.1 Design Requirements

The High-Speed ISO 11898 Standard specifications are given for a maximum signaling rate of 1 Mbps with a bus length of 40 m and a maximum of 30 nodes. It also recommends a maximum un-terminated stub length of 0.3 m. The cable is specified to be a shielded or unshielded twisted-pair with a 120-W characteristic impedance (ZO). The Standard defines a single line of twisted-pair cable with the network topology as shown in Figure 34. It is terminated at both ends with 120-W resistors, which match the characteristic impedance of the line to prevent signal reflections. According to ISO 11898, placing RL on a node should be avoided because the bus lines lose termination if the node is disconnected from the bus.



Typical Application (continued)

10.2.2 Detailed Design Procedure

1000

BUS LENGTH (m) SIGNALING RATE (Mbps)

40 1

100 0.5

200 0.25

500 0.10

0.05

Table 5. Suggested Cable Length vs Signaling Rate

Basically, the maximum bus length is determined by, or rather is a trade-off with the selected signaling rate as listed in Table 5.

A signaling rate decreases as transmission distance increases. While steady-state losses may become a factor at the longest transmission distances, the major factors limiting signaling rate as distance is increased are time varying. Cable bandwidth limitations, which degrade the signal transition time and introduce inter-symbol interference (ISI), are primary factors reducing the achievable signaling rate when transmission distance is increased.

For a CAN bus, the signaling rate is also determined from the total system delay – down and back between the two most distant nodes of a system and the sum of the delays into and out of the nodes on a bus with the typical 5ns/m prop delay of a twisted-pair cable. Also, consideration must be given the signal amplitude loss due to resistance of the cable and the input resistance of the transceivers. Under strict analysis, skin effects, proximity to other circuitry, dielectric loss, and radiation loss effects all act to influence the primary line parameters and degrade the signal.

A conservative rule of thumb for bus lengths over 100 m is derived from the product of the signaling rate in Mbps and the bus length in meters, which should be less than or equal to 50.

Signaling Rate (Mbps) × Bus Length (m) <= 50. Operation at extreme temperatures should employ additional conservatism.

10.2.2.1 Slope Control

The rise and fall slope of the SN65HVD233 driver output can be adjusted by connecting a resistor from R_s (pin 8) to ground (GND), or to a low-level input voltage (see Figure 35).

The slope of the driver output signal is proportional to the output current of the pin. This slope control is implemented with an external resistor value of 10 k Ω to achieve a \$15-V/\mus slew rate, and up to 100 k Ω to achieve a \$2.0- V/\mus slew rate (see Figure 36). Typical driver output waveforms with slope control are displayed in Figure 37.

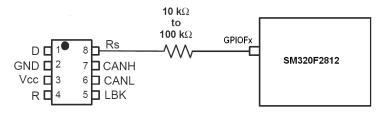


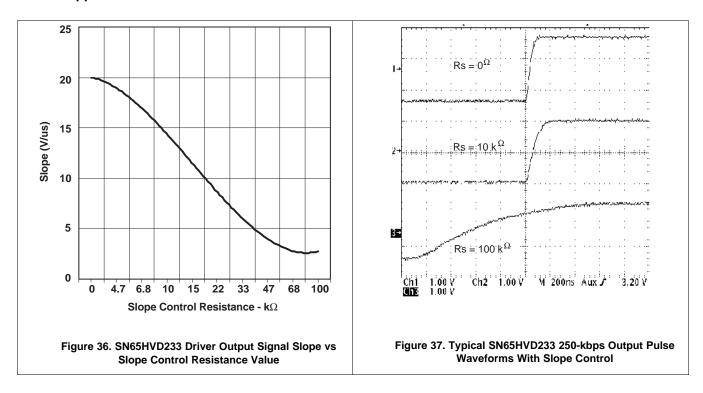
Figure 35. Slope Control/Standby Connection to DSP

10.2.2.2 Standby

If a high-level input (>0.75 V_{CC}) is applied to R_s , the circuit enters a low-current, *listen-only* standby mode, during which the driver is switched off and the receiver remains active. The local controller can reverse this low-power standby mode when the rising edge of a dominant state (bus differential voltage >900 mV typical) occurs on the bus.



10.2.3 Application Curves



11 Power Supply Recommendations

TI recommend to have localized capacitive decoupling near device VCC pin to GND. Values of 4.7 μ F at VCC pin and 10 μ F, 1 μ F, and 0.1 μ F at supply have tested well on evaluation modules.

12 Layout

12.1 Layout Guidelines

Minimize stub length from node insertion to bus.



12.2 Layout Example

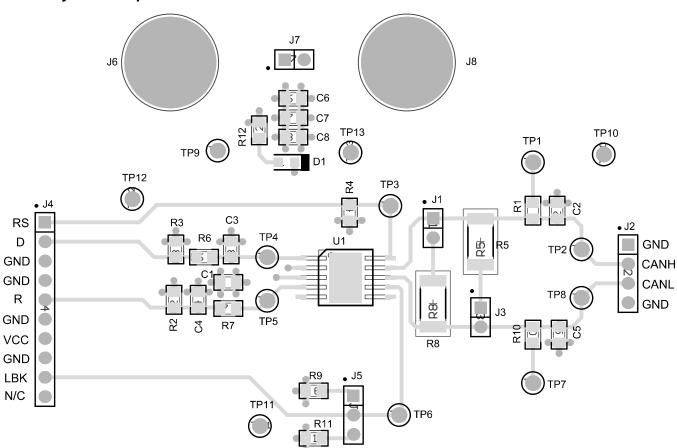




Figure 38. Layout Example



13 Device and Documentation Support

13.1 Trademarks

SDS is a trademark of Texas Instruments.

DeviceNet is a trademark of Open DeviceNet Vendor Association.

All other trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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10-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN65HVD233HD	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 175	233S
SN65HVD233HD.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 175	233S
SN65HVD233SHKJ	Active	Production	CFP (HKJ) 8	25 TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 210	SN65HVD233S HKJ
SN65HVD233SHKJ.A	Active	Production	CFP (HKJ) 8	25 TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 210	SN65HVD233S HKJ
SN65HVD233SHKQ	Active	Production	CFP (HKQ) 8	25 TUBE	Yes	AU	N/A for Pkg Type	-55 to 210	HVD233S HKQ
SN65HVD233SHKQ.A	Active	Production	CFP (HKQ) 8	25 TUBE	Yes	AU	N/A for Pkg Type	-55 to 210	HVD233S HKQ
SN65HVD233SJD	Active	Production	CDIP SB (JDJ) 8	37 TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 210	SN65HVD233SJD
SN65HVD233SJD.A	Active	Production	CDIP SB (JDJ) 8	37 TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 210	SN65HVD233SJD
SN65HVD233SKGDA	Active	Production	XCEPT (KGD) 0	130 OTHER	Yes	Call TI	N/A for Pkg Type	-55 to 210	
SN65HVD233SKGDA.A	Active	Production	XCEPT (KGD) 0	130 OTHER	Yes	Call TI	N/A for Pkg Type	-55 to 210	

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 10-Nov-2025

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65HVD233-HT:

Catalog: SN65HVD233

Automotive: SN65HVD233-Q1

Enhanced Product : SN65HVD233-EP

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 23-May-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD233HD	D	SOIC	8	75	507	8	3940	4.32
SN65HVD233HD.A	D	SOIC	8	75	507	8	3940	4.32
SN65HVD233SHKJ	HKJ	CFP	8	25	506.98	26.16	6220	NA
SN65HVD233SHKJ.A	HKJ	CFP	8	25	506.98	26.16	6220	NA
SN65HVD233SHKQ	HKQ	CFP	8	25	506.98	26.16	6220	NA
SN65HVD233SHKQ.A	HKQ	CFP	8	25	506.98	26.16	6220	NA



SMALL OUTLINE INTEGRATED CIRCUIT



- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



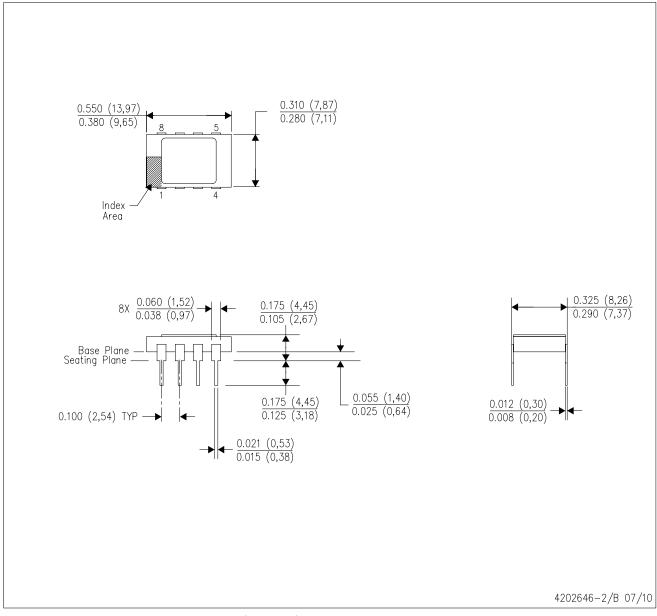
NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



JDJ (R-CDIP-T8)

CERAMIC DUAL IN-LINE PACKAGE

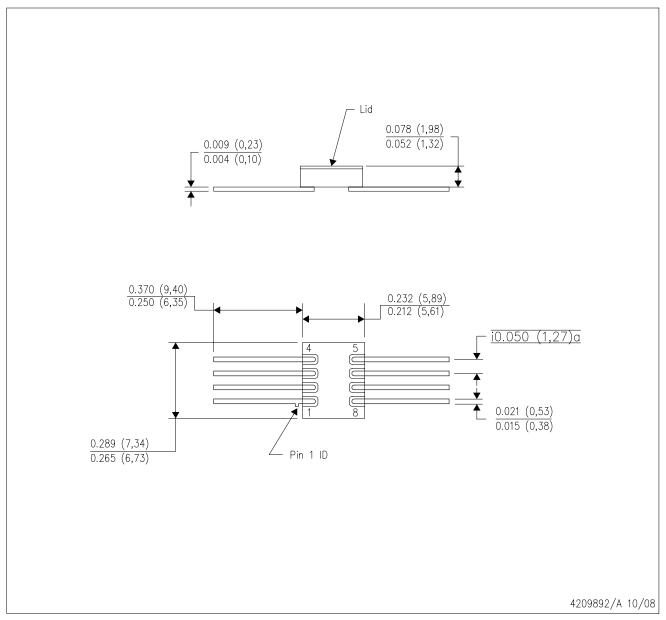


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
- D. This package is hermetically sealed with a metal lid.
- E. The leads are gold plated and can be solderdipped.
- F. Leads not shown for clarity purposes.
- G. Lid and heat sink are connected to GND leads.



HKJ (R-CDFP-F8)

CERAMIC DUAL FLATPACK

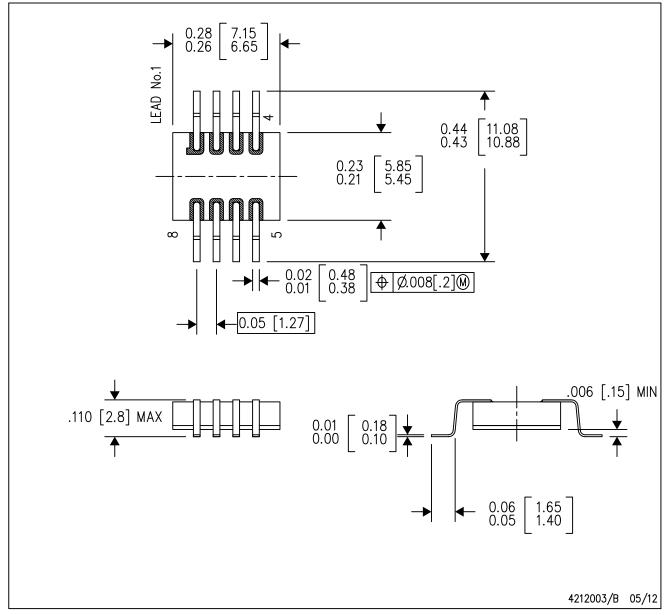


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals will be gold plated.



HKQ (R-CDFP-G8)

CERAMIC GULL WING



- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a metal lid.
- D. The terminals will be gold plated.E. Lid is not connected to any lead.



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