

## SNx5176B Differential Bus Transceivers

### 1 Features

- Bidirectional transceivers
- Meets or exceeds the requirements of ANSI standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27
- Designed for multipoint transmission on long bus lines in noisy environments
- 3-state driver and receiver outputs
- Individual driver and receiver enables
- Wide positive and negative input/output bus voltage ranges
- $\pm 60\text{mA}$  maximum driver output capability
- Thermal shutdown protection
- Driver positive and negative current limiting
- $12\text{k}\Omega$  minimum receiver input impedance
- $\pm 200\text{mV}$  receiver input sensitivity
- $50\text{mV}$  typical receiver input hysteresis
- Operates from a single  $5\text{V}$  supply

### 2 Applications

- [Chemical and gas sensors](#)
- Digital signage
- Human machine interfaces (HMI)
- [Motor controls](#)
  - AC induction
  - Brushed and brush-less DC
  - Low- and high-voltage
  - Stepper motors
  - Permanent magnets
- TETRA base stations
- Telecommunication towers
  - Remote electrical tilt (RET) units
  - Tower mounted amplifiers (TMA)
- Weigh scales
- Wireless repeaters

### 3 Description

The SN65176B and SN75176B differential bus transceivers are designed for bidirectional data communication on multipoint bus transmission lines. The SN65176B and SN75176B are designed for balanced transmission lines and meet ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27.

The SN65176B and SN75176B devices combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single  $5\text{V}$  power supply. The driver has a active-high enable and the receiver has an active-low enable, that can connect together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or  $V_{CC} = 0$ . These ports feature wide positive and negative common-mode voltage ranges, making the device appropriate for party-line applications.

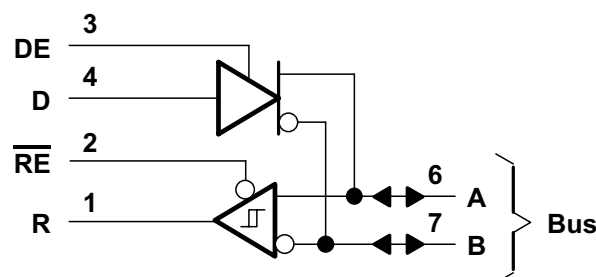
The driver is designed for up to  $60\text{mA}$  of sink or source current. The driver features positive and negative current limiting and thermal shutdown for protection from line-fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately  $150^\circ\text{C}$ . The receiver features a minimum input impedance of  $12\text{k}\Omega$ , an input sensitivity of  $\pm 200\text{mV}$ , and a typical input hysteresis of  $50\text{mV}$ .

#### Package Information

| PART NUMBER | PACKAGE (PIN) <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup>          |
|-------------|------------------------------|--------------------------------------|
| SNx5176     | D (SOIC, 8)                  | $4.90\text{mm} \times 3.91\text{mm}$ |
|             | P (PDIP, 8)                  | $9.81\text{mm} \times 6.35\text{mm}$ |
|             | PS (SOP, 8)                  | $6.20\text{mm} \times 5.30\text{mm}$ |

(1) For more information, see [Section 10](#).

(2) The package size (length  $\times$  width) is a nominal value and includes pins, where applicable.



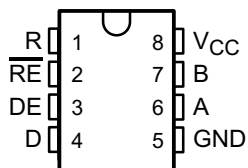
**Simplified Schematic**



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## 4 Pin Configuration and Functions



**Figure 4-1. Top View**

**Table 4-1. Pin Functions**

| PIN             |     | TYPE | DESCRIPTION                             |
|-----------------|-----|------|-----------------------------------------|
| NAME            | NO. |      |                                         |
| R               | 1   | O    | Logic data output from RS-485 Receiver  |
| $\overline{RE}$ | 2   | I    | Receive enable (active low)             |
| DE              | 3   | I    | Driver enable (active high)             |
| D               | 4   | I    | Logic data input to RS-485 driver       |
| GND             | 5   | —    | Device ground pin                       |
| A               | 6   | I/O  | RS-422 or RS-485 data line              |
| B               | 7   | I/O  | RS-422 or RS-485 data line              |
| V <sub>CC</sub> | 8   | —    | Power input, connect to 5V power source |

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                                             | MIN | MAX | UNIT |
|-------------------------------------------------------------|-----|-----|------|
| V <sub>CC</sub> Supply voltage <sup>(2)</sup>               |     | 7   | V    |
| Voltage range at any bus terminal                           | –10 | 15  | V    |
| V <sub>I</sub> Enable input voltage                         |     | 5.5 | V    |
| T <sub>J</sub> Operating virtual junction temperature       |     | 150 | °C   |
| T <sub>stg</sub> Storage temperature range                  | –65 | 150 | °C   |
| Lead temperature 1.6mm (1/16 inch) from case for 10 seconds |     | 260 | °C   |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

### 5.2 Recommended Operating Conditions

|                                                                                           | MIN           | TYP | MAX  | UNIT |
|-------------------------------------------------------------------------------------------|---------------|-----|------|------|
| V <sub>CC</sub> Supply voltage                                                            | 4.75          | 5   | 5.25 | V    |
| V <sub>I</sub> or V <sub>IC</sub> Voltage at any bus terminal (separately or common mode) | –7            |     | 12   | V    |
| V <sub>IH</sub> High-level input voltage                                                  | D, DE, and RE | 2   |      | V    |
| V <sub>IL</sub> Low-level input voltage                                                   | D, DE, and RE |     | 0.8  | V    |
| V <sub>ID</sub> Differential input voltage <sup>(1)</sup>                                 |               |     | ±12  | V    |
| I <sub>OH</sub> High-level output current                                                 | Driver        |     | –60  | mA   |
|                                                                                           | Receiver      |     | –400 | µA   |
| I <sub>OL</sub> Low-level output current                                                  | Driver        |     | 60   | mA   |
|                                                                                           | Receiver      |     | 8    | mA   |
| T <sub>A</sub> Operating free-air temperature                                             | SN65176B      | –40 | 105  | °C   |
|                                                                                           | SN75176B      | 0   | 70   |      |

- (1) Differential input/output bus voltage is measured at the non-inverting terminal A, with respect to the inverting terminal B.

### 5.3 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | SNx5176  |         |          | UNIT |
|-------------------------------|----------------------------------------------|----------|---------|----------|------|
|                               |                                              | D (SOIC) | PS (SO) | P (PDIP) |      |
|                               |                                              | 8 PINS   |         |          |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 114.4    | 113.2   | 88.1     | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 55.1     | 57.9    | 65.9     | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 61.6     | 69.0    | 69.0     | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 8.8      | 14.6    | 35.2     | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 60.8     | 68.1    | 64.3     | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics application note](#).

## 5.4 Electrical Characteristics – Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER         |                                                                   | TEST CONDITIONS <sup>(1)</sup>               | MIN                                    | TYP <sup>(2)</sup> | MAX             | UNIT |
|-------------------|-------------------------------------------------------------------|----------------------------------------------|----------------------------------------|--------------------|-----------------|------|
| V <sub>IK</sub>   | Input clamp voltage                                               | I <sub>I</sub> = –18mA                       |                                        |                    | –1.5            | V    |
| V <sub>O</sub>    | Output voltage                                                    | I <sub>O</sub> = 0                           | 0                                      |                    | V <sub>CC</sub> | V    |
| V <sub>OD1</sub>  | Differential output voltage                                       | I <sub>O</sub> = 0                           | 1.5                                    | 3.6                | V <sub>CC</sub> | V    |
| V <sub>OD2</sub>  | Differential output voltage                                       | R <sub>L</sub> = 100Ω, see Figure 6-1        | ½ V <sub>OD1</sub> or 2 <sup>(3)</sup> |                    |                 | V    |
|                   |                                                                   | R <sub>L</sub> = 54Ω, see Figure 6-1         | 1.5                                    | 2.5                | 5               |      |
| V <sub>OD3</sub>  | Differential output voltage                                       | See <sup>(4)</sup>                           | 1.5                                    |                    | 5               | V    |
| Δ V <sub>OD</sub> | Change in magnitude of differential output voltage <sup>(5)</sup> | R <sub>L</sub> = 54Ω or 100Ω, see Figure 6-1 |                                        |                    | ±0.2            | V    |
| V <sub>OC</sub>   | Common-mode output voltage                                        | R <sub>L</sub> = 54Ω or 100Ω, see Figure 6-1 | –1                                     |                    | +3              | V    |
| Δ V <sub>OC</sub> | Change in magnitude of common-mode output voltage <sup>(5)</sup>  | R <sub>L</sub> = 54Ω or 100Ω, see Figure 6-1 |                                        |                    | ±0.2            | V    |
| I <sub>O</sub>    | Output current                                                    | Output disabled <sup>(6)</sup>               | V <sub>O</sub> = 12V                   |                    | 1               | mA   |
|                   |                                                                   |                                              | V <sub>O</sub> = –7V                   |                    | –0.8            |      |
| I <sub>IH</sub>   | High-level input current                                          | V <sub>I</sub> = 2.4V                        |                                        |                    | 20              | μA   |
| I <sub>IL</sub>   | Low-level input current                                           | V <sub>I</sub> = 0.4V                        |                                        |                    | –400            | μA   |
| I <sub>OS</sub>   | Short-circuit output current                                      |                                              | V <sub>O</sub> = –7V                   |                    | –250            | mA   |
|                   |                                                                   |                                              | V <sub>O</sub> = 0                     |                    | –150            |      |
|                   |                                                                   |                                              | V <sub>O</sub> = V <sub>CC</sub>       |                    | 250             |      |
|                   |                                                                   |                                              | V <sub>O</sub> = 12V                   |                    | 250             |      |
| I <sub>CC</sub>   | Supply current (total package)                                    | No load                                      | Outputs enabled                        |                    | 42              | mA   |
|                   |                                                                   |                                              | Outputs disabled                       |                    | 26              |      |
|                   |                                                                   |                                              |                                        |                    | 35              |      |

- (1) The power-off measurement in ANSI Standard TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
- (2) All typical values are at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C.
- (3) The minimum V<sub>OD2</sub> with a 100Ω load is either ½ V<sub>OD1</sub> or 2V, whichever is greater.
- (4) See ANSI Standard TIA/EIA-485-A, Figure 3.5, Test Termination Measurement 2.
- (5) Δ|V<sub>OD</sub>| and Δ|V<sub>OC</sub>| are the changes in magnitude of V<sub>OD</sub> and V<sub>OC</sub>, respectively, that occur when the input is changed from a high level to a low level.
- (6) This applies for both power on and off; refer to ANSI Standard TIA/EIA-485-A the for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

## 5.5 Electrical Characteristics – Receiver

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| PARAMETER        |                                                                 | TEST CONDITIONS                                                   | MIN                 | TYP <sup>(1)</sup>   | MAX  | UNIT |
|------------------|-----------------------------------------------------------------|-------------------------------------------------------------------|---------------------|----------------------|------|------|
| V <sub>IT+</sub> | Positive-going input threshold voltage                          | V <sub>O</sub> = 2.7V, I <sub>O</sub> = –0.4mA                    |                     |                      | 0.2  | V    |
| V <sub>IT–</sub> | Negative-going input threshold voltage                          | V <sub>O</sub> = 0.5V, I <sub>O</sub> = 8mA                       | –0.2 <sup>(2)</sup> |                      |      | V    |
| V <sub>hys</sub> | Input hysteresis voltage (V <sub>IT+</sub> – V <sub>IT–</sub> ) |                                                                   |                     | 50                   |      | mV   |
| V <sub>IK</sub>  | Enable Input clamp voltage                                      | I <sub>I</sub> = –18mA                                            |                     |                      | –1.5 | V    |
| V <sub>OH</sub>  | High-level output voltage                                       | V <sub>ID</sub> = 200mV, I <sub>OH</sub> = –400μA, see Figure 6-2 | 2.7                 |                      |      | V    |
| V <sub>OL</sub>  | Low-level output voltage                                        | V <sub>ID</sub> = –200mV, I <sub>OL</sub> = 8mA, see Figure 6-2   |                     |                      | 0.45 | V    |
| I <sub>OZ</sub>  | High-impedance-state output current                             | V <sub>O</sub> = 0.4V to 2.4V                                     |                     |                      | ±20  | μA   |
| I <sub>I</sub>   | Line input current                                              | Other input = 0V <sup>(3)</sup>                                   |                     | V <sub>I</sub> = 12V | 1    | mA   |
|                  |                                                                 |                                                                   |                     | V <sub>I</sub> = –7V | –0.8 |      |
| I <sub>IH</sub>  | High-level enable input current                                 | V <sub>IH</sub> = 2.7V                                            |                     |                      | 20   | μA   |
| I <sub>IL</sub>  | Low-level enable input current                                  | V <sub>IL</sub> = 0.4V                                            |                     |                      | –100 | μA   |
| r <sub>I</sub>   | Input resistance                                                | V <sub>I</sub> = 12V                                              | 12                  |                      |      | kΩ   |
| I <sub>OS</sub>  | Short-circuit output current                                    |                                                                   | –15                 |                      | –85  | mA   |
| I <sub>CC</sub>  | Supply current (total package)                                  | No load                                                           |                     | Outputs enabled      | 42   | mA   |
|                  |                                                                 |                                                                   |                     | Outputs disabled     | 26   |      |

(1) All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

(3) This applies for both power on and power off. Refer to EIA Standard TIA/EIA-485-A for exact conditions.

## 5.6 Switching Characteristics – Driver

V<sub>CC</sub> = 5V, R<sub>L</sub> = 110Ω, T<sub>A</sub> = 25°C (unless otherwise noted)

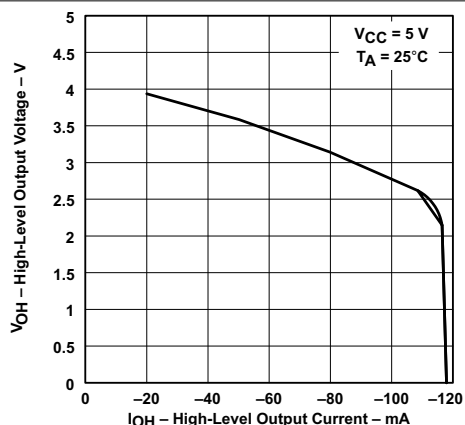
| PARAMETER          |                                     | TEST CONDITIONS                      | MIN | TYP | MAX | UNIT |
|--------------------|-------------------------------------|--------------------------------------|-----|-----|-----|------|
| t <sub>d(OD)</sub> | Differential-output delay time      | R <sub>L</sub> = 54Ω, see Figure 6-3 |     | 15  | 22  | ns   |
| t <sub>t(OD)</sub> | Differential-output transition time | R <sub>L</sub> = 54Ω, see Figure 6-3 |     | 20  | 30  | ns   |
| t <sub>PZH</sub>   | Output enable time to high level    | See Figure 6-4                       |     | 85  | 120 | ns   |
| t <sub>PZL</sub>   | Output enable time to low level     | See Figure 6-5                       |     | 40  | 60  | ns   |
| t <sub>PHZ</sub>   | Output disable time from high level | See Figure 6-4                       |     | 150 | 250 | ns   |
| t <sub>PLZ</sub>   | Output disable time from low level  | See Figure 6-5                       |     | 20  | 30  | ns   |

## 5.7 Switching Characteristics – Receiver

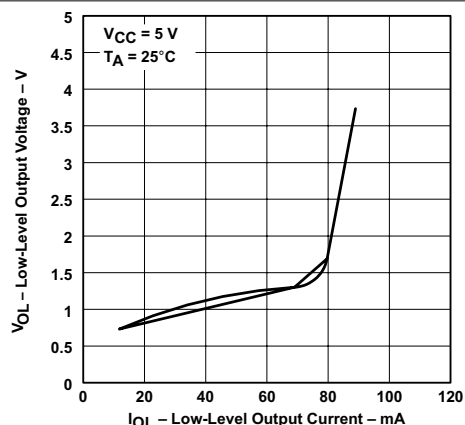
V<sub>CC</sub> = 5V, C<sub>L</sub> = 15pF, T<sub>A</sub> = 25°C

| PARAMETER        |                                                   | TEST CONDITIONS                           | MIN | TYP | MAX | UNIT |
|------------------|---------------------------------------------------|-------------------------------------------|-----|-----|-----|------|
| t <sub>PLH</sub> | Propagation delay time, low- to high-level output | V <sub>ID</sub> = 0 to 3V, see Figure 6-6 |     | 21  | 35  | ns   |
| t <sub>PHL</sub> | Propagation delay time, high- to low-level output |                                           |     | 23  | 35  |      |
| t <sub>PZH</sub> | Output enable time to high level                  | See Figure 6-7                            |     | 10  | 20  | ns   |
| t <sub>PZL</sub> | Output enable time to low level                   |                                           |     | 12  | 20  |      |
| t <sub>PHZ</sub> | Output disable time from high level               | See Figure 6-7                            |     | 20  | 35  | ns   |
| t <sub>PLZ</sub> | Output disable time from low level                |                                           |     | 17  | 25  |      |

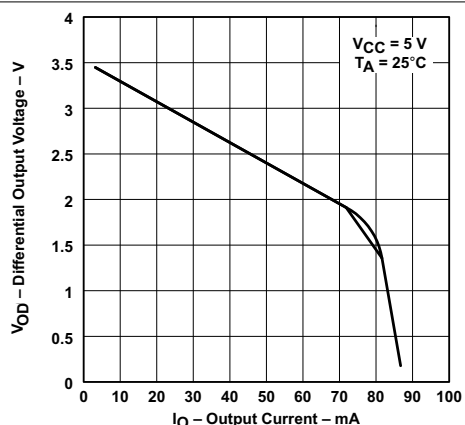
## 5.8 Typical Characteristics



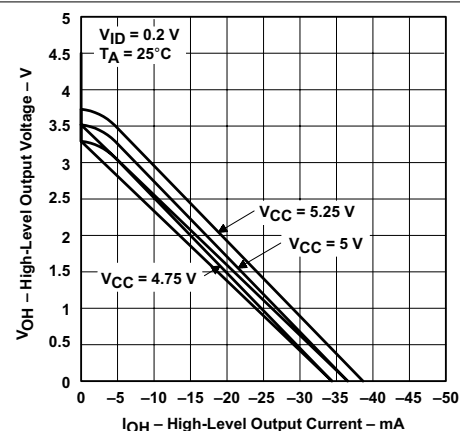
**Figure 5-1. Driver High-Level Output Voltage vs High-Level Output Current**



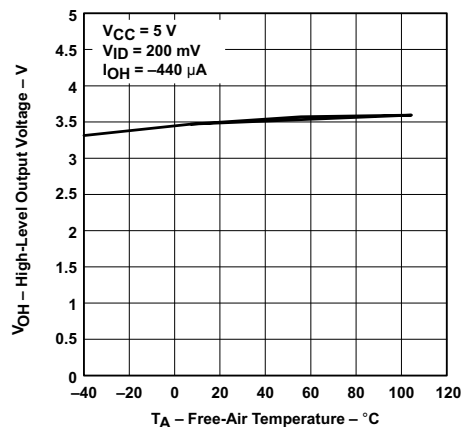
**Figure 5-2. Driver Low-Level Output Voltage vs Low-Level Output Current**



**Figure 5-3. Driver Differential Output Voltage vs Output Current**

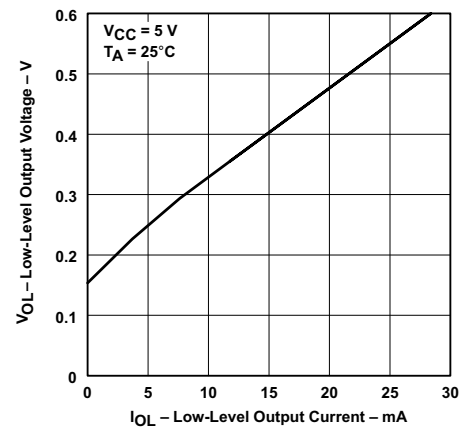


**Figure 5-4. Receiver High-Level Output Voltage vs High-Level Output Current**



Only the 0°C to 70°C portion of the curve applies to the SN75176B device.

**Figure 5-5. Receiver High-Level Output Voltage vs Free-Air Temperature**



**Figure 5-6. Receiver Low-Level Output Voltage vs Low-Level Output Current**

## 5.8 Typical Characteristics (continued)

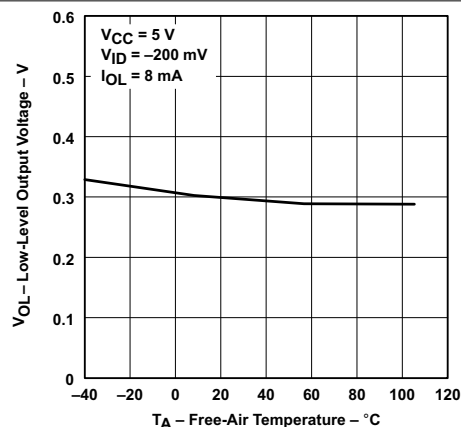


Figure 5-7. Receiver Low-Level Output Voltage vs Free-Air Temperature

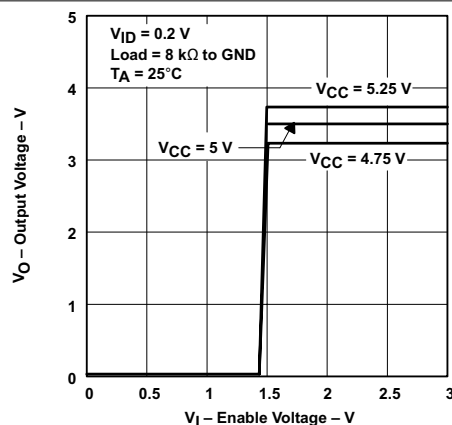


Figure 5-8. Receiver Output Voltage vs Enable Voltage

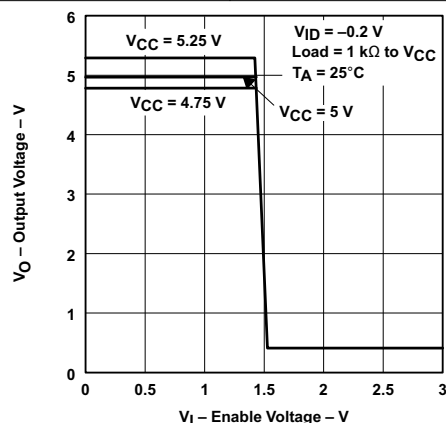


Figure 5-9. Receiver Output Voltage vs Enable Voltage



## Parameter Measurement Information

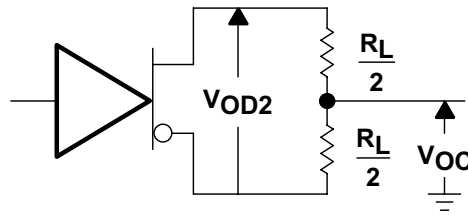


Figure 6-1. Driver  $V_{OD}$  and  $V_{OC}$

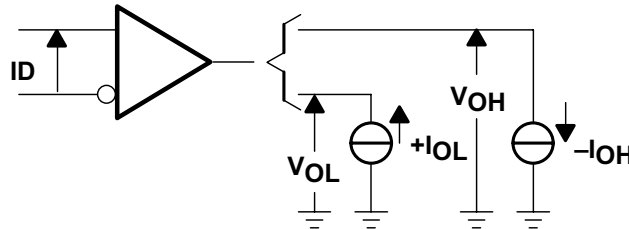
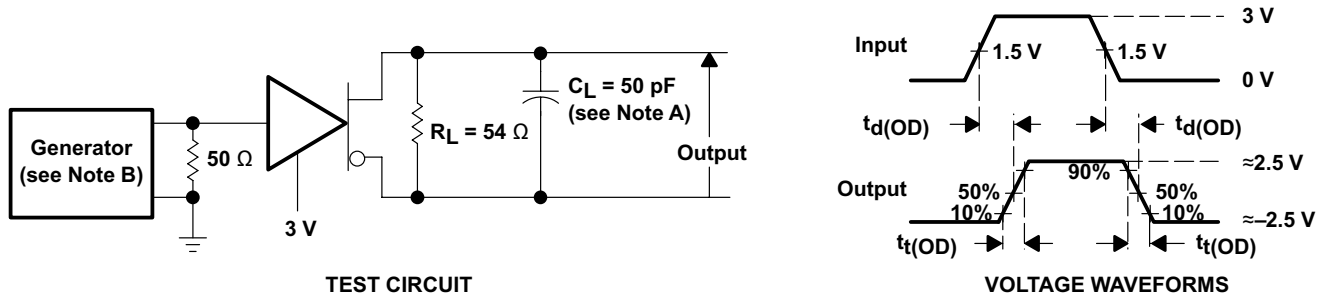
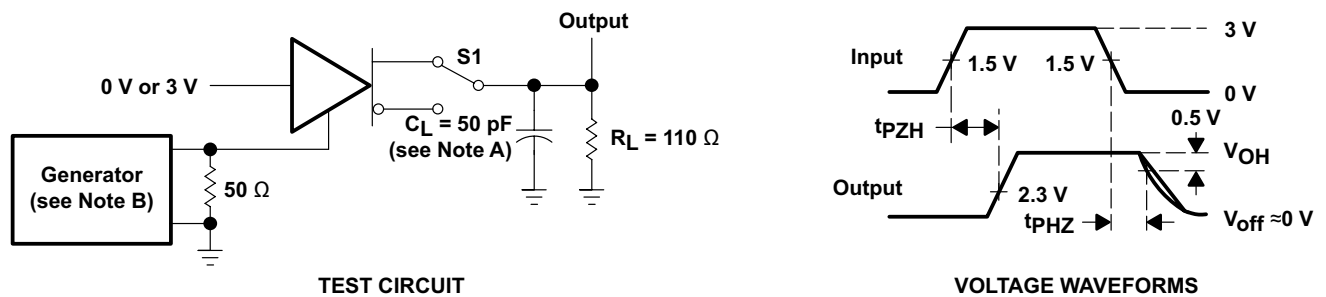


Figure 6-2. Receiver  $V_{OH}$  and  $V_{OL}$



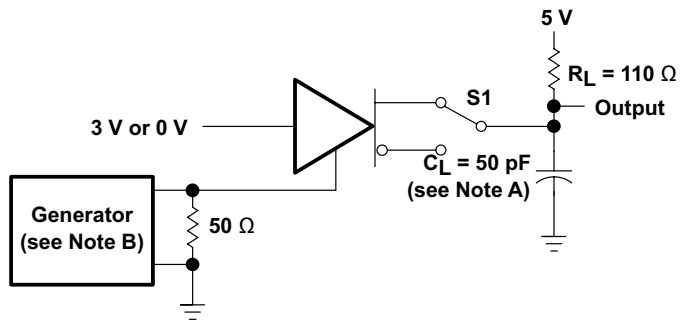
- A.  $C_L$  includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq 1\text{MHz}$ , 50% duty cycle,  $t_r \leq 6\text{ns}$ ,  $t_f \leq 6\text{ns}$ ,  $Z_O = 50\Omega$ .

Figure 6-3. Driver Test Circuit and Voltage Waveforms

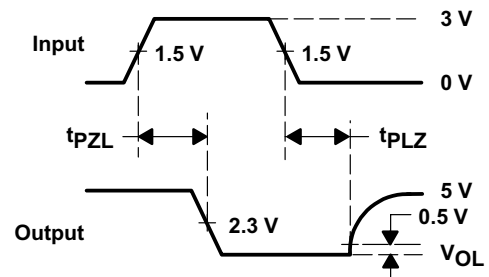


- A.  $C_L$  includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq 1\text{MHz}$ , 50% duty cycle,  $t_r \leq 6\text{ns}$ ,  $t_f \leq 6\text{ns}$ ,  $Z_O = 50\Omega$ .

Figure 6-4. Driver Test Circuit and Voltage Waveforms



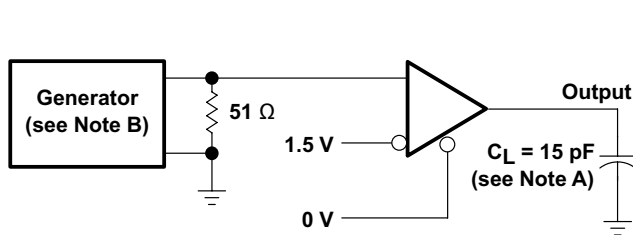
TEST CIRCUIT



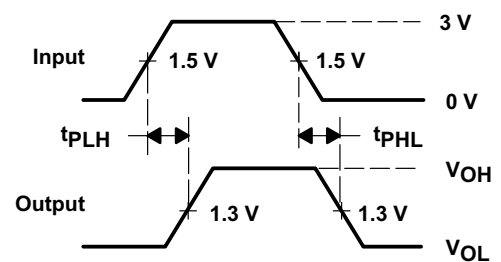
VOLTAGE WAVEFORMS

- A.  $C_L$  includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1\text{MHz}$ , 50% duty cycle,  $t_r \leq 6\text{ns}$ ,  $t_f \leq 6\text{ns}$ ,  $Z_O = 50\Omega$ .

Figure 6-5. Driver Test Circuit and Voltage Waveforms



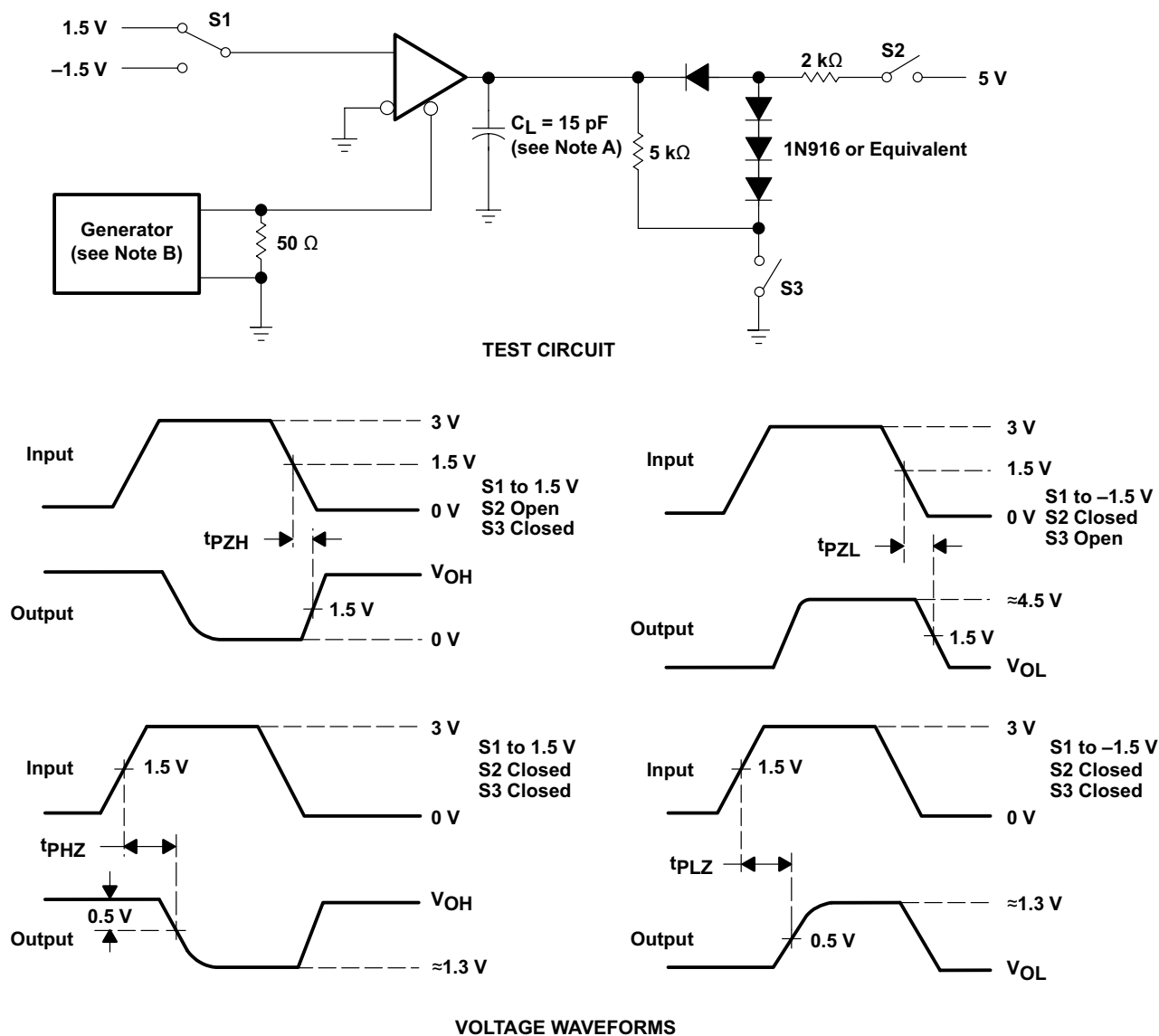
TEST CIRCUIT



VOLTAGE WAVEFORMS

- A.  $C_L$  includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1\text{MHz}$ , 50% duty cycle,  $t_r \leq 6\text{ns}$ ,  $t_f \leq 6\text{ns}$ ,  $Z_O = 50\Omega$ .

Figure 6-6. Receiver Test Circuit and Voltage Waveforms



- A.  $C_L$  includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1\text{MHz}$ , 50% duty cycle,  $t_r \leq 6\text{ns}$ ,  $t_f \leq 6\text{ns}$ ,  $Z_O = 50\Omega$ .

**Figure 6-7. Receiver Test Circuit and Voltage Waveforms**

## 6 Detailed Description

### 6.1 Overview

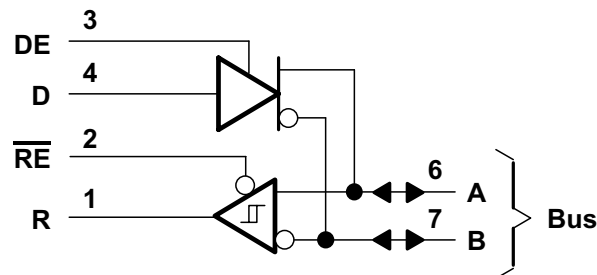
The SN65176B and SN75176B differential bus transceivers are integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27.

The SN65176B and SN75176B devices combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or  $V_{CC} = 0$ . These ports feature wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The driver is designed for up to 60 mA of sink or source current. The driver features positive and negative current limiting and thermal shutdown for protection from line-fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 k $\Omega$ , an input sensitivity of  $\pm 200$  mV, and a typical input hysteresis of 50 mV.

The SN65176B and SN75176B devices can be used in transmission-line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

### 6.2 Functional Block Diagram



### 6.3 Feature Description

#### 6.3.1 Driver

The driver converts a TTL logic signal level to RS-422 and RS-485 compliant differential output. Use the TTL logic input, the DE pin, to turn the driver on and off.

**Table 6-1. Driver Function** <sup>(1)</sup>

| INPUT D | ENABLE DE | DIFFERENTIAL OUTPUTS |   |
|---------|-----------|----------------------|---|
|         |           | A                    | B |
| H       | H         | H                    | L |
| L       | H         | L                    | H |
| X       | L         | Z                    | Z |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

### 6.3.2 Receiver

The receiver converts a RS-422 or RS-485 differential input voltage to a TTL logic level output. Use the TTL logic input, the  $\overline{RE}$  pin, to turn the receiver logic output on and off.

**Table 6-2. Receiver Function Table <sup>(1)</sup>**

| DIFFERENTIAL INPUTS A–B | ENABLE $\overline{RE}$ | OUTPUT R |
|-------------------------|------------------------|----------|
| $V_{ID} \geq 0.2V$      | L                      | H        |
| $-0.2V < V_{ID} < 0.2V$ | L                      | U        |
| $V_{ID} \leq -0.2V$     | L                      | L        |
| X                       | H                      | Z        |
| Open                    | L                      | U        |

(1) H = high level, L = low level, U = unknown, Z = high impedance (off)

## 6.4 Device Functional Modes

### 6.4.1 Device Powered

Both the driver and receiver can be individually enabled or disabled in any combination. DE and  $\overline{RE}$  can be connected together for a single port direction control bit.

### 6.4.2 Device Unpowered

The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports. The bus ports are designed to offer minimum loading to the bus when the driver is disabled or  $V_{CC} = 0$ .

### 6.4.3 Symbol Cross Reference

**Table 6-3. Symbol Equivalents**

| DATA SHEET PARAMETER | TIA/EIA-422-B                  | TIA/EIA-485-A                          |
|----------------------|--------------------------------|----------------------------------------|
| $V_O$                | $V_{oa}, V_{ob}$               | $V_{oa}, V_{ob}$                       |
| $ V_{OD1} $          | $V_o$                          | $V_o$                                  |
| $ V_{OD2} $          | $V_t @ L = 100\Omega$          | $V_t @ L = 54\Omega$                   |
| $ V_{OD3} $          |                                | $V_t$ (test termination measurement 2) |
| $\Delta V_{OD} $     | $  V_t  -  \overline{V}_t  $   | $  V_t  -  \overline{V}_t  $           |
| $V_{OC}$             | $ V_{os} $                     | $ V_{os} $                             |
| $\Delta V_{OC} $     | $ V_{os} - \overline{V}_{os} $ | $ V_{os} - \overline{V}_{os} $         |
| $I_{OS}$             | $ I_{sa} ,  I_{sb} $           |                                        |
| $I_O$                | $ I_{xa} ,  I_{xb} $           | $I_{ia}, I_{ib}$                       |

## 7 Application and Implementation

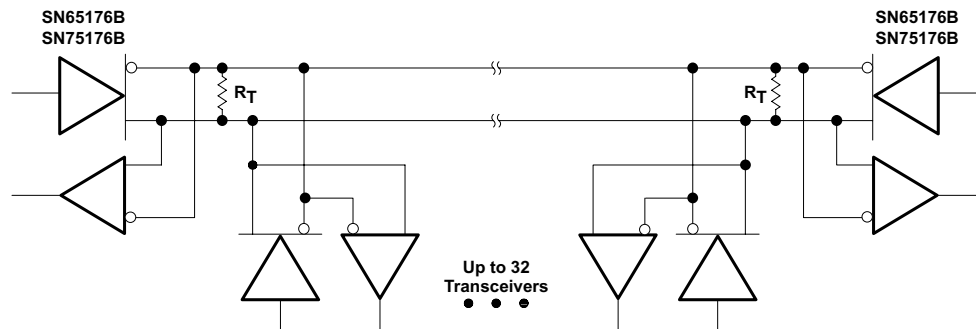
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Application Information

Use SN65176B and SN75176B in RS-485 and RS-422 physical layer communications.

### 7.2 Typical Application



Terminate the line at both ends in its characteristic impedance ( $R_T = Z_0$ ). Keep the stub lengths off of the main line as short as possible.

**Figure 7-1. Typical RS-485 Application Circuit**

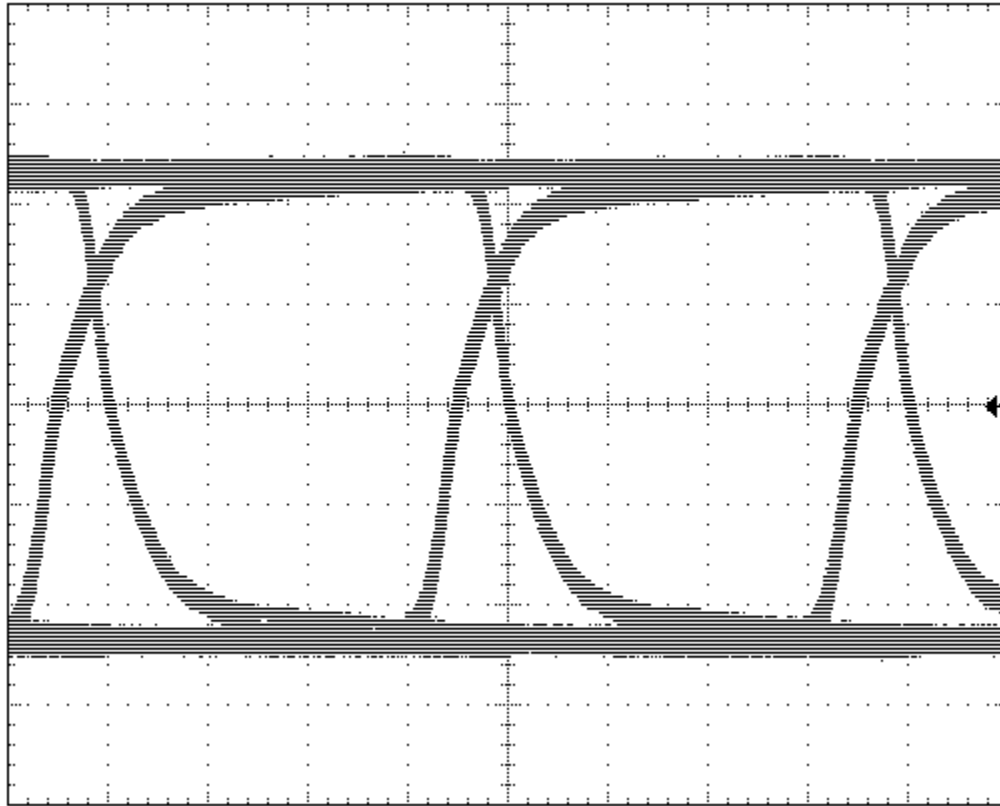
#### 7.2.1 Design Requirements

- 5V power source
- RS-485 bus operating at 10Mbps or less
- Connector that establishes the correct polarity for port pins
- External fail safe implementation

#### 7.2.2 Detailed Design Procedure

Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line. If desired, add external fail-safe biasing to establish +200mV on the A-B port.

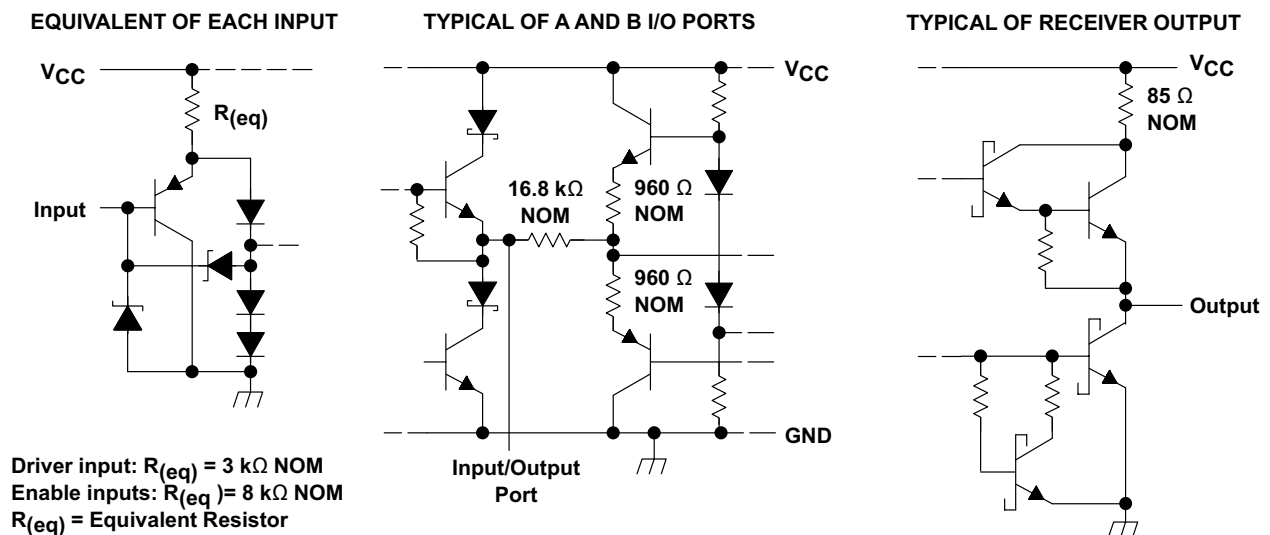
### 7.2.3 Application Curves



**Figure 7-2. Eye Diagram for 10Mbps/s Over 100 feet of Standard CAT-5E Cable 120Ω Termination at Both Ends**

In [Figure 7-2](#), the scale is 1V per division and 25ns per division.

### 7.3 System Examples



**Figure 7-3. Schematics of Inputs and Outputs**

## 7.4 Power Supply Recommendations

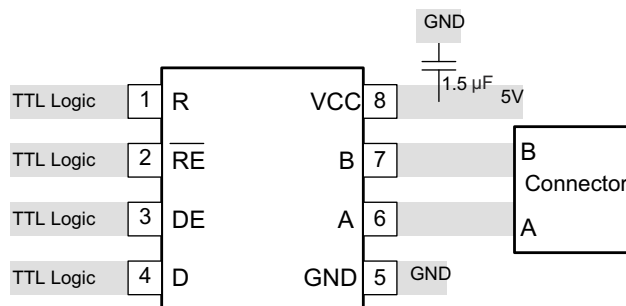
Establish a power supply of 5V with a tolerance less than 10%.

## 7.5 Layout

### 7.5.1 Layout Guidelines

Traces from device pins A and B to connector must be short and capable of 250 mA maximum current.

### 7.5.2 Layout Example



**Figure 7-4. Layout Diagram**



## 8 Device and Documentation Support

### 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

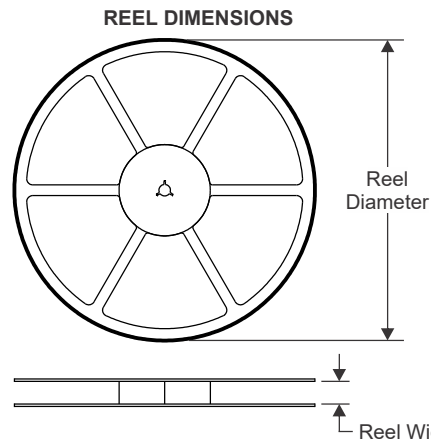
| <b>Changes from Revision H (December 2021) to Revision I (August 2025)</b> | <b>Page</b> |
|----------------------------------------------------------------------------|-------------|
| • Added a 3-row tape and reel option for the SN65176BDE orderable.....     | <b>18</b>   |

| <b>Changes from Revision G (July 2021) to Revision H (December 2021)</b>                              | <b>Page</b> |
|-------------------------------------------------------------------------------------------------------|-------------|
| • Changed $\psi_{JT}$ From 78.8 to 8.8 for the D package in the <i>Thermal Information</i> table..... | <b>4</b>    |

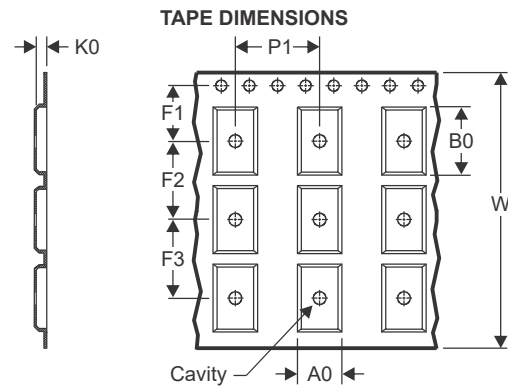
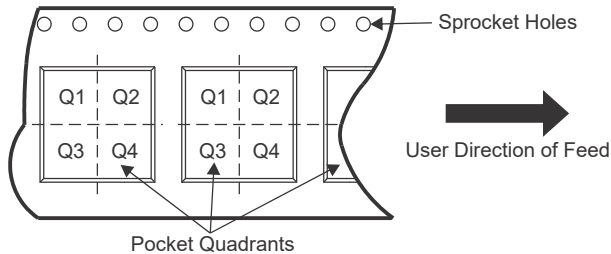
## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 10.1 Tape and Reel Information



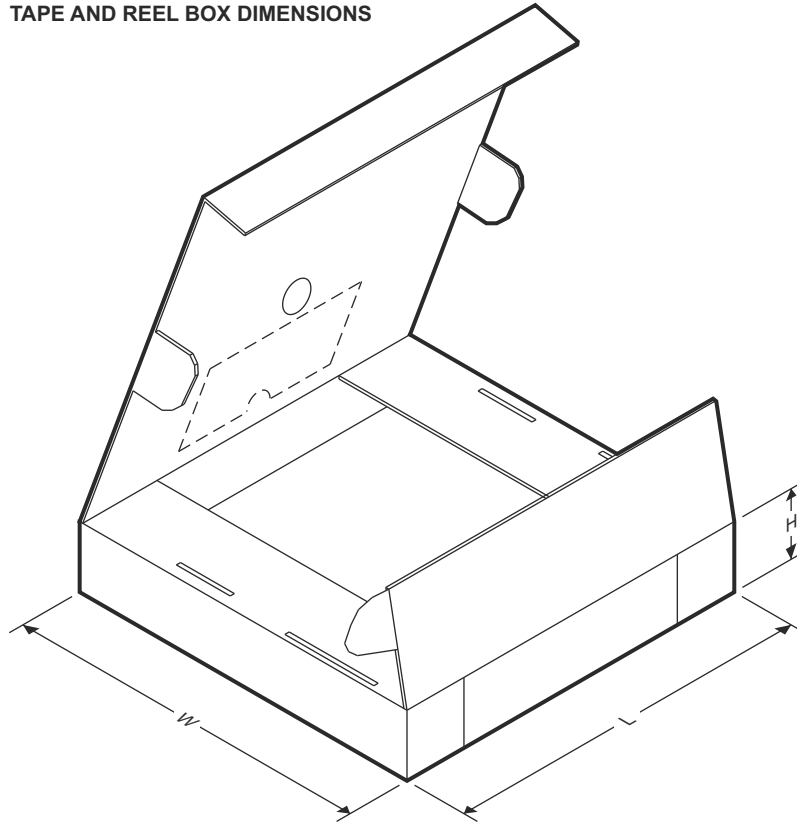
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



|    |                                                                |
|----|----------------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width          |
| B0 | Dimension designed to accommodate the component length         |
| K0 | Dimension designed to accommodate the component thickness      |
| W  | Overall width of the carrier tape                              |
| P1 | Pitch between successive cavity centers                        |
| F1 | Distance between centers of sprocket hole and first cavity row |
| F2 | Distance between centers of first and second cavity rows       |
| F3 | Distance between centers of second and third cavity rows       |

| Device       | Package Type | Package Drawing | Pins | SPQ  | Carrier       | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant | F1 (mm) | F2 (mm) | F3 (mm) |
|--------------|--------------|-----------------|------|------|---------------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|---------|---------|---------|
| SN65176BDR   | SOIC         | D               | 8    | 2500 | Single row    | 330                | 12.4               | 6.4     | 5.2     | 2.1     | 8       | 12     | Q1            | —       | —       | —       |
| SN65176BDR   | SOIC         | D               | 8    | 2500 | Single row    | 330                | 12.4               | 6.4     | 5.2     | 2.1     | 8       | 12     | Q1            | —       | —       | —       |
| SN65176BDR   | SOIC         | D               | 8    | 2500 | Single row    | 330                | 12.4               | 6.4     | 5.2     | 2.1     | 8       | 12     | Q1            | —       | —       | —       |
| SN65176BDRG4 | SOIC         | D               | 8    | 2500 | Single row    | 330                | 12.4               | 6.4     | 5.2     | 2.1     | 8       | 12     | Q1            | —       | —       | —       |
| SN65176BDRG4 | SOIC         | D               | 8    | 2500 | Single row    | 330                | 12.4               | 6.4     | 5.2     | 2.1     | 8       | 12     | Q1            | —       | —       | —       |
| SN75176BDR   | SOIC         | D               | 8    | 2500 | Single row    | 330                | 12.4               | 6.4     | 5.2     | 2.1     | 8       | 12     | Q1            | —       | —       | —       |
| SN75176BDR   | SOIC         | D               | 8    | 2500 | Single row    | 330                | 12.4               | 6.4     | 5.2     | 2.1     | 8       | 12     | Q1            | —       | —       | —       |
| SN75176BDR   | SOIC         | D               | 8    | 2500 | Single row    | 330                | 12.4               | 6.4     | 5.2     | 2.1     | 8       | 12     | Q1            | —       | —       | —       |
| SN75176BDRG4 | SOIC         | D               | 8    | 2500 | Single row    | 330                | 12.4               | 6.4     | 5.2     | 2.1     | 8       | 12     | Q1            | —       | —       | —       |
| SN75176BPSR  | SO           | PS              | 8    | 2000 | Single row    | 330                | 16.4               | 8.35    | 6.6     | 2.4     | 12      | 16     | Q1            | —       | —       | —       |
| SN65176BDE   | SOIC         | D               | 8    | 7500 | Multi-row (3) | 330                | 24.4               | 6.45    | 5.25    | 2.1     | 8       | 24     | Q1            | 5.25    | 6.25    | 6.25    |

**TAPE AND REEL BOX DIMENSIONS**



| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65176BDR   | SOIC         | D               | 8    | 2500 | 353         | 353        | 32          |
| SN65176BDR   | SOIC         | D               | 8    | 2500 | 353         | 353        | 32          |
| SN65176BDR   | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| SN65176BDRG4 | SOIC         | D               | 8    | 2500 | 340.5       | 336.1      | 25          |
| SN65176BDRG4 | SOIC         | D               | 8    | 2500 | 353         | 353        | 32          |
| SN75176BDR   | SOIC         | D               | 8    | 2500 | 353         | 353        | 32          |
| SN75176BDR   | SOIC         | D               | 8    | 2500 | 353         | 353        | 32          |
| SN75176BDR   | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| SN75176BDRG4 | SOIC         | D               | 8    | 2500 | 340.5       | 336.1      | 25          |
| SN75176BPSR  | SO           | PS              | 8    | 2000 | 353         | 353        | 32          |
| SN65176BDE   | SOIC         | D               | 8    | 7500 | 356.0       | 356.0      | 45.0        |

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN65176BD</a>    | Obsolete      | Production           | SOIC (D)   8   | -                     | -           | Call TI                              | Call TI                           | -40 to 105   | 65176B              |
| <a href="#">SN65176BDE</a>   | Active        | Production           | SOIC (D)   8   | 7500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65176B              |
| <a href="#">SN65176BDR</a>   | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65176B              |
| SN65176BDR.A                 | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65176B              |
| SN65176BDRE4                 | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65176B              |
| <a href="#">SN65176BDRG4</a> | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65176B              |
| SN65176BDRG4.A               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65176B              |
| <a href="#">SN65176BP</a>    | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 105   | SN65176BP           |
| SN65176BP.A                  | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 105   | SN65176BP           |
| <a href="#">SN75176BD</a>    | Obsolete      | Production           | SOIC (D)   8   | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | 75176B              |
| SN75176BDG4                  | NRND          | Production           | null (null)    | 75   TUBE             | -           | Call TI                              | Call TI                           | 0 to 70      |                     |
| <a href="#">SN75176BDR</a>   | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 75176B              |
| SN75176BDR.A                 | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 75176B              |
| SN75176BDRE4                 | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 75176B              |
| <a href="#">SN75176BDRG4</a> | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 75176B              |
| SN75176BDRG4.A               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 75176B              |
| <a href="#">SN75176BP</a>    | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | SN75176BP           |
| SN75176BP.A                  | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | SN75176BP           |
| SN75176BP.E4                 | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | SN75176BP           |
| <a href="#">SN75176BPSR</a>  | Active        | Production           | SO (PS)   8    | 2000   LARGE T&R      | Yes         | NIPDAU   NIPDAU                      | Level-1-260C-UNLIM                | 0 to 70      | A176B               |
| SN75176BPSR.A                | Active        | Production           | SO (PS)   8    | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | A176B               |
| SN75176BPSRG4                | Active        | Production           | SO (PS)   8    | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | A176B               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

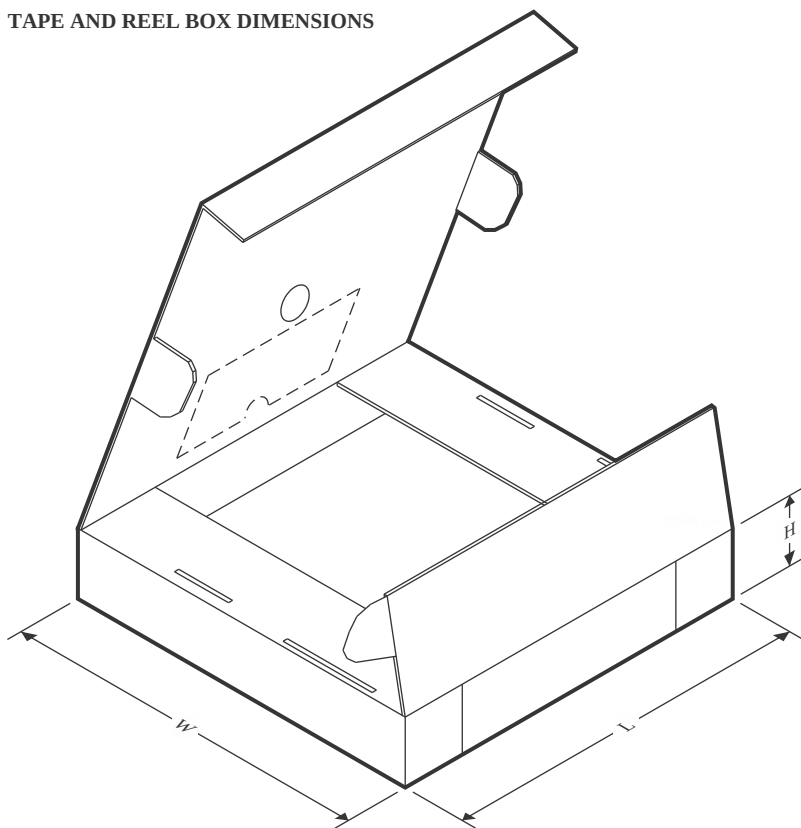
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65176BDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN65176BDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN65176BDRG4 | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN75176BDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN75176BDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN75176BDRG4 | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN75176BPSR  | SO           | PS              | 8    | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65176BDR   | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| SN65176BDR   | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| SN65176BDRG4 | SOIC         | D               | 8    | 2500 | 340.5       | 336.1      | 25.0        |
| SN75176BDR   | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| SN75176BDR   | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| SN75176BDRG4 | SOIC         | D               | 8    | 2500 | 340.5       | 336.1      | 25.0        |
| SN75176BPSR  | SO           | PS              | 8    | 2000 | 353.0       | 353.0      | 32.0        |

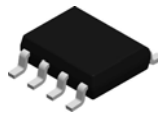
## TUBE



\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN65176BP   | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| SN65176BP.A | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| SN75176BP   | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| SN75176BP.A | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| SN75176BPE4 | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |



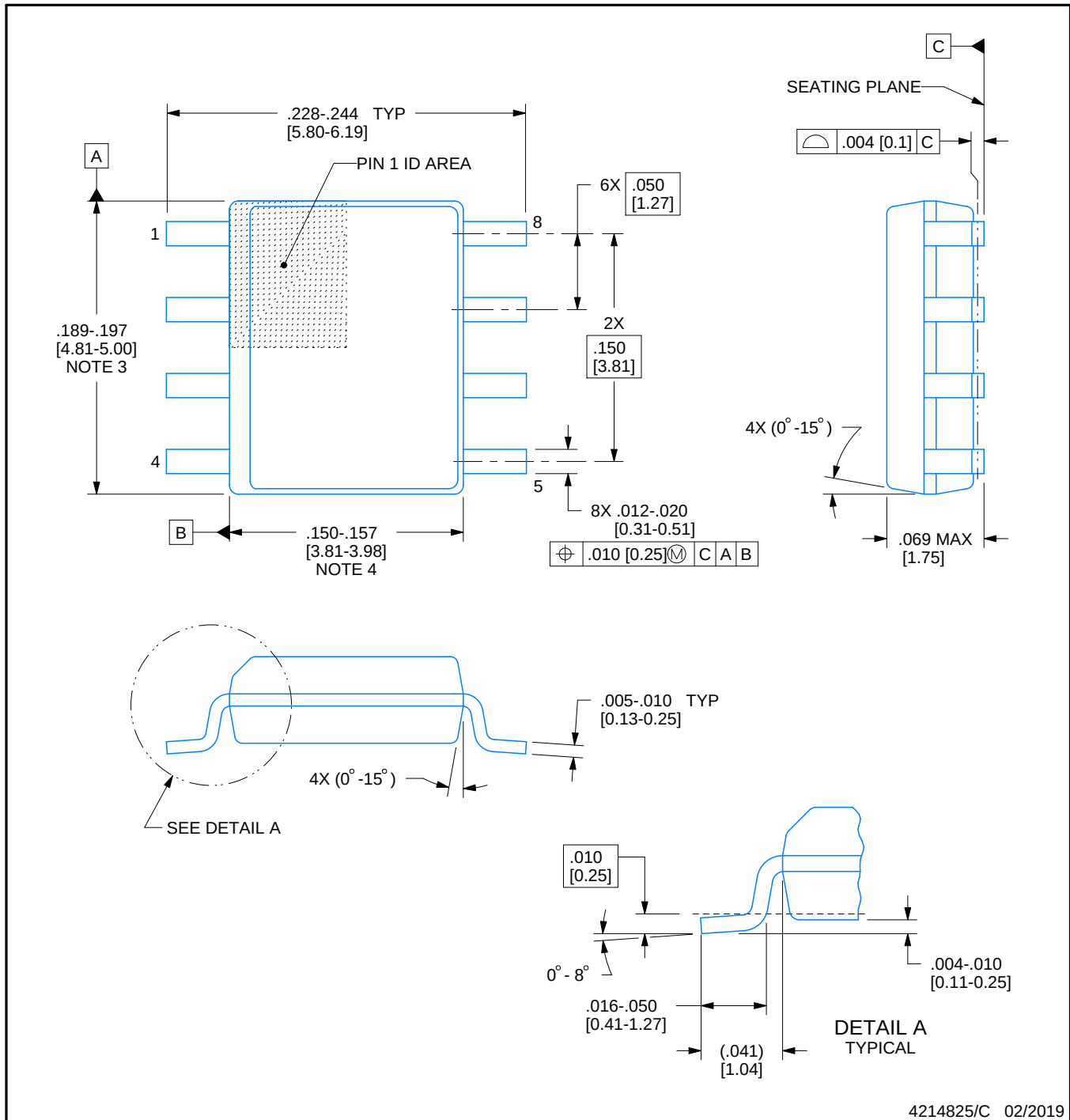


**D0008A**

# PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

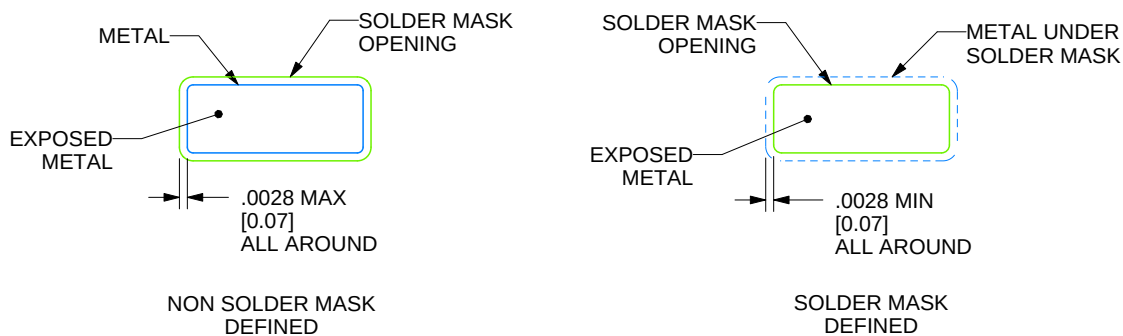
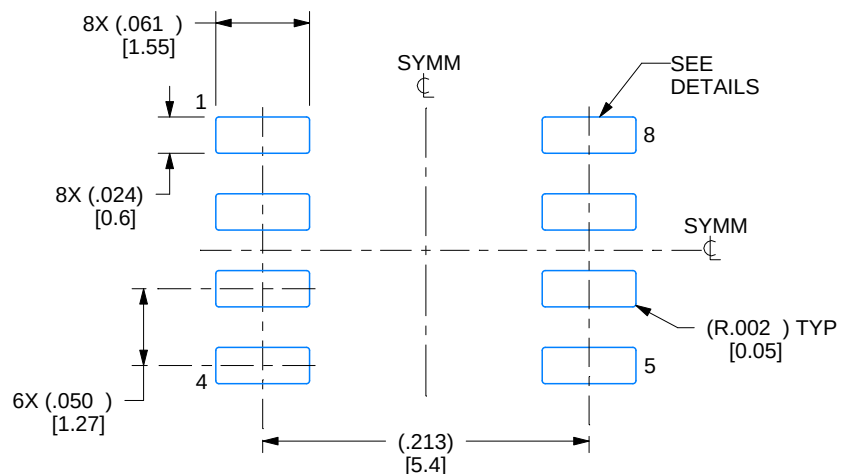
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

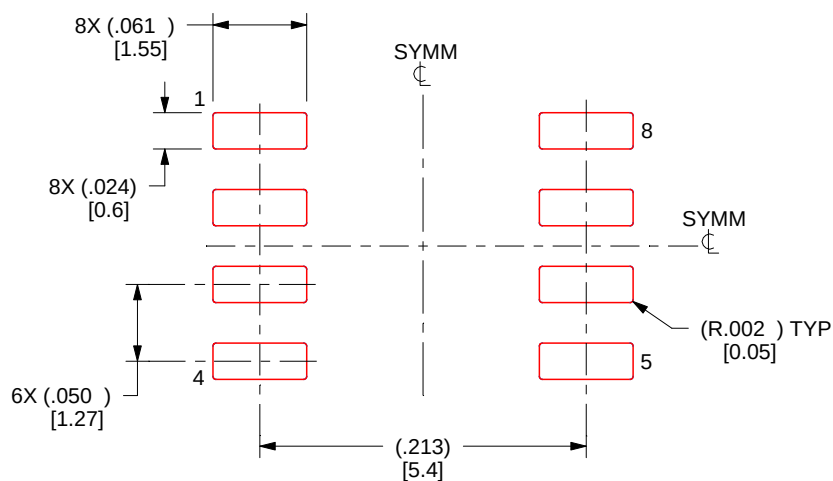
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

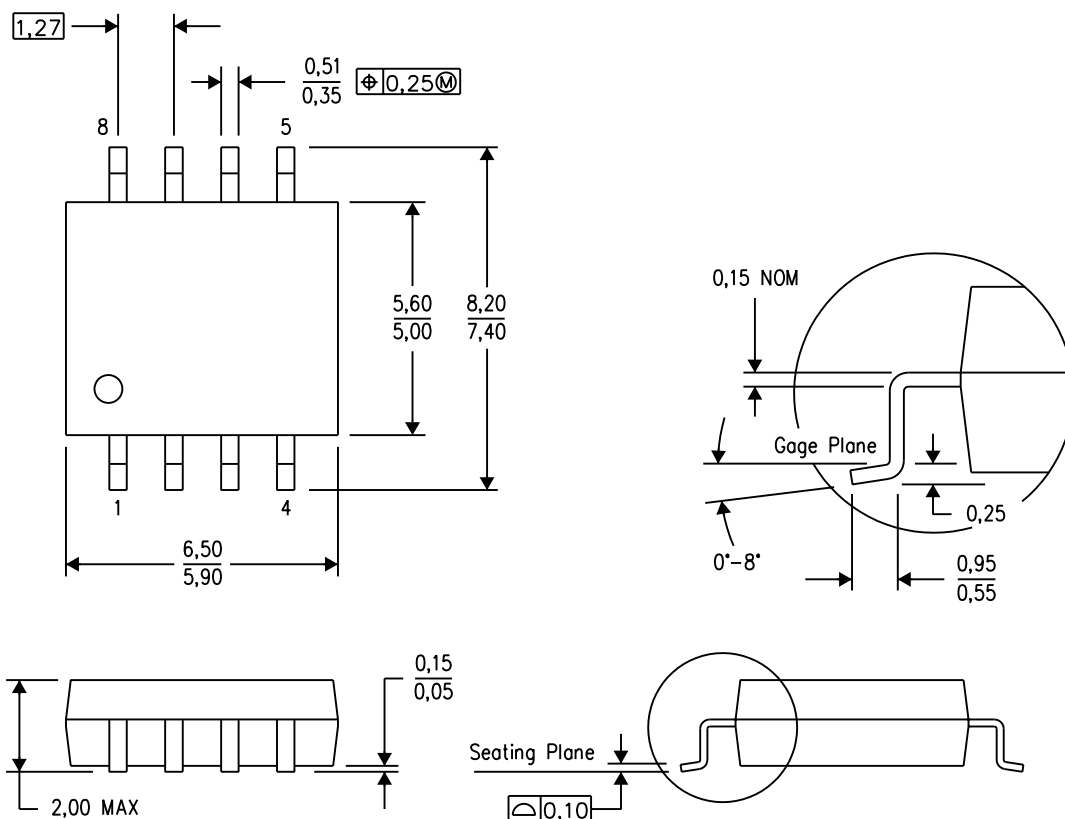
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

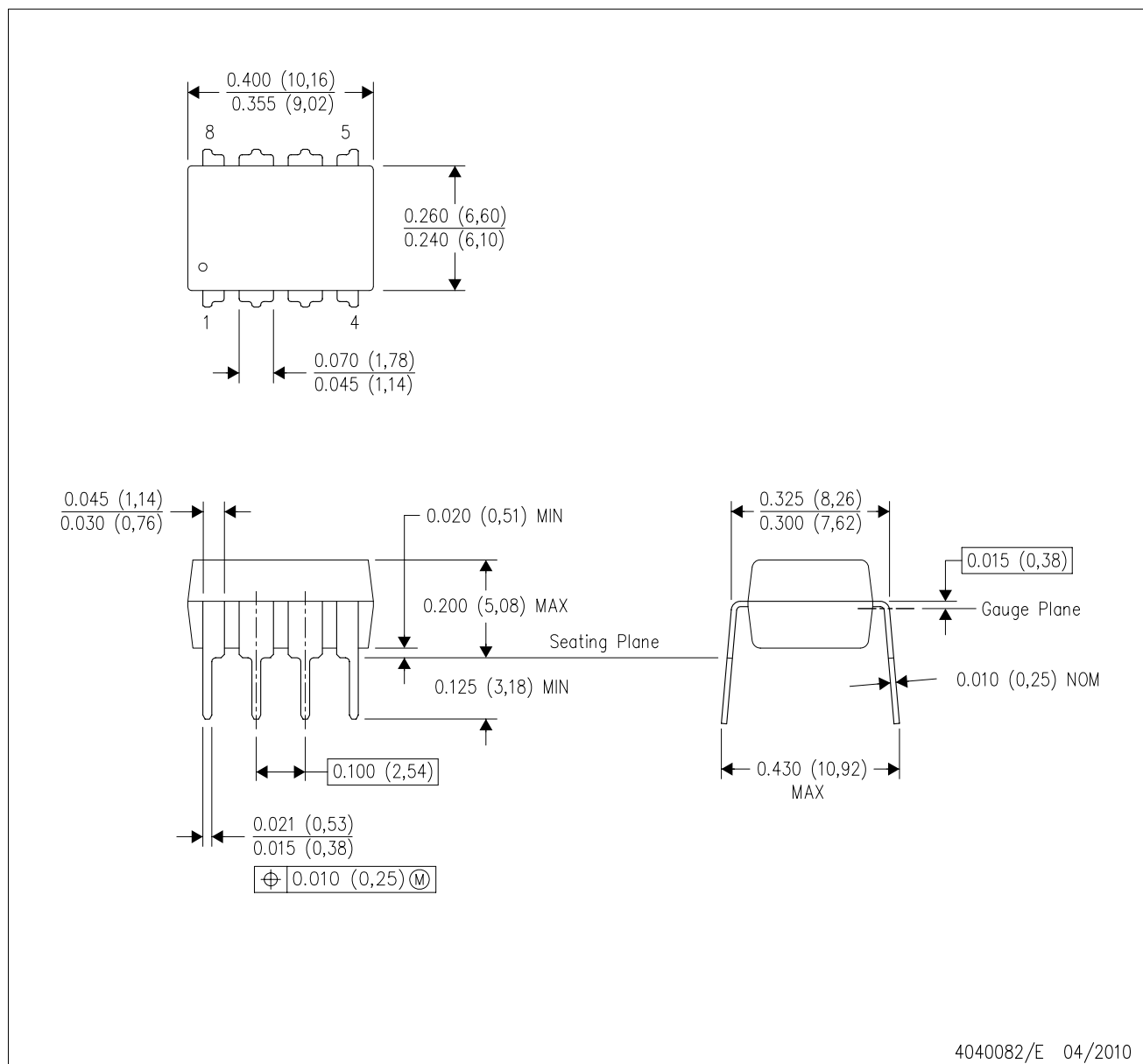


4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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