

# CLASS V 2x2 LVDS CROSSPOINT SWITCH

Check for Samples: SN55LVCP22-SP

#### **FEATURES**

- High Speed (>1000 Mbps) Upgrade for DS90CP22 2x2 LVDS Crosspoint Switch
- · Low-Jitter Fully Differential Data Path
- 50 ps (Typ), of Peak-to-Peak Jitter With PRBS = 2<sup>23</sup>-1 Pattern
- Less Than 200 mW (Typ), 300 mW (Max) Total Power Dissipation
- Output (Channel-to-Channel) Skew Is 80 ps (Typ)
- Configurable as 2:1 Mux, 1:2 Demux, Repeater or 1:2 Signal Splitter
- Inputs Accept LVDS, LVPECL, and CML Signals
- Fast Switch Time of 1.7 ns (Typ)
- Fast Propagation Delay of 0.65 ns (Typ)
- Available in 16 pin CFP Package
- Inter-Operates With TIA/EIA-644-A LVDS Standard
- Military Temperature Range: –55°C to 125°C

#### **APPLICATIONS**

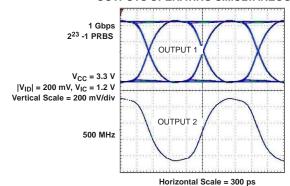
- Base Stations
- Add/Drop Muxes
- Protection Switching for Serial Backplanes
- Network Switches/Routers
- Optical Networking Line Cards/Switches
- Clock Distribution
- Engineering Evaluation (/EM) Samples are Available (1)
- (1) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (e.g. no burn-in, etc.) and are tested to temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance on full MIL specified temperature range of -55°C to 125°C or operating life.

#### DESCRIPTION

The SN55LVCP22 is a 2x2 crosspoint switch providing greater than 1000 Mbps operation for each path. The dual channels incorporate wide commonmode (0 V to 4 V) receivers, allowing for the receipt of LVDS, LVPECL, and CML signals. The dual outputs are LVDS drivers to provide low-power, low-EMI, high-speed operation. The SN55LVCP22 provides a single device supporting 2:2 buffering (repeating), 1:2 splitting, 2:1 multiplexing, 2x2 switching, and LVPECL/CML to LVDS translation on each channel. The flexible operation of the SN55LVCP22 provides a single device to support the redundant serial bus transmission needs (working and protection switching cards) of fault-tolerant switch systems found in optical networking, wireless infrastructure, and data communications systems. TI offers additional gigabit repeater/ translator and crosspoint products in the SN65LVDS100 and SN65LVDS122.

The SN55LVCP22 uses a fully differential data path to ensure low-noise generation, fast switching times, low pulse width distortion, and low jitter. Output channel-to- channel skew is 80 ps (typ) to ensure accurate alignment of outputs in all applications. Both SOIC and TSSOP package options are available to allow easy upgrade for existing solutions, and board area savings where space is critical.

#### **OUTPUTS OPERATING SIMULTANEOUSLY**



A

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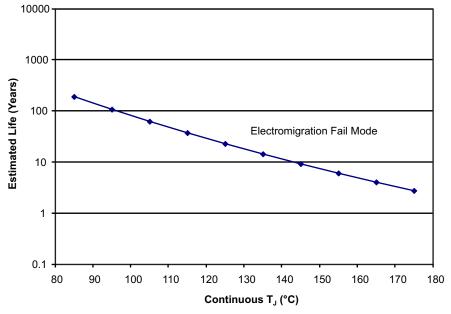


This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### THERMAL CHARACTERISTICS

	PARAMETER		TEST CONDITIONS	VALUE	UNITS
$\theta_{JA}$	Junction-to-ambient thermal resistance			82.5	°C/W
$\theta_{JC}$	Junction-to-case thermal resistance			7.5	°C/W
_	Davisa navvandinainatian	Typical	V <sub>CC</sub> = 3.3 V, T <sub>A</sub> = 25°C, 1 Gbps	198	
$P_{D}$	P <sub>D</sub> Device power dissipation	Maximum	V <sub>CC</sub> = 3.6 V, T <sub>A</sub> = 125°C, 1 Gbps	313	mW



- A. See datasheet for absolute maximum and minimum recommended operating conditions.
- Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
- C. The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

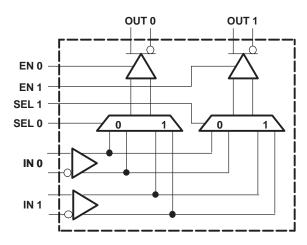
Figure 1. SN55LVCP22-SP Operating Life Derating Chart



**Table 1. FUNCTION TABLE** 

SEL0	SEL1	OUT0	OUT1	FUNCTION
0	0	IN0	IN0	1:2 Splitter
0	1	IN0	IN1	Repeater
1	0	IN1	IN0	Switch
1	1	IN1	IN1	1:2 Splitter

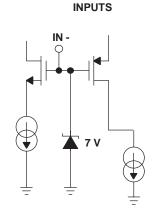
## **FUNCTIONAL BLOCK DIAGRAM**

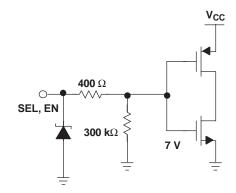




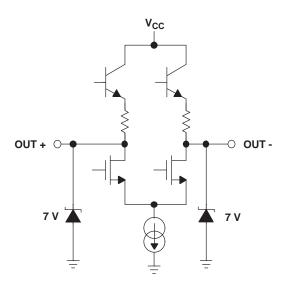
#### **EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS**

# 7 V A





#### **OUTPUTS**



#### **ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range unless otherwise noted (1)

			UNITS
Supply voltage (2) range, \	/cc		–0.5 V to 4 V
CMOS/TTL input voltage	–0.5 V to 4 V		
LVDS receiver input volta	−0.7 V to 4.3 V		
LVDS driver output voltage (OUT+, OUT-)			–0.5 V to 4 V
LVDS output short circuit	current		Continuous
Storage temperature rang	e		–65°C to 125°C
Maximum Junction tempe	rature		150°C
Electrostatic discharge	Human body model <sup>(3)</sup>	All pins	±5 kV
	Charged-device mode (4)	All pins	±500 V

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminals.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101.

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#### RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>	3	3.3	3.6	V
Receiver input voltage	0		4	V
Operating Case Ttemperature range, T <sub>C</sub> <sup>(1)</sup>	<b>-</b> 55		125	°C
Magnitude of differential input voltage  V <sub>ID</sub>	0.1		3	V

<sup>(1)</sup> Maximum case temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

## INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

	PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
CMOS/T	TL DC SPECIFICATIONS (EN0, EN1, SEL0, SEL1)					
V <sub>IH</sub>	High-level input voltage		2		$V_{CC}$	V
$V_{IL}$	Low-level input voltage		GND		8.0	V
I <sub>IH</sub>	High-level input current	$V_{IN} = 3.6 \text{ V or } 2.0 \text{ V}, V_{CC} = 3.6 \text{ V}$	-25	±3	25	μΑ
I <sub>IL</sub>	Low-level input current	V <sub>IN</sub> = 0.0 V or 0.8 V, V <sub>CC</sub> = 3.6 V	-15	±1	15	μΑ
V <sub>CL</sub>	Input clamp voltage	I <sub>CL</sub> = -18 mA		-0.8	-1.5	V
LVDS O	UTPUT SPECIFICATIONS (OUT0, OUT1)					
		$R_L = 75 \Omega$ , See Figure 3	255	365	475	
V <sub>OD</sub>	Differential output voltage	$R_L$ = 75 $\Omega$ , $V_{CC}$ = 3.3 V, $T_A$ = 25°C, See Figure 3	285	365	440	mV
$\Delta  V_{OD} $	Change in differential output voltage magnitude between logic states	V <sub>ID</sub> = ±100 mV, See Figure 3	-25		25	mV
Vos	Steady-state offset voltage	See Figure 4	1	1.2	1.45	V
ΔV <sub>OS</sub>	Change in steady-state offset voltage between logic states	See Figure 4	-25		25	mV
V <sub>OC(PP)</sub>	Peak-to-peak common-mode output voltage	See Figure 4		50		mV
l <sub>OZ</sub>	High-impedance output current	V <sub>OUT</sub> = GND or V <sub>CC</sub>	-15		15	μΑ
I <sub>OFF</sub>	Power-off leakage current	V <sub>CC</sub> = 0 V, 1.5 V; V <sub>OUT</sub> = 3.6 V or GND	-15		15	μΑ
Ios	Output short-circuit current	V <sub>OUT+</sub> or V <sub>OUT-</sub> = 0 V			-8	mA
I <sub>OSB</sub>	Both outputs short-circuit current	V <sub>OUT+</sub> and V <sub>OUT-</sub> = 0 V	-8		8	mA
Co	Differential output capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5 V$		3		pF
LVDS R	ECEIVER DC SPECIFICATIONS (IN0, IN1)	*			·	
$V_{TH}$	Positive-going differential input voltage threshold	See Figure 2 and Table 2			100	mV
$V_{TL}$	Negative-going differential input voltage threshold	See Figure 2 and Table 2	-100			mV
$V_{ID(HYS)}$	Differential input voltage hysteresis			25	150	mV
$V_{\text{CMR}}$	Common-mode voltage range	$V_{ID}$ = 100 mV, $V_{CC}$ = 3.0 V to 3.6 V	0.05		3.95	V
	Input ourront	$V_{IN} = 4 \text{ V}, V_{CC} = 3.6 \text{ V or } 0.0$	-18	±1	18	
I <sub>IN</sub>	Input current	$V_{IN} = 0 \text{ V}, V_{CC} = 3.6 \text{V or } 0.0$	-18	±1	18	μA
C <sub>IN</sub>	Differential input capacitance	$V_I = 0.4 \sin (4E6\pi t) + 0.5 V$		3		pF
SUPPLY	CURRENT					
Iccq	Quiescent supply current	$R_L = 75 \Omega$ , EN0=EN1=High		60	87	mA
I <sub>CCD</sub>	Total supply current	$R_L$ = 75 Ω, $C_L$ = 5 pF, 500 MHz (1000 Mbps), EN0=EN1=High		63	87	mA
I <sub>CCZ</sub>	3-state supply current	EN0 = EN1 = Low		25	35	mA

<sup>(1)</sup> All typical values are at 25°C and with a 3.3-V supply.



#### SWITCHING CHARACTERISTICS

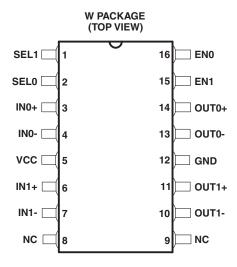
over recommended operating conditions unless otherwise noted

	parameter	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>SET</sub>	Input to SEL setup time	See Figure 7	2.2	0.8		ns
t <sub>HOLD</sub>	Input to SEL hold time	See Figure 7	2.2	1.0		ns
t <sub>SWITCH</sub>	SEL to switched output	See Figure 7		1.7	2.6	ns
t <sub>PHZ</sub>	Disable time, high-level-to-high-impedance	See Figure 6		2	8	ns
t <sub>PLZ</sub>	Disable time, low-level-to-high-impedance	See Figure 6		2	8	ns
t <sub>PZH</sub>	Enable time, high-impedance -to-high-level output	See Figure 6		2	8	ns
t <sub>PZL</sub>	Enable time, high-impedance-to-low-level output	See Figure 6		2	8	ns
t <sub>LHT</sub>	Differential output signal rise time (20%-80%) <sup>(1)</sup>	C <sub>L</sub> = 5 pF, See Figure 5		280	620	ps
t <sub>HLT</sub>	Differential output signal fall time (20%-80%) <sup>(1)</sup>	C <sub>L</sub> = 5 pF, See Figure 5		280	620	ps
		$V_{ID}$ = 200 mV, 50% duty cycle, $V_{CM}$ = 1.2 V, 50 MHz, $C_L$ = 5 pF		13.7	22.2	
		$V_{ID}$ = 200 mV, 50% duty cycle, $V_{CM}$ = 1.2 V, 240 MHz, $C_L$ = 5 pF		13.4	24.5	ps
t <sub>JIT</sub>	Added peak-to-peak jitter	$V_{ID}$ = 200 mV, 50% duty cycle, $V_{CM}$ = 1.2 V, 500 MHz, $C_L$ = 5 pF				
		$V_{ID}$ = 200 mV, PRBS = 2 <sup>15</sup> -1 data pattern, $V_{CM}$ = 1.2 V, 240 Mbps, $C_L$ = 5 pF		68.3	204	
		$V_{ID}$ = 200 mV, PRBS = 2 <sup>15</sup> -1 data pattern, $V_{CM}$ = 1.2 V, 1000 Mbps, $C_L$ = 5 pF		73.2	282	ps
		$V_{ID} = 200 \text{ mV}, 50\% \text{ duty cycle},  V_{CM} = 1.2 \text{ V}, 50 \text{ MHz}, C_L = 5 \text{ pF}$		0.97	1.5	
t <sub>Jrms</sub>	Added random jitter (rms)	$V_{ID}$ = 200 mV, 50% duty cycle, $V_{CM}$ = 1.2 V, 240 MHz, $C_L$ = 5 pF		0.85	1.53	ps <sub>RMS</sub>
		$V_{ID} = 200 \text{ mV}, 50\% \text{ duty cycle},  V_{CM} = 1.2 \text{ V}, 500 \text{ MHz}, C_L = 5 \text{ pF}$		0.86	1.79	
t <sub>PLHD</sub>	Propagation delay time, low-to-high-level output (1)		200	650	2350	ps
t <sub>PHLD</sub>	Propagation delay time, high-to-low-level output (1)		200	650	2350	ps
t <sub>skew</sub> (2)	Pulse skew ( t <sub>PLHD</sub> - t <sub>PHLD</sub>  ) <sup>(3)</sup>	C <sub>L</sub> = 5 pF, See Figure 5		45	160	ps
t <sub>CCS</sub>	Output channel-to-channel skew, splitter mode	C <sub>L</sub> = 5 pF, See Figure 5		80		ps
f <sub>MAX</sub> <sup>(2)</sup>	Maximum operating frequency (4)		1			GHz

 <sup>(1)</sup> Input: V<sub>IC</sub> = 1.2 V, V<sub>ID</sub> = 200 mV, 50% duty cycle, 1 MHz, t<sub>r</sub>/t<sub>f</sub> = 500 ps
 (2) t<sub>skew</sub> and f<sub>MAX</sub> parameters are guaranteed by characterization, but not production tested.
 (3) t<sub>skew</sub> is the magnitude of the time difference between the t<sub>PLHD</sub> and t<sub>PHLD</sub> of any output of a single device.
 (4) Signal generator conditions: 50% duty cycle, t<sub>r</sub> or t<sub>f</sub> ≤ 100 ps (10% to 90%), transmitter output criteria: duty cycle = 45% to 55% V<sub>OD</sub> ≥ 300 mV.



#### **PIN ASSIGNMENTS**



NC - No internal connection

#### PARAMETER MEASUREMENT INFORMATION

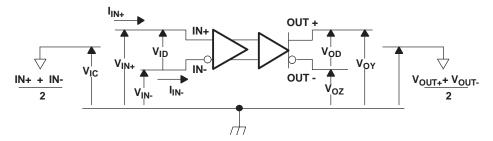


Figure 2. Voltage and Current Definitions

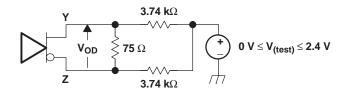
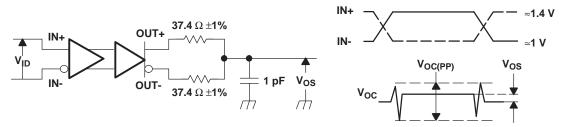


Figure 3. Differential Output Voltage (VoD) Test Circuit

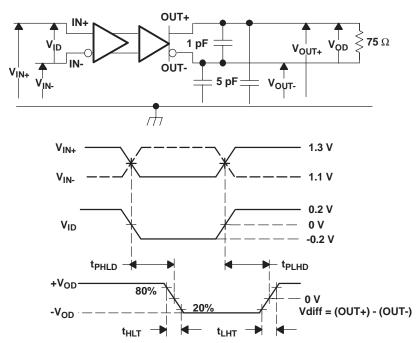


NOTE: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \le 1$  ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ±10 ns;  $R_L$  = 100  $\Omega$ ;  $C_L$  includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.; the measurement of  $V_{OC(PP)}$  is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

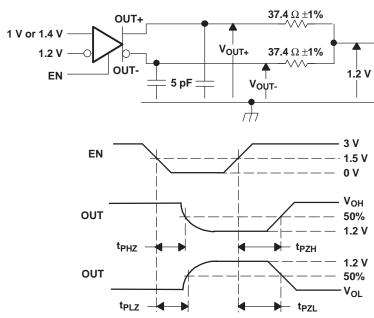


### PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \le .25$  ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500  $\pm$  10 ns.  $C_L$  includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 5. Timing Test Circuit and Waveforms



NOTE: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \le 1$  ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500  $\pm$  10 ns.  $C_L$  includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 6. Enable and Disable Time Circuit and Definitions

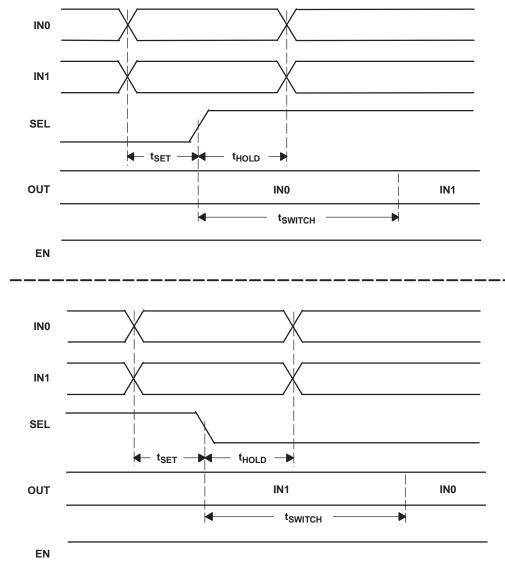


Table 2. Receiver Input Voltage Threshold Test

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON- MODE INPUT VOLTAGE	OUTPUT <sup>(1)</sup>
VIA	V <sub>IB</sub>	V <sub>ID</sub>	V <sub>IC</sub>	
1.25 V	1.15 V	100 mV	1.2 V	Н
1.15 V	1.25 V	−100 mV	1.2 V	L
4.0 V	3.9 V	100 mV	3.95 V	Н
3.9 V	4. 0 V	-100 mV	3.95 V	L
0.1 V	0.0 V	100 mV	0.05 V	Н
0.0 V	0.1 V	–100 mV	0.05 V	L
1.7 V	0.7 V	1000 mV	1.2 V	Н
0.7 V	1.7 V	-1000 mV	1.2 V	L
4.0 V	3.0 V	1000 mV	3.5 V	Н
3.0 V	4.0 V	–1000 mV	3.5 V	L
1.0 V	0.0 V	1000 mV	0.5 V	Н
0.0 V	1.0 V	-1000 mV	0.5 V	L

<sup>(1)</sup> H = high level, L = low level



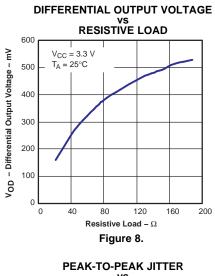


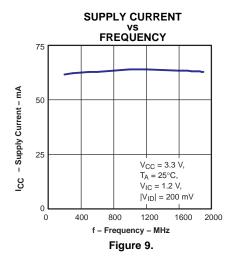
NOTE: t<sub>SET</sub> and t<sub>HOLD</sub> times specify that data must be in a stable state before and after mux control switches.

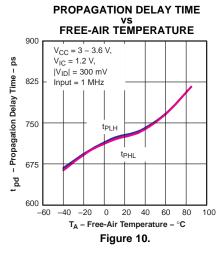
Figure 7. Input to Select for Both Rising and Falling Edge Setup and Hold Times

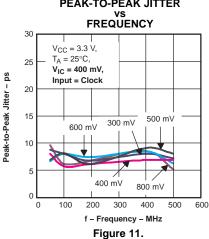


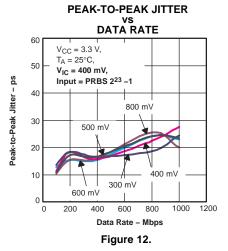
#### TYPICAL CHARACTERISTICS

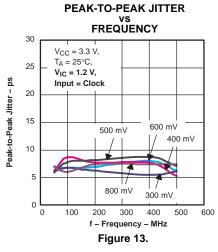


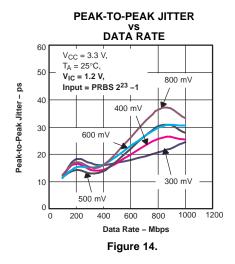


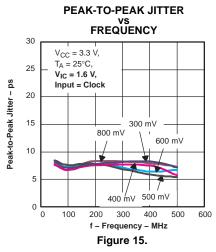


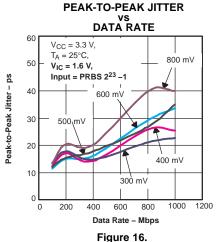






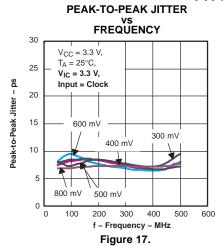


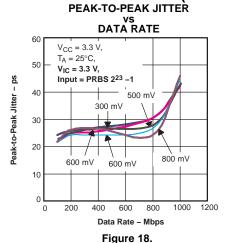






# **TYPICAL CHARACTERISTICS (continued)**





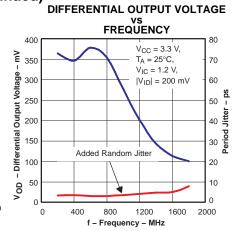
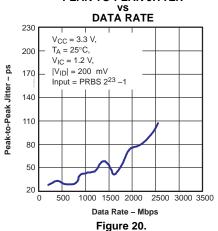


Figure 19.

PEAK-TO-PEAK JITTER



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#### **APPLICATION INFORMATION**

## TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, etc.)

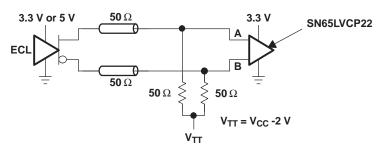


Figure 21. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

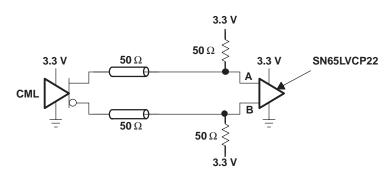


Figure 22. Current-Mode Logic (CML)

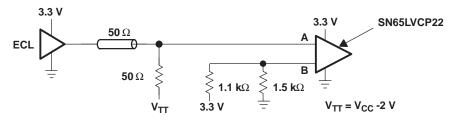


Figure 23. Single-Ended (LVPECL)

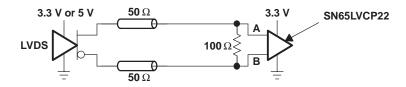


Figure 24. Low-Voltage Differential Signaling (LVDS)



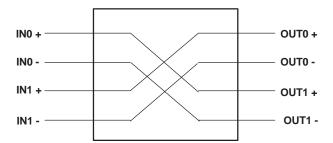


Figure 25. 2 x 2 Crosspoint

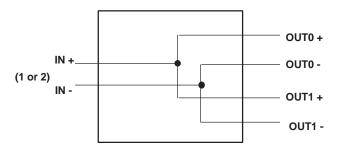


Figure 26. 1:2 Spitter

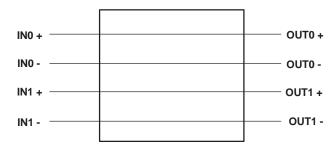


Figure 27. Dual Repeater

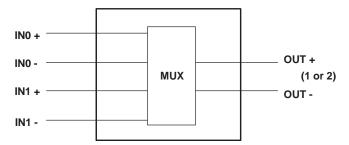


Figure 28. 2:1 MUX



## **REVISION HISTORY**

C	hanges from Original (June 2012) to Revision A	Page
•	Added /EM bullet to FEATURES	1
•	Deleted PACKAGE/ORDERING INFORMATION table	2
•	Changed SWITCHING CHARACTERISTICS, t <sub>JIT</sub> and t <sub>Jrms</sub>	6

Product Folder Links : SN55LVCP22-SP

www.ti.com 7-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
5962-1124201VFA	Last Time Buy	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-1124201VF A LVCP22W-SP
SN55LVCP22W/EM	Last Time Buy	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	0 to 0	SN55LVCP22W/EM EVAL ONLY

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF SN55LVCP22-SP:

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# **PACKAGE OPTION ADDENDUM**

www.ti.com 7-Nov-2025

• Catalog : SN55LVCP22

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

# **PACKAGE MATERIALS INFORMATION**

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## **TUBE**



#### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-1124201VFA	W	CFP	16	25	506.98	26.16	6220	NA
SN55LVCP22W/EM	W	CFP	16	25	506.98	26.16	6220	NA

# W (R-GDFP-F16)

# CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP2-F16



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