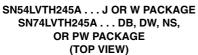
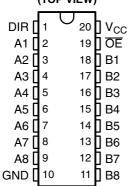
SN54LVTH245A, SN74LVTH245A 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

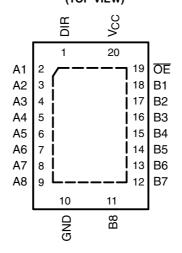
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- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Unregulated Battery Operation Down to 2.7 V
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

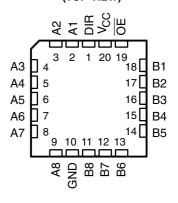




SN74LVTH245A . . . RGY PACKAGE (TOP VIEW)



SN54LVTH245A . . . FK PACKAGE (TOP VIEW)



description/ordering information

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

ORDERING INFORMATION

| T _A | PACKAGE ⁻ | t | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------------------|----------------|--------------------------|------------------|
| | QFN – RGY | Tape and reel | SN74LVTH245ARGYR | LXH245A |
| | SOIC - DW | Tube | SN74LVTH245ADW | LVTH045A |
| | SOIC - DW | Tape and reel | SN74LVTH245ADWR | LVTH245A |
| | SOP - NS | Tape and reel | SN74LVTH245ANSR | LVTH245A |
| –40°C to 85°C | SSOP - DB | Tape and reel | SN74LVTH245ADBR | LXH245A |
| | TOOOD DW | Tube | SN74LVTH245APW | 1 VI IO 45 A |
| | TSSOP – PW | Tape and reel | SN74LVTH245APWR | LXH245A |
| | VFBGA – GQN | Ton a and week | SN74LVTH245AGQNR | 1 VI 10 4 F A |
| | VFBGA – ZQN (Pb-free) | Tape and reel | SN74LVTH245AZQNR | LXH245A |
| | CDIP – J | Tube | SNJ54LVTH245AJ | SNJ54LVTH245AJ |
| –55°C to 125°C | CFP – W | Tube | SNJ54LVTH245AW | SNJ54LVTH245AW |
| | LCCC - FK | Tube | SNJ54LVTH245AFK | SNJ54LVTH245AFK |

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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description/ordering information (continued)

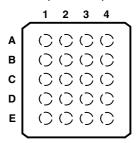
These devices are designed for asynchronous communication between data buses. They transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the devices so the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

SN74LVTH245A . . . GQN OR ZQN PACKAGE (TOP VIEW)



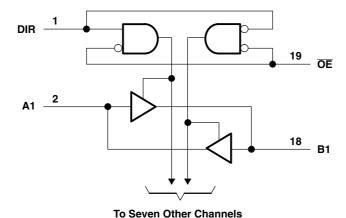
terminal assignments

| | 1 | 2 | 3 | 4 |
|---|-----|-----|----------|----|
| Α | A1 | DIR | V_{CC} | ŌĒ |
| В | А3 | B2 | A2 | B1 |
| С | A5 | A4 | B4 | B3 |
| D | A7 | B6 | A6 | B5 |
| Е | GND | A8 | B8 | B7 |

FUNCTION TABLE

| INP | UTS | ODEDATION |
|-----|-----|-----------------|
| ŌĒ | DIR | OPERATION |
| L | L | B data to A bus |
| L | Н | A data to B bus |
| Н | Χ | Isolation |

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, FK, J, NS, PW, RGY, and W packages.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| Supply voltage range, V _{CC} | –0.5 V to 4.6 V |
|--|-----------------------------------|
| Input voltage range, V _I (see Note 1) | |
| Voltage range applied to any output in the high-impedance | |
| or power-off state, V _O (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high state, V _O (see Note 1) | –0.5 V to V _{CC} + 0.5 V |
| Current into any output in the low state, I _O : SN54LVTH245A | 96 mA |
| SN74LVTH245A | 128 mA |
| Current into any output in the high state, I _O (see Note 2): SN54LVTH245A | 48 mA |
| SN74LVTH245A | 64 mA |
| Input clamp current, I _{IK} (V _I < 0) | –50 mA |
| Output clamp current, I _{OK} (V _O < 0) | –50 mA |
| Package thermal impedance, θ_{JA} (see Note 3): DB package | 70°C/W |
| (see Note 3): DW package | 58°C/W |
| (see Note 3): GQN/ZQN package | 78°C/W |
| (see Note 3): NS package | 60°C/W |
| (see Note 3): PW package | 83°C/W |
| (see Note 4): RGY package | 37°C/W |
| Storage temperature range, T _{stg} | –65°C to 150°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.
- 4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

| | | | SN54LVT | H245A | SN74LVT | H245A | UNIT |
|--------------------------|------------------------------------|-----------------|---------|-------|---------|-------|------|
| | | | MIN | MAX | MIN | MAX | UNIT |
| V _{CC} | Supply voltage | y voltage | | | | | V |
| V _{IH} | High-level input voltage | 2 | | 2 | | V | |
| V _{IL} | Low-level input voltage | | 0.8 | | 0.8 | V | |
| VI | Input voltage | | 5.5 | | 5.5 | V | |
| I _{OH} | High-level output current | | | -24 | | -32 | mA |
| I _{OL} | Low-level output current | | | 48 | | 64 | mA |
| Δt/Δν | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | | 200 | | 200 | | μs/V |
| T _A | Operating free-air temperature | | -55 | 125 | -40 | 85 | °C |

NOTE 5: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN54LVTH245A, SN74LVTH245A 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| DA | DAMETER | TEOT 0 | ONDITIONS | SN5 | 4LVTH2 | 45A | SN7 | 4LVTH2 | 45A | | | | | |
|----------------------|----------------|--|-----------------------------|---------------------|--------|-------|---------------------|--------|-------------|------|--|--|--|--|
| PA | RAMETER | TEST C | ONDITIONS | MIN | TYP† | MAX | MIN | TYP† | MAX | UNIT | | | | |
| V _{IK} | | $V_{CC} = 2.7 \text{ V},$ | I _I = -18 mA | | | -1.2 | | | -1.2 | V | | | | |
| | | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V},$ | $I_{OH} = -100 \mu A$ | V _{CC} -0. | 2 | | V _{CC} -0. | 2 | | | | | | |
| l ,, | | $V_{CC} = 2.7 \text{ V},$ | $I_{OH} = -8 \text{ mA}$ | 2.4 | | | 2.4 | | | V | | | | |
| V _{OH} | | V 2V | $I_{OH} = -24 \text{ mA}$ | 2 | | | | | | V | | | | |
| | | V _{CC} = 3 V | $I_{OH} = -32 \text{ mA}$ | | | | 2 | | | | | | | |
| | | V 0.7.V | $I_{OL} = 100 \mu A$ | | | 0.2 | | | 0.2 | | | | | |
| | | V _{CC} = 2.7 V | I _{OL} = 24 mA | | | 0.5 | | | 0.5 | | | | | |
| ., | | | I _{OL} = 16 mA | | | 0.4 | | | 0.4 | ., | | | | |
| V _{OL} | | \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ | $I_{OL} = 32 \text{ mA}$ | | | 0.5 | | | 0.5 | V | | | | |
| | | V _{CC} = 3 V | $I_{OL} = 48 \text{ mA}$ | | | 0.55 | | | | | | | | |
| | | | I _{OL} = 64 mA | | | | | | 0.55 | | | | | |
| | Control inputs | $V_{CC} = 3.6 \text{ V},$ | $V_I = V_{CC}$ or GND | | | ±1 | | | ±1 | | | | | |
| | I _I | $V_{CC} = 0 \text{ or } 3.6 \text{ V},$ | V _I = 5.5 V | | | 10 | | | 10 | | | | | |
| lį | | | V _I = 5.5 V | | | 20 | | | 20 | μΑ | | | | |
| | A or B ports‡ | V _{CC} = 3.6 V | $V_I = V_{CC}$ | | | 1 | | | 1 | - | | | | |
| | | | V _I = 0 | | | -5 | | | - 5 | | | | | |
| I _{off} | | $V_{CC} = 0$, | V_I or $V_O = 0$ to 4.5 V | | | | | | ±100 | μΑ | | | | |
| | | V _{CC} = 3 V | V _I = 0.8 V | 75 | | | 75 | | | | | | | |
| I _{I(hold)} | A or B ports | | V _I = 2 V | -75 | | | -75 | | | μΑ | | | | |
| il(noid) | 7 or B porto | V _{CC} = 3.6 V [§] , | V _I = 0 to 3.6 V | | | | | | 500 -750 | μπ | | | | |
| I _{OZPU} | | $V_{CC} = 0$ to 1.5 V, $V_O = 0$ $\overline{OE} = \text{don't care}$ | 0.5 V to 3 V, | | | ±100* | | | ±100 | μА | | | | |
| I _{OZPD} | | V_{CC} = 1.5 V to 0, V_{O} = \overline{OE} = don't care | 0.5 V to 3 V, | | | ±100* | | | ±100 | μА | | | | |
| | | V _{CC} = 3.6 V, | Outputs high | | | 0.19 | | | 0.19 | | | | | |
| I _{CC} | | $I_0 = 0$, | Outputs low | | | 5 | 5 | | 5 | mA | | | | |
| | | $V_I = V_{CC}$ or GND | Outputs disabled | | | 0.19 | | | 0.19 | | | | | |
| Δl _{CC} ¶ | | $V_{CC} = 3 \text{ V to } 3.6 \text{ V, One}$ Other inputs at V_{CC} or | | | | 0.2 | | | 0.2 | mA | | | | |
| C _i | | V _I = 3 V or 0 | | | 4 | | | 4 | | | | | | |
| C _{io} | | V _O = 3 V or 0 | | | 9 | | | 9 | | pF | | | | |

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.



 $^{^{\}dagger}$ All typical values are at V_{CC} = 3.3 V, T_{A} = 25 $^{\circ}C.$

 $[\]mbox{‡}$ Unused terminals are at $\mbox{$V_{CC}$}$ or GND.

[§] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

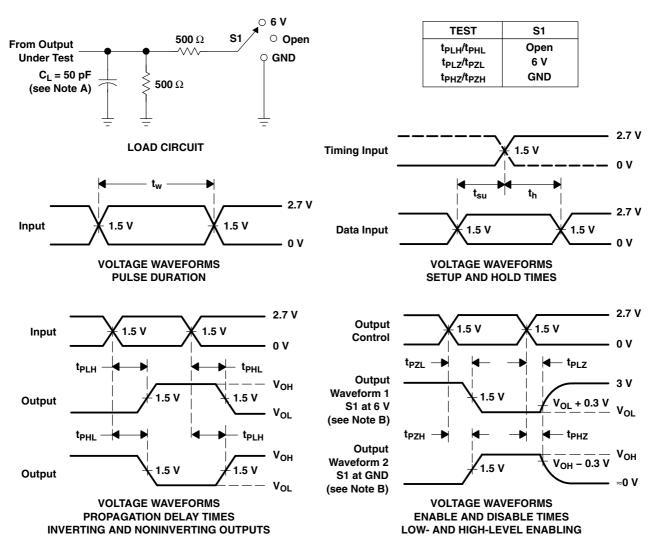
This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| | | | ; | SN54LVTH245A | | | | SN7 | 4LVTH2 | 45A | | |
|------------------|-----------------|----------------|------------------------------|--------------|-------------------------|-----|------------------------------|------|--------|-------------------------|-----|------|
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} = 3.3 V \pm 0.3 V | | V _{CC} = 2.7 V | | V_{CC} = 3.3 V \pm 0.3 V | | | V _{CC} = 2.7 V | | UNIT |
| | | | MIN | MAX | MIN | MAX | MIN | TYP† | MAX | MIN | MAX | |
| t _{PLH} | | D or A | 0.7 | 3.7 | | 4.2 | 1.2 | 2.3 | 3.5 | | 4 | |
| t _{PHL} | A or B | B or A | 0.7 | 3.7 | | 4.2 | 1.2 | 2.1 | 3.5 | | 4 | ns |
| t _{PZH} | <u> </u> | A or D | 1.2 | 5.7 | | 7.4 | 1.3 | 3.2 | 5.5 | | 7.1 | 20 |
| t _{PZL} | ŌĒ | A or B | 1.6 | 5.7 | | 6.8 | 1.7 | 3.4 | 5.5 | | 6.5 | ns |
| t _{PHZ} | OF | A or B | 1.8 | 6.2 | | 6.8 | 2.2 | 3.5 | 5.9 | | 6.5 | |
| t _{PLZ} | ŌĒ | | 1.8 | 5.3 | | 5.5 | 2.2 | 3.4 | 5 | | 5.1 | ns |

 $^{^{\}dagger}$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{Q} = 50 Ω , $t_{r} \leq$ 2.5 ns, $t_{f} \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

| Orderable part number | Status | Material type | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material | MSL rating/ Peak reflow | Op temp (°C) | Part marking (6) |
|-----------------------|--------|---------------|----------------|-----------------------|-----------------|-------------------------------|----------------------------|--------------|--|
| 5962-9564201Q2A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9564201Q2A SNJ54LVTH 245AFK |
| 5962-9564201QRA | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9564201QR A SNJ54LVTH245AJ |
| 5962-9564201QSA | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9564201QS A SNJ54LVTH245AW |
| 5962-9564201V2A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9564201V2A SNV54LVTH 245AFK |
| 5962-9564201VRA | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9564201VR A SNV54LVTH245AJ |
| 5962-9564201VSA | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9564201VS A SNV54LVTH245AW |
| SN74LVTH245ADBR | Active | Production | SSOP (DB) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH245A |
| SN74LVTH245ADBR.B | Active | Production | SSOP (DB) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH245A |
| SN74LVTH245ADBR1G4 | Active | Production | SSOP (DB) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH245A |
| SN74LVTH245ADBR1G4.B | Active | Production | SSOP (DB) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH245A |
| SN74LVTH245ADW | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH245A |
| SN74LVTH245ADW.B | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH245A |
| SN74LVTH245ADWR | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH245A |
| SN74LVTH245ADWR.B | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH245A |
| SN74LVTH245ADWRG4 | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH245A |
| SN74LVTH245ANS.B | Active | Production | SOP (NS) 20 | 40 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH245A |
| SN74LVTH245ANSR | Active | Production | SOP (NS) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH245A |
| SN74LVTH245ANSR.B | Active | Production | SOP (NS) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH245A |
| SN74LVTH245ANSRG4 | Active | Production | SOP (NS) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH245A |





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| Orderable part number | Status (1) | Material type | Package Pins | Package qty Carrier | RoHS | Lead finish/ Ball material | MSL rating/ Peak reflow | Op temp (°C) | Part marking (6) |
|-----------------------|------------|---------------|-----------------|-----------------------|------|-------------------------------|----------------------------|--------------|--|
| SN74LVTH245ANSRG4.B | Active | Production | SOP (NS) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH245A |
| SN74LVTH245APW | Active | Production | TSSOP (PW) 20 | 70 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH245A |
| SN74LVTH245APW.B | Active | Production | TSSOP (PW) 20 | 70 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH245A |
| SN74LVTH245APWE4 | Active | Production | TSSOP (PW) 20 | 70 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH245A |
| SN74LVTH245APWG4 | Active | Production | TSSOP (PW) 20 | 70 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH245A |
| SN74LVTH245APWR | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | LXH245A |
| SN74LVTH245APWR.B | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH245A |
| SN74LVTH245APWRE4 | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH245A |
| SN74LVTH245APWRG4 | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH245A |
| SN74LVTH245APWRG4.B | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH245A |
| SN74LVTH245ARGYR | Active | Production | VQFN (RGY) 20 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LXH245A |
| SN74LVTH245ARGYR.B | Active | Production | VQFN (RGY) 20 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LXH245A |
| SN74LVTH245ARGYRG4 | Active | Production | VQFN (RGY) 20 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LXH245A |
| SN74LVTH245ARGYRG4.B | Active | Production | VQFN (RGY) 20 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LXH245A |
| SNJ54LVTH245AFK | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9564201Q2A SNJ54LVTH 245AFK |
| SNJ54LVTH245AJ | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9564201QR A SNJ54LVTH245AJ |
| SNJ54LVTH245AW | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9564201QS A SNJ54LVTH245AW |

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

PACKAGE OPTION ADDENDUM

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(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54LVTH245A, SN54LVTH245A-SP, SN74LVTH245A:

Catalog: SN74LVTH245A, SN54LVTH245A

Enhanced Product: SN74LVTH245A-EP, SN74LVTH245A-EP

Military: SN54LVTH245A

Space : SN54LVTH245A-SP

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application



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TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

| A0 | Dimension designed to accommodate the component width |
|----|---|
| В0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|-----------------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| SN74LVTH245ADBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVTH245ADBR1G4 | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVTH245ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LVTH245ANSR | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LVTH245ANSRG4 | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LVTH245APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74LVTH245APWRG4 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74LVTH245ARGYR | VQFN | RGY | 20 | 3000 | 330.0 | 12.4 | 3.71 | 4.71 | 1.1 | 8.0 | 12.0 | Q1 |
| SN74LVTH245ARGYRG4 | VQFN | RGY | 20 | 3000 | 330.0 | 12.4 | 3.71 | 4.71 | 1.1 | 8.0 | 12.0 | Q1 |



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*All dimensions are nominal

| All difficultions are norminal | | | | | | | |
|--------------------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
| SN74LVTH245ADBR | SSOP | DB | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVTH245ADBR1G4 | SSOP | DB | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVTH245ADWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74LVTH245ANSR | SOP | NS | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74LVTH245ANSRG4 | SOP | NS | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74LVTH245APWR | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVTH245APWRG4 | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVTH245ARGYR | VQFN | RGY | 20 | 3000 | 353.0 | 353.0 | 32.0 |
| SN74LVTH245ARGYRG4 | VQFN | RGY | 20 | 3000 | 353.0 | 353.0 | 32.0 |

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9564201Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9564201V2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9564201VSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74LVTH245ADW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74LVTH245ADW.B | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74LVTH245ANS.B | NS | SOP | 20 | 40 | 530 | 10.5 | 4000 | 4.1 |
| SN74LVTH245APW | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| SN74LVTH245APW.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| SN74LVTH245APWE4 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| SN74LVTH245APWG4 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| SNJ54LVTH245AFK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

 D. Index point is provided on cap for terminal identification only.

 E. Falls within Mil—Std 1835 GDFP2—F20







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





PLASTIC QUAD FLATPACK - NO LEAD



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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SOIC



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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