SDLS195 - MARCH 1985 - REVISED MARCH 1988

#### **'LS673**

- 16-Bit Serial-In, Serial-Out Shift Register with 16-Bit Parallel-Out Storage Register
- Performs Serial-to-Parallel Conversion

#### **'LS674**

- 16-Bit Parallel-In, Serial-Out Shift Register
- Performs Parallel-to-Serial Conversion

#### description

# SN54LS673, SN74LS673

The 'LS673 is a 16-bit shift register and a 16-bit storage register in a single 24-pin package. A three-state input/output (SER/Q15) port to the shift register allows serial entry and/or reading of data. The storage register is connected in a parallel data loop with the shift register and may be asynchronously cleared by taking the storeclear input low. The storage register may be parallel loaded with shift-register data to provide shift-register status via the parallel outputs. The shift register can be parallel loaded with the storage-register data upon command.

A high logic level at the chip-level ( $\overline{CS}$ ) input disables both the shift-register clock and the storage register clock and places SER/Q15 in the high-impedance state. The store-clear function is not disabled by the chip select.

Caution must be exercised to prevent false clocking of either the shift register or the storage register via the chip-select input. The shift clock should be low during the low-to-high transition of chip select and the store clock should be low during the high-to-low transition of chip select.

#### SN54LS674, SN74LS674

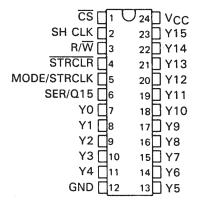
The 'LS674 is a 16-bit parallel-in, serial-out shift register. A three-state input/output (SER/Q15) port provides access for entering a serial data or reading the shift-register word in a recirculating loop.

The device has four basic modes of operation:

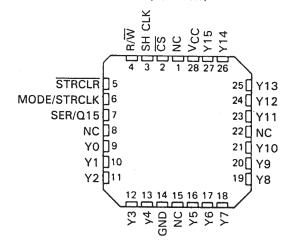
- 1) Hold (do nothing)
- 2) Write (serially via input/output)
- 3) Read (serially)
- 4) Load (parallel via data inputs)

Low-to-high-level changes at the chip select input should be made only when the clock input is low to prevent false clocking.

#### SN54LS673...J OR W PACKAGE SN74LS673...DW OR N PACKAGE (TOP VIEW)



# SN54LS673 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

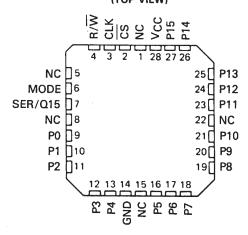
# SN54LS673, SN54LS674, SN74LS673, SN74LS674 16-BIT SHIFT REGISTERS

SDLS195 - MARCH 1985 - REVISED MARCH 1988

SN54LS674 . . . J OR W PACKAGE SN74LS674 . . . DW OR N PACKAGE (TOP VIEW)

#### CS [1 U24] VCC CLK 2 23 P15 **R/W** □3 22 P14 NC ∏4 21 P13 20 P12 MODE ∏5 SER/Q15 ∏6 19 P11 P0 🛮 7 18 P10 17 P9 P2 9 16 P8 P3 []10 15 P7 P4 ∐11 14 P6 GND ☐12 13 P5

# SN54LS674 . . . FK PACKAGE (TOP VIEW)



# 'LS673 FUNCTION TABLE

		INPL	JTS	MODE/	SER/ Q15	SHIFT REGISTER FUNCTIONS  READ FROM   WRITE INTO   PARALLEL					RAGE
CS	R/W	SH CLK	STRCLR	STRCLK	u is	SHIFT	SERIAL OUTPUT	SERIAL INPUT	LOAD	FUNCTIONS CLEAR LOAD	
Н	Х	X	Х	X	Z	NO	NO	NO	NO		NO
X	Х	Х	L	Х						YES	
L	L	Į.	Х	Х	Z	YES	NO	YES	NO		
L	Н	х	Х	Х	Q15		YES	NO			NO
L	Н	↓	Х	L	Q14n	YES	YES	NO	NO		NO
L	Н	Ţ	L	Н	L	NO	YES		YES	YES	NO
L	Н	ļ	Н	Н	Y15n	NO	YES		YES	NO	NO
L	L	Х	H	1	Z		NO		NO	NO	YES

## **'LS674 FUNCTION TABLE**

		INPUTS		SER/				
cs	R/W	MODE	CLK	Q15	OPERATION			
Н	X	X	х	Z	Do nothing			
L	L	x	1	z	Shift and write (serial load)			
L	н	L	Į.	Q14n	Shift and read			
L	Н	Н	1	P15	Parallel load			

H = high level (steady state)

L = low level (steady state)

1 = transition from low to high level

 $\downarrow$  = transition from high to low level

X = irrelevant (any input including transitions)

Z = high impedance, input mode

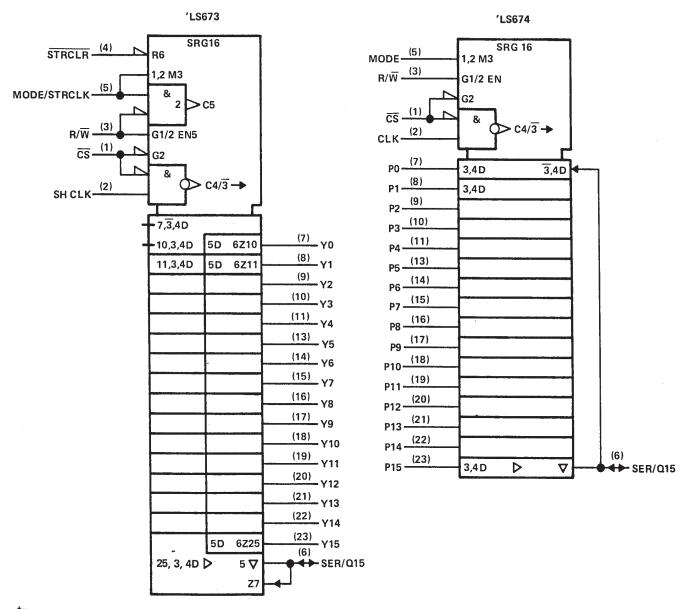
Q14n = content of 14th bit of the shift register before the most recent \$\foat\$ transition of the clock.

Q15 = present content of 15th bit of the shift register

Y15n = content of the 15th bit of the storage register before the most recent \$\psi\$ transition of the clock.

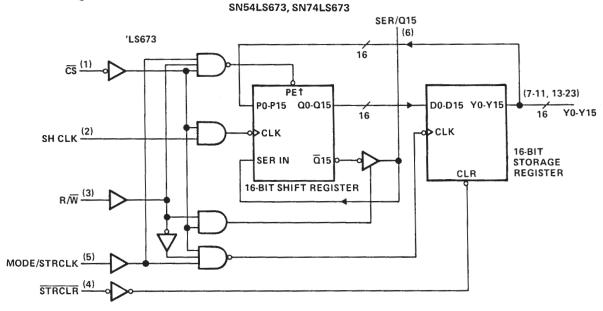
P15 = level of input P15

# logic symbols†

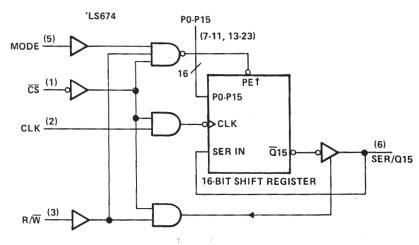


<sup>&</sup>lt;sup>†</sup>These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, N, and W packages.

# functional block diagrams

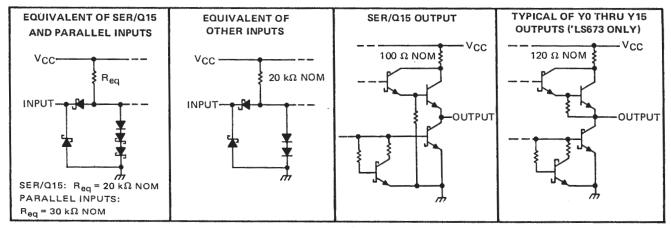


#### SN54LS674, SN74LS674



<sup>†</sup>When PE is active, data is synchronously parallel loaded into the shift registers from the 16 P inputs and no shifting takes place. Pin numbers shown are for DW, J, N, and W packages.

# schematics of inputs and outputs



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	
Input voltage: SER/Q15	5.5 V
All others	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS673, SN54LS674	
`SN74LS673, SN74LS674	o 70°C
Storage temperature range—65°C to	150°C

NOTE 1. Voltage values are with respect to network ground terminal.

#### recommended operating conditions

					SN54LS	•	5	N74LS'		1.18117
				MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage				5	5.5	4.75	5	5.25	V
lau	High-level output current	SER/Q15				- 1			-2.6	mA
ЮН	riigii-level output culterit	Y0 thru Y15			-0.4			-0.4	'''	
loi	Low-level output current	SER/Q15				12			24	mA
loL	Low-level output current	Y0 thru Y15		4				8	1 '''	
fclock	Clock frequency			0		20	0		20	MHz
tw(clock)	Width of clock input pulse			20			20			ns
tw(clear)	Width of clear input pulse			20			20			ns
		SER/Q15		20			20			
	Setup time	P0 thru P15	20			20			1	
<b>t</b>		Mode	35			35			ns	
t <sub>su</sub>		R/W, CS	35			35			] '''	
		SH CLK ↓ to Mode/STR CLK ↑ See Note 2		25			25			
		SER/Q15		0			0			
	Hold time	P0 thru P15	'LS673	0			0			ns
th	Hold time	PothruP15	'LS674	5.0			5.0			] ""
		Mode		0			. 0			]
T <sub>A</sub>	Operating free-air temperat	ure		- 55		125	0		70	°C

NOTE 2: This setup time ensures the storage register will see stable data from the shift register.



# SN54LS673, SN54LS674, SN74LS673, SN74LS674 16-BIT SHIFT REGISTERS

SDLS195 - MARCH 1985 - REVISED MARCH 1988

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONI	DITIONST		SN54LS	3'	SN74LS'			UNIT
	FARAMETER		TEST CONL	)	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage				2			2			V
VIL	Low-level input voltage	Low-level input voltage					0.7			0.8	V
VIK	Input clamp voltage		V <sub>CC</sub> = MIN,	I <sub>I</sub> = -18 mA			-1.5			-1.5	V
Vон	High-level output voltage	SER/Q15	VCC = MIN,	V <sub>1H</sub> = 2 V,	2.4	3.2		2.4	3.1		V
VOH		Y0 thru Y15¶	V <sub>IL</sub> = V <sub>IL</sub> max,	$I_{OH} = MAX$	2.5	3.4		2.7	3.4		
		SER/Q15	V MIN	I <sub>OL</sub> = 12 mA		0.25	0.4		0.25	0.4	
٧	Low-level output voltage	3211/013	V <sub>CC</sub> = MIN,	I <sub>OL</sub> = 24 mA					0.35	0.5	V
VOL	Low-level output voltage	Y0 thru Y15¶	V <sub>IH</sub> = 2 V,	IOL = 4 mA		0.25	0.4		0.25	0.4	
			V <sub>IL</sub> = V <sub>IL</sub> max	I <sub>OL</sub> = 8 mA					0.35	0.5	
10-11	Off-state output current,	SER/Q15	VCC = MAX,	V <sub>IH</sub> = 2 V,		40				40	
lozh	high-level voltage applied	-SEN/Q15	VIL = VILmax,	$V_0 = 2.7 V$						40	μΑ
lozu	Off-state output current,	050/045	V <sub>CC</sub> = MAX,	V <sub>IH</sub> = 2 V,	T						
IOZL	low-level voltage applied	SER/Q15	VIL = VILmax,	$V_0 = 0.4 V$	- 0.4				- 0.4	mA	
1.	Input current at maximum	SER/Q15	V <sub>CC</sub> = MAX	V <sub>I</sub> = 5.5 V			0.1			0.1	
Ц	input voltage	Others	ACC - MAY	V <sub>I</sub> = 7 V			0.1			0.1	mA
ЧН	High-level input current	SER/Q15	Vcc = MAX,	V <sub>1</sub> = 2.7 V			40			40	
'IH	riigii-level iliput carreit	Others	VCC - WAX,	V1 = 2.7 V			20			20	μА
IIL	Low-level input current		VCC = MAX,	V <sub>I</sub> = 0.4 V			-0.4			-0.4	mA
los	Short-circuit output current§	SER/Q15	V <sub>CC</sub> = MAX		-30		-130	-30		-130	
-03	onort-circuit output currents	Y0 thru Y15¶	VCC - WAX	-20		-100	-20		-100	mA	
Icc	Supply current	'LS673	Voc = MAY			50	80		52	80	^
100	Supply culterit	'LS674	V <sub>CC</sub> = MAX			25	40		25	40	mA

<sup>&</sup>lt;sup>†</sup>For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

# switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$ , see note 2

PARAMETER	'L	S673	'LS	674	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PARAMETER	FROM	то	FROM	FROM TO TEST CONDITIONS		IVIIIV	ITP	WAX	נואט
fmax	SH CLK	SER/Q15	CLK	SER/Q15	$R_L = 667 \Omega, C_L = 45 pF$	20	28		MHz
tPHL t	STRCLR	Y0 thru Y15					25	40	
<sup>t</sup> PLH	MODE/	Y0 thru Y15			$R_L = 2 k\Omega$ , $C_L = 15 pF$		28	45	ns
<sup>t</sup> PHL	STRCLK	10 01110 1110					30	45	
tPLH	SH CLK	SH CLK SER/Q15		SER/Q15	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 45 pF		21	33	ns
<sup>t</sup> PHL	L SIT OLIK	0211/010	CLK	0211/013	11 = 007 42, OL = 43 pi		26	40	""
<sup>t</sup> PZH	CS, R/₩	SER/Q15	CS, R/W	SER/Q15	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 45 pF		30	45	ns
<sup>t</sup> PZL	00,11,11	02/1/010	00,11,11	3211/013	11 = 007 12, CL = 43 pi		30	45	113
<sup>t</sup> PHZ	CS, R/W	SER/Q15	CS, R/W	SER/Q15	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 5 pF		25	40	ne
tPLZ	00,11,11	02.1./010	00,.17	0011/013	п_ оо, и, о_ орг		25	40	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



 $<sup>\</sup>ddagger$ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>§</sup> Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

<sup>¶&#</sup>x27;LS673 only.

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# **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-88602013A	Active	Production	LCCC (FK)   28	42   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88602013A SNJ54LS 673FK
5962-8860201JA	Active	Production	CDIP (J)   24	15   TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8860201JA SNJ54LS673J
5962-8860201LA	Active	Production	CDIP (JT)   24	15   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8860201LA SNJ54LS673JT
5962-88607013A	Active	Production	LCCC (FK)   28	42   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88607013A SNJ54LS 674FK
5962-8860701JA	Active	Production	CDIP (J)   24	15   TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8860701JA SNJ54LS674J
SN54LS673J	Active	Production	CDIP (J)   24	15   TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	SN54LS673J
SN54LS673J.A	Active	Production	CDIP (J)   24	15   TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	SN54LS673J
SN54LS674J	Active	Production	CDIP (J)   24	15   TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	SN54LS674J
SN54LS674J.A	Active	Production	CDIP (J)   24	15   TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	SN54LS674J
SN74LS673DW	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS673
SN74LS673DW.A	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS673
SN74LS674DW	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS674
SN74LS674DW.A	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS674
SNJ54LS673FK	Active	Production	LCCC (FK)   28	42   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88602013A SNJ54LS 673FK
SNJ54LS673FK.A	Active	Production	LCCC (FK)   28	42   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88602013A SNJ54LS 673FK
SNJ54LS673J	Active	Production	CDIP (J)   24	15   TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8860201JA SNJ54LS673J



-55 to 125

11-Nov-2025

5962-8860701JA

SNJ54LS674J



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Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	(3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SNJ54LS673J.A	Active	Production	CDIP (J)   24	15   TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8860201JA SNJ54LS673J
SNJ54LS673JT	Active	Production	CDIP (JT)   24	15   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8860201LA SNJ54LS673JT
SNJ54LS673JT.A	Active	Production	CDIP (JT)   24	15   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8860201LA SNJ54LS673JT
SNJ54LS674FK	Active	Production	LCCC (FK)   28	42   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88607013A SNJ54LS 674FK
SNJ54LS674FK.A	Active	Production	LCCC (FK)   28	42   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88607013A SNJ54LS 674FK
SNJ54LS674J	Active	Production	CDIP (J)   24	15   TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-8860701JA SNJ54LS674J

Active

SNJ54LS674J.A

No

Call TI

N/A for Pkg Type

15 | TUBE

Production

CDIP (J) | 24

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# **PACKAGE OPTION ADDENDUM**

www.ti.com 11-Nov-2025

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF SN54LS673, SN54LS674, SN74LS673, SN74LS674:

Catalog: SN74LS673, SN74LS674

Military: SN54LS673, SN54LS674

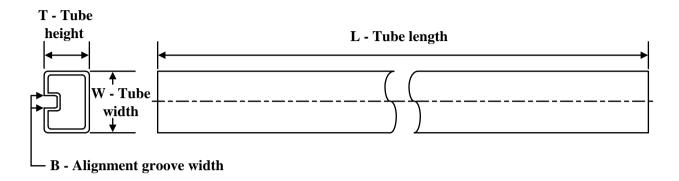
NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 23-May-2025

# **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LS673DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LS673DW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LS674DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LS674DW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R-PDSO-G24)

# PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.

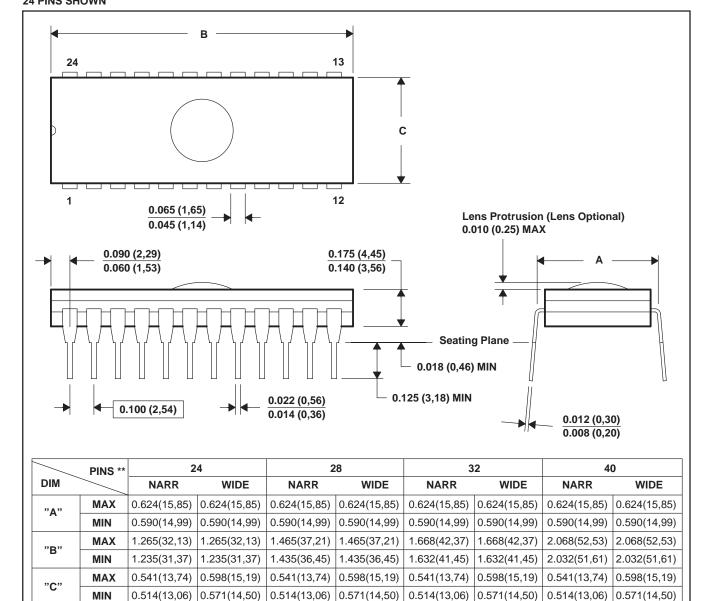


4040084/C 10/97

# J (R-GDIP-T\*\*)

## 24 PINS SHOWN

# **CERAMIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
- D. This package can be hermetically sealed with a ceramic lid using glass frit.
- E. Index point is provided on cap for terminal identification.



# JT (R-GDIP-T\*\*)

#### 24 LEADS SHOWN

## **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

# FK (S-CQCC-N\*\*)

# LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



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