SDLS166 OCTOBER 1976 - REVISED MARCH 1988

Supply Voltage and Ground on Corner Pins To Simplify P-C Board Layout

description

The SN54LS375 and SN74LS375 bistable latches are electrically and functionally identical to the SN54LS75 and SN74LS75, respectively. Only the arrangement of the terminals has been changed in the SN54LS375 and SN74LS375.

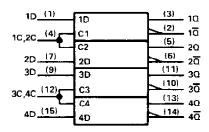
These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable goes high.

All inputs are diode-clamped to minimize transmissionline effects and simplify system design. The SN54LS375 is characterized for operation over the full military temperature range of -55°C to 125°C ; SN74LS375 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH LATCH) INPUTS OUTPUTS D G Q ā I ī Ħ н н н $\underline{\sigma}^{\vec{0}}$ σ^{0} L

 $H = high \ level, \ L = low \ level, \ X = irrelevant.$ Qg = the level of Q before the high-to low transition of C.

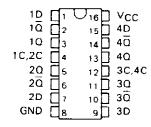
logic symbol[†]



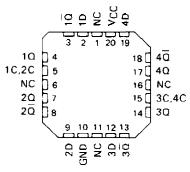
 † This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

SN54LS375 . . . J OR W PACKAGE SN74LS375 . . . D OR N PACKAGE (TOP VIEW)

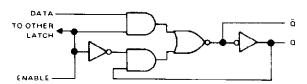


SN54LS375 . . . FK PACKAGE (TOP VIEW)

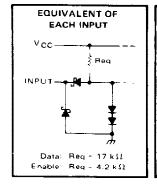


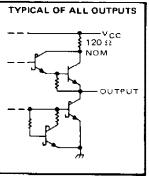
NC - No internal connection

logic diagram (each latch)



schematics of inputs and outputs





PRODUCTION DATA documents centern information current as of publication data. Products conform to specifications per the terms of Taxes Instruments standard warranty. Production processing does not necessarily include testing of all peremeters.



SN54LS375, SN74LS375 4-BIT BISTABLE LATCHES

olute maximum rati <mark>ngs over oper</mark> a	ting fr ee -air	tem	pe	ratı	ure	ran	ıge	(ur	1le:	SS C	th	BIV	vis	n	ote	d)			
Supply voltage, VCC (see Note 1) .											. ,							, .	
Input voltage				,															
Operating free air temperature range:	SN54L5375																-5	5°C	to 12
	SN74LS375																	0°4	C to 7
Storage temperature range				,													-6	5°C	to 15

recommended operating conditions

			SN54LS375			SN74LS375			
		MIN	NOM	NOM MAX		MIN NOM		UNIT	
V _{CC}	Supply voltage	4.5	5	5.5	4,75	5	5.25	V	
VIH	High-lever input voltage	2			2			V	
ViL	Low-level input voltage			0.7			0.8	V	
Юн	High-level autput current			~ 0.4			- 0.4	mA	
^I OL	Low-level output current		•	4			8	mA	
t _w	Width of enabling pulse	20		***************************************	20			ns	
:setup	Setup time	20			20			ns	
thold	Hold time	0			0			пѕ	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DARAMETER	TEST COND		SN54LS	375						
PARAMETER	TEST CONDI	TUNST	MIN TYPE MAX			MIN	TYP‡	MAX	TINU	
ViK	V _{CC} = MIN, 1 ₁ = −18 mA	·			-1.5			- 1.5	V	
Vон	$V_{CC} = MIN, V_{IH} = 2 V,$ $I_{OH} = -0.4 \text{ mA}$	VIL = MAX	2.5	3.5	•	2.7	3.5		٧	
V	VCC = MIN, VIH = 2 V,	IOL = 4 mA		0.25	0.4		0.25		V	
VOL	VIL = MAX	IOL = 8 mA					0.35	0.5	1 *	
	V _{CC} = MAX. V _I = 7 V	D input			0.1			0.1	mA	
11	ACC - MAX: Al - 14	Cinput			0.4			0.4		
,	V _{CC} = MAX V _I = 2.7 V	D input			20			20		
IН	VCC - WAX V - 2.7 0	C input			80	1		80	Α.,	
	14 14 14 14 14	D input			- 0.4			- 0.4	mA	
1 ₁ £	$V_{CC} = MAX$, $V_{\parallel} = 0.4 V$	Cinput			- 16			- 1.6	1 ""^	
1 _{Q5} ;	V _{CC} = MAX	- <u></u>	-20		- 100	-20		- 100	mΑ	
1CC	VCC = MAX. See Note 2			6.3	12		6.3	12	mΑ	

 $[\]dagger$ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, VCC = 5 V, TA = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN TYP	MAX	UNIT
1PL H	D	0		15	27	D.
1PHL				9	17	ns
tPLH .	D	ā	R _L = 2 kΩ.	12	20	ns
tPHL			∩_ 2 K28.	7	15	113
†PLH	 C	o		15	27	
[†] PHL				14	25	ns
1PLH	С	ā		16	30	
[†] PHL				7	15	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



^{\$} All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ C}$.

\$ Not more than one output should be shorted at a time.

NOTE 2 ^{-1}CC is tested with all inputs grounded and all outputs open

11-Nov-2025 www.ti.com

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN54LS375J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS375J
SN54LS375J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS375J
SN74LS375D	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS375
SN74LS375D.A	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS375
SN74LS375N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS375N
SN74LS375N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS375N
SNJ54LS375J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS375J
SNJ54LS375J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS375J

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2025

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS375, SN74LS375:

Catalog: SN74LS375

Military: SN54LS375

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 23-May-2025

TUBE

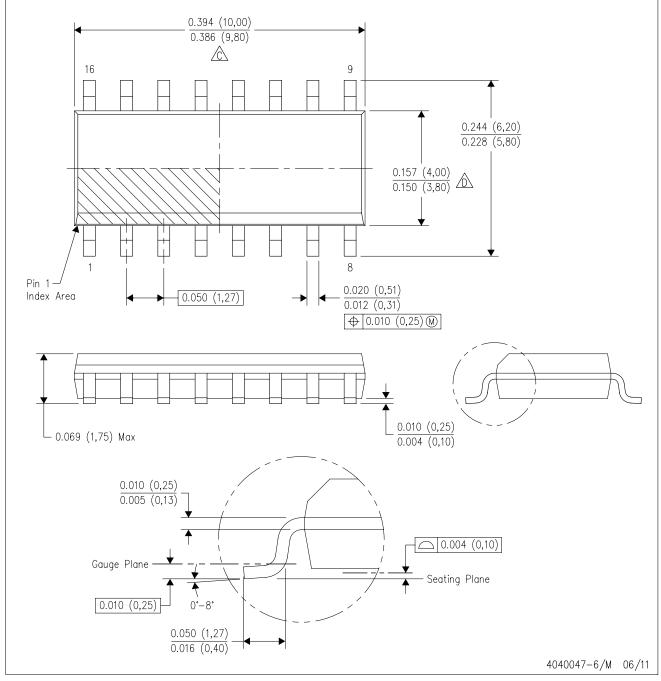


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LS375D	D	SOIC	16	40	507	8	3940	4.32
SN74LS375D.A	D	SOIC	16	40	507	8	3940	4.32
SN74LS375N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS375N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS375N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS375N.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE

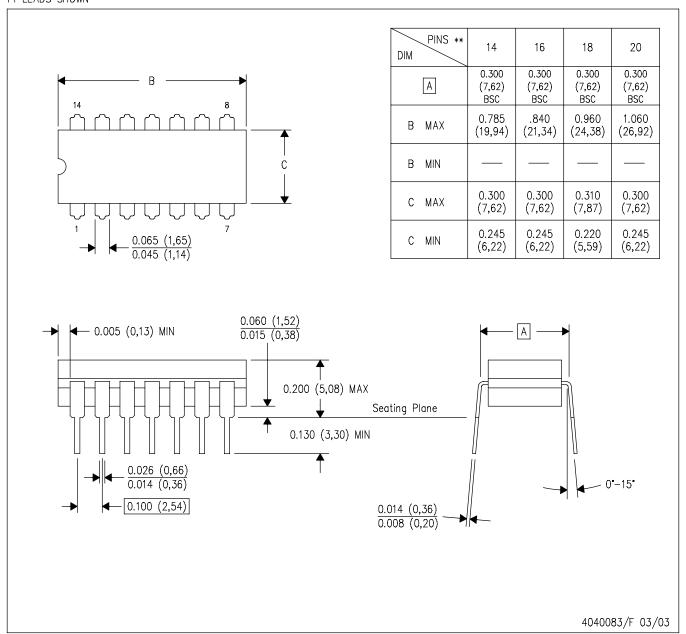


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



14 LEADS SHOWN



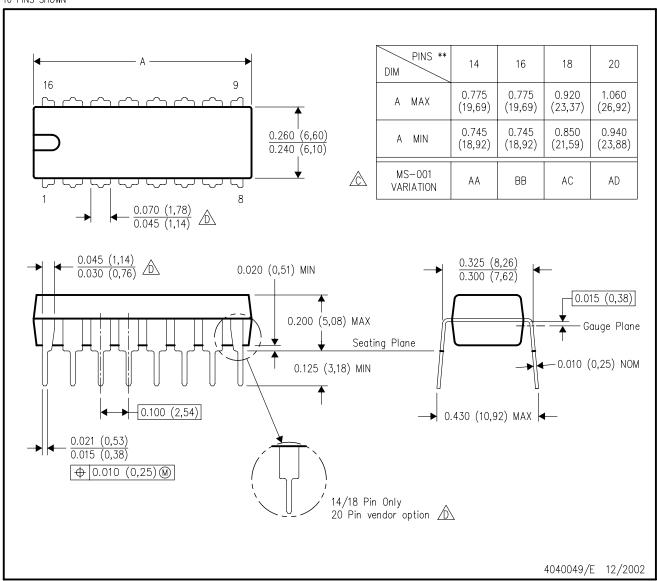
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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