- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operations:

Hold (Store)

Shift Left

Shift Right Load Data

- Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- SN54LS323 and SN74LS323 Are Similar But Have Synchronous Clear
- Applications:

Stacked or Push-Down Registers Buffer Storage, and Accumulator Registers

	GUARANTEED	TYPICAL
TYPE	SHIFT (CLOCK)	POWER
	FREQUENCY	DISSIPATION
'LS299	25 MHz	175 mW
'S299	50 MHz	700 mW

A/QA U7 QA/ U8

CLR 09

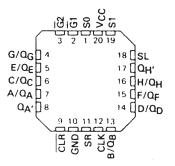
GND 110

14 D/QD

13 □ B/QB

12 CLK

SN54LS299, SN54S299 . . . FK PACKAGE (TOP VIEW)



description

These Schottky TTL eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

FUNCTION TABLE

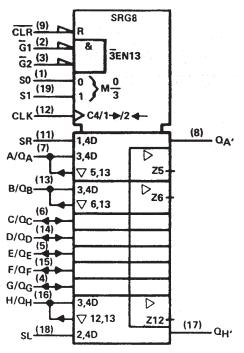
				INPL	ITS						IN	PUTS/0	DUTPU	TS			OUT	PUTS
MODE	CLR	FUNC	TION		TPUT TROL	CLK	SEF	RIAL	A/Q _A	B/QB	c/Q _C	D/QD	E/QE	F/Q _F	G/QG	H/QH	Q _A ,	Q _H ,
		S1	S0	Ğ1 [†]	G2†		SL	SR										
	L	Х	L	L	L	×	Х	Х	L	L	L	L	L	L	L	L	L	, L
Clear	L	L.	Х	L	L	×	X	X	L	L	L	L	L	L	L	L.	L	L
	L	Н	Н	Х	Х	×	x	X	×	X	×	×	X	Х	X	×	L	L
Hold	н	L	Ł	L	°L.	×	X	×	QAO	Q _{B0}	Q _{C0}	a _{D0}	QEO	Q _{F0}	Q _{G0}	αнο	QAO	QHO
71010	н	×	×	L	L	l L	×	×	QAO	Q _{BQ}	σ^{CO}	a_{D0}	σ_{E0}	Q_{F0}			QAO	Q _{H0}
Shift Right	Н	L	Н	L	L	t	X	Н	Н	QAn	QBn	Q _{Cn}	QDn	QEn	QFn	Q_{Gn}	Н	a_{Gn}
Smit mynt	Н	L	н	L	L	1	×	L	L	Q_{An}	QBn	a_{Cn}	a_{Dn}	α_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	Н	Н	L	L	L	1	Н	×	QBn	QCn	QDn	QEn	QFn	QGn	QHn	Н	QBn	Н
Smit Left	н	H	L	L	L	t	L	×	QBn	a_{Cn}	Q_{Dn}	Q_{En}	a_{Fn}	α_{Gn}	Q_{Hn}	L	QBn	L
Load	Н	Н	Н	Х	X	Ť	Х	X	а	Ь.	С	d	e	f	g	h	а	h

[†]When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a...h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

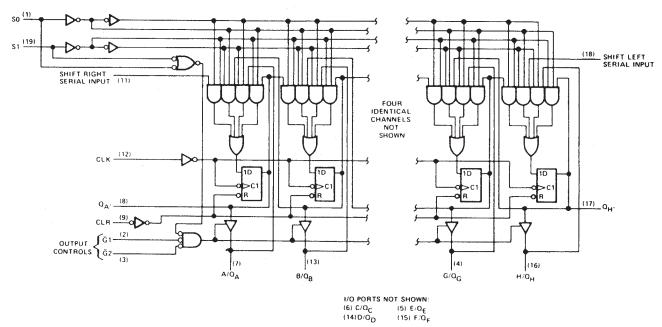


logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, N, and W packages.

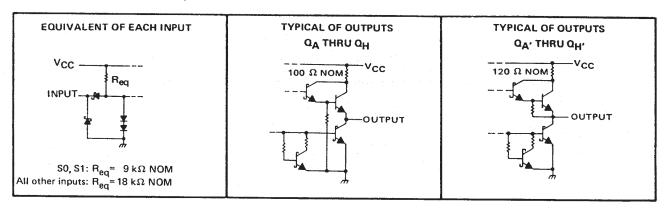
logic diagram (positive logic)



Pin numbers shown are for DW, J, N, and W packages.



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

S	upply voltage, VCC (see Note 1)																					7 V	,
- 1	nput voltage						٠.								٠.							7 V	/
C	ff-state output voltage																				5.	.5 V	,
(perating free-air temperature range:	: S	N5	4L	.S2	99												-5	5°(C to	12	25°C)
_		S	N7	'4L	.S2	99													0	°C 1	o 7	o°C	;
S	torage temperature					٠												-6	5°(Cto	15	o°C	;

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		s	N54LS2	99	s	N74LS2	99	l <u> </u>
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, VCC		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH	QA thru QH	1777		-1	-		-2.6	
output content, TOH	QA' or QH'			-0.4			-0.4	mA
Low-level output current, IOL	Q _A thru Q _H			12			24	
	Q _A ' or Q _H '			4			8	mA
Clock frequency, fclock		0		20	0		20	MHz
Width of clock pulse, tw(clock)	Clock high	30			30			
	Clock low	1.8			10			ns
Width of clear pulse, tw(clear)	Clear low	25			20			ns
	Select	35†			35↑			
Setup time, t _{su}	High-level data [†]	201			20†			
	Low-level data [†]	20↑			201			ns
	Clear inactive-state	241			201			
Hold time, th	Select	10↑			101			
	Data [†]	3†	1977.4		01			ns
Operating free-air temperature, TA		-55		125	0		70	°c

[†] Data includes the two serial inputs and the eight input/output data lines.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST COND	NTIONST	S	N54LS2	99	SI	N74LS2	99	
	- ANAMETER		1EST CONE	ATTONS.	MIN	TYP‡	MAX	MIN	TYP [‡]	MAX	UNIT
VIH	High-level input voltage			-	2			2			V
VIL	Low-level input voltage						0.7			0.8	V
VIK	Input clamp voltage		V _{CC} = MIN,	I _I = -18 mA			-1.5			-1.5	V
Vou	High-level output voltage	Q _A thru Q _H	V _{CC} = MIN,	V _{IH} = 2 V,	2.4	3.2		2.4	3.1		V
VOH	riigiinevei output voitage	QA' or QH'	VIL = VILmax,	IOH = MAX	2.5	3.4		2.7	3.4		\ \
		Q _A thru Q _H	V _{CC} = MIN,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
VOL	Low-level output voltage	ад ши ан	V _{1H} = 2 V,	I _{OL} = 24 mA					0.35	0.5	V
VUL	LOW-level Output Voltage	QA' or QH'	VIH = 2 V, VIL = VILmax	IOL = 4 mA		0.25	0.4		0.25	0.4	1 °
		CA OI CH	AIF - AIFINGY	IOL = 8 mA					0.35	0.5	1
lozh	Off-state output current,	QA thru QH	V _{CC} = MAX,	V _{IH} = 2 V,			40			40	μΑ
·02H	high-level voltage applied	CA UTU CH	V _O = 2.7 V				40			70	μ^
lozL	Off-state output current,	Q _Δ thru Q _H	$V_{CC} = MAX$,	V _{IH} = 2 V,			-400			-400	μА
·02L	low-level voltage applied		V _O = 0.4 V				400				μΛ
	Input current at maximum	S0, S1		V1 = 7 V			200			200	
11	input voltage	A thru H	V _{CC} = MAX	V ₁ = 5.5 V			100			100	μА
	mput vortage	Any other		V ₁ = 7 V			100			100	1
tн	High-level input current	A thru H, SO, S1	V _{CC} = MAX,	V ₁ = 2.7 V			40			40	1
'IH	mgn-lever mput current	Any other	ACC - MAY	V1 - 2.7 V			20			20	μΑ
l _{IL}	Low-level input current	S0, S1	V _{CC} = MAX,	V ₁ = 0.4 V			-0.8			-0.8	
'IL	CON-level input current	Any other	ACC - MWV	V - U.4 V			-0.4			-0.4	mA
loc	Short-circuit output current§	Q _A thru Q _H	\/ \AAA\		-30		130	-30		-130	^
los	Short-circuit output currents	QA' or QH'	V _{CC} = MAX		-20	***************************************	-100	-20		-100	mA
¹ CC	Supply current		V _{CC} = MAX			33	53		33	53	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ} \text{ C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			See Note 2	20	35		MHz
[†] PLH	CLV	0.4000.4	B. = 2 kO		22	33	
^t PHL	CLK	Q _A ' or Q _H '	$R_L = 2 k\Omega$, $C_L = 15 pF$		26	39	ns
^t PHL	CLR	QA' or QH'	1		27	40	ns
^t PLH		Q _A thru Q _H			17	25	
[†] PHL	CLK	da illia da	$R_1 = 665 \Omega$, $C_1 = 45 pF$		26	39	ns
^t PHL	CLR	Q _A thru Q _H	1 11 000 12, 00 10 10		26	40	ns
^t PZH	G1, G2	QA thru QH	7		13	21	
^t PZL	01,02	α _A tina α _H			19	30	ns
^t PHZ	G1, G2	QA thru QH	$R_L = 665 \Omega$, $C_L = 5 pF$		10	20	
^t PLZ] . 31, 32	ZA UITO CH			10	15	ns

 $[\]P_{\mathsf{fmax}} \equiv \mathsf{maximum} \; \mathsf{clock} \; \mathsf{frequency}$



 $^{^{\}ddagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25^{\circ}\text{C}$.

[§]Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

tplH = propagation delay time, low-to-high-level output.

tpHL = propagation delay time, high-to-low-level output

 $t_{PZH} = output$ enable time to high level

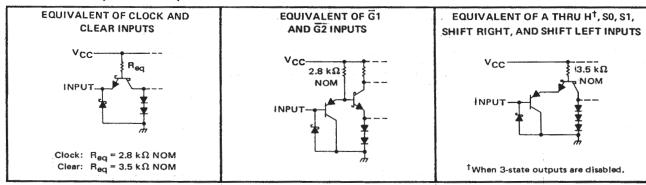
 $t_{PZL} \equiv output$ enable time to low level

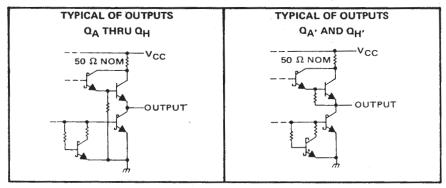
tpHZ ≡ output disable time from high level

 $t_{PLZ} \equiv output disable time from low level$

NOTE 2: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times, Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)
Input voltage
Off-state output voltage
Operating free-air temperature range: SN54S299 (See Note 1)55°C to 125°C
SN74S299 0 °C to 70 °C
Storage temperature range65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			N54S29	9		N74S29	9	
		MIN	NOM	MAX	MIN	NOM	MAX	TINU
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH	QA thru QH			-2			-6.5	
riigii-iever output current, 10H	QA' or QH'			-0.5			-0.5	mA
Low-level output current, IOL	Q _A thru Q _H			20			20	mA
	QA' or QH'			6			6	I IIIA
Clock frequency, fclock		0		50	0		50	MHz
Width of clock pulse, tw(clock)	Clock high	10			10			
	Clock low	10			10			ns
Width of clear pulse, tw(clear)	Clear low	10			10			ns
	Select	15↑			15↑			
Setup time, t _{SU}	High-level data [‡]	7↑			7↑			
Setup time, tsu	Low-level data [‡]	5↑			5↑			ns
	Clear inactive-state	10↑			10↑			
Hold time, th	Select	5↑			51			
Tiold time, th	Data [‡]	5↑			5↑			ns
Operating free-air temperature, TA		-55		125	0		70	°c

[‡] Data includes the two serial inputs and the eight input/output data lines.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
VIK	Input clamp voltage		V _{CC} = MIN,	I _I = -18 mA			-1.2	V
VOH	High-level output voltage	QA thru QH	VCC = MIN,	V _{IH} = 2 V,	2.4	3.2		
*On		QA' or QH'	V1L = 0.8 V,	IOH = MAX	2.7	3.4		٧
VOL	Low-level output voltage		VCC = MIN,	V _{IH} = 2 V,				
- 01			V _{IL} = 0.8 V,	IOL = MAX			0.5	٧
lozh	Off-state output current,	QA thru QH	V _{CC} = MAX,	V _{IH} = 2 V,				
-0211	high-level voltage applied	ag mru ag	V _O = 2.4 V				100	μА
IOZL	Off-state output current,	0 1 1	VCC = MAX,	V _{IH} = 2 V,			-	
-02L	low-level voltage applied	Q _A thru Q _H	V _O = 0.5 V				-250	μА
4	Input current at maximum input voltage		V _{CC} = MAX,	V _I = 5.5 V			1	mA
Ήн	High-level input current	A thru H, SO, S1					100	IIIA
-111		Any other	V _{CC} = MAX,	V ₁ = 2.7 V			50	μА
		CLK or CLR					-2	mA
HL	Low-level input current	S0, S1	VCC = MAX,	V _I = 0.5 V			-500	μΑ
		Any other		· ·			-250	μА
los	Short-circuit output current§	Q _A thru Q _H			-40	1	-100	
-03	Short shi suit output culterity	QA' or QH'	V _{CC} = MAX	ľ	-20		-100	mA
lcc	Supply current		V _{CC} = MAX			140	225	mA

 $^{^\}dagger$ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, VCC = 5 V, TA = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			See Note 2	50	70	· · · · · · · · · · · · · · · · · · ·	MHz
^t PLH	CLK	0.4050.4	D. = 110 C = 15 : 5		12	20	
^t PHL		Q _A ' or Q _H '	$R_{L} = 1 k\Omega$, $C_{L} = 15 pF$		13	20	ns
^t PHL	CLR	QA' or QH'			14	21	ns
^t PLH	CLK	0.450			15	21	
^t PHL		QA thru QH			15	21	ns
tPHL	CLR	QA thru QH	$R_{L} = 280 \Omega$, $C_{L} = 45 pF$		16	24	ns
^t PZH	G1, G2	0 4 0	1		10	18	
^t PZL	G1, G2	QA thru QH			12	18	ns
^t PHZ	Ğ1, Ğ2		$R_1 = 280 \Omega$, $C_1 = 5 pF$	 	7	12	
^t PLZ	31,62	• QA thru QH			7	12	ns

NOTE 2: For testing f_{max} , all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times. Load circuits and voltage waveforms are shown in Section 1.



[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ} \text{C}$.

[§] Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

[¶]f_{max} = maximum clock frequency t_{PLH} = Propagation delay time, low-to-high-level output

tpHL = Propagation delay time, high-to-low-level output

tpzH = output enable time to high level

tpzL = output enable time to low level

tpHZ = output disable time from high level

tpLZ = output disable time from low level

www.ti.com

11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
78024012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	78024012A SNJ54LS 299FK
7802401RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7802401RA SNJ54LS299J
7802401SA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7802401SA SNJ54LS299W
SN54LS299J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS299J
SN54LS299J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS299J
SN74LS299DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS299
SN74LS299DW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS299
SN74LS299N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS299N
SN74LS299N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS299N
SNJ54LS299FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	78024012A SNJ54LS 299FK
SNJ54LS299FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	78024012A SNJ54LS 299FK
SNJ54LS299J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7802401RA SNJ54LS299J
SNJ54LS299J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7802401RA SNJ54LS299J
SNJ54LS299W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7802401SA SNJ54LS299W
SNJ54LS299W.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7802401SA SNJ54LS299W

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2025

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS299, SN74LS299:

Catalog: SN74LS299

Military: SN54LS299

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

www.ti.com 23-May-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
78024012A	FK	LCCC	20	55	506.98	12.06	2030	NA
7802401SA	W	CFP	20	25	506.98	26.16	6220	NA
SN74LS299DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS299DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS299N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS299N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54LS299FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS299FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS299W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54LS299W.A	W	CFP	20	25	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

 D. Index point is provided on cap for terminal identification only.

 E. Falls within Mil—Std 1835 GDFP2—F20



14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025