### **SDLS076**

# SN54195, SN54LS195A, SN54S195, SN74195, SN74LS195A, SN74S195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

MARCH 1974-REVISED MARCH 1988

· Synchronous Parallel Load

- Positive-Edge-Triggered Clocking
- Parallel Inputs and Outputs from Each Flip-Flop
- Direct Overriding Clear
- J and K Inputs to First Stage
- Complementary Outputs from Last Stage
- For Use in High Performance:
   Accumulators/Processors
   Serial-to-Parallel, Parallel-to-Serial
   Converters

### description

These 4-bit registers feature parallel inputs, parallel outputs,  $J \cdot \overline{K}$  serial inputs, shift/load (SH/ $\overline{LD}$ ) control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The register has two modes of operation:

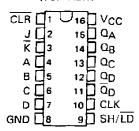
Parallel (broadside) load Shift (in the direction Q<sub>A</sub> toward Q<sub>D</sub>)

Parallel loading is accomplished by applying the four bits of data and taking  $SH/\overline{LD}$  low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

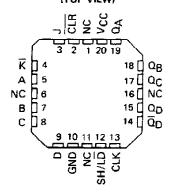
Shifting is accomplished synchronously when SH/ $\overline{\text{LD}}$  is high. Serial data for this mode is entered at the J- $\overline{\text{K}}$  inputs. These inputs permit the first stage to perform as a J- $\overline{\text{K}}$ , D-, or T-type flip-flop as shown in the function table.

The high-performance '\$195, with a 105-megahertz typical maximum shift-frequency, is particularly attractive for very-high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky-clamped shift register.

SN54195, SN54LS195A, SN54S195...J OR W PACKAGE SN74195...N PACKAGE SN74LS195A, SN74S195...D OR N PACKAGE (TOP VIEW)



SN54LS195, SN54S195...FK PACKAGE (TOP VIEW)



NC - No internal connection

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
195	39 MHz	195 mW
'LS195A	39 MHz	70 mW
'\$195	105 MHz	350 mW

### **FUNCTION TABLE**

		INP	UTS							0	UTPU	TS	
CLEAR	SHIFT/	01.001	SEF	IIAL	P.	AR/	<b>ILL</b> I	EL					
CLEAR	LOAD	CLOCK	J	ĸ	Α	В	C	D	QA	Q <sub>B</sub>	QC	σo	QD
L	х	×	х	×	×	×	X	Х	L	L	L	L	Н
н	L	t	х	х	a	ь	c	đ	a	b	c	d	đ
н	н	L	х	х	X	Х	Х	Х	QAO	$\sigma_{B0}$	$\alpha_{CO}$	$\alpha_{D0}$	$\bar{\alpha}_{D0}$
н	н	Ť	L	н	×	Х	X	×	QAD	$\alpha_{A0}$	$\sigma_{Bn}$	$\alpha_{Cn}$	$\overline{\Omega}_{Cn}$
н	H	1	L	L	X	Х	X	X	Ļ	$\mathbf{Q}_{An}$	$\mathbf{Q}_{Bn}$	$o_{Cn}$	ā <sub>Cn</sub>
н	н	1	н	н	х	х	х	Х	н	$\alpha_{An}$	QBn	$\alpha_{Cn}$	$\bar{\alpha}_{Cn}$
н	н	t l	H	L	x	X	x	х	ā <sub>An</sub>	$\mathbf{Q}_{An}$	QBn	$Q_{Cn}$	$\bar{\alpha}_{Cn}$

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

† = transition from low to high level

a, b, c, d = the level of steady-state input at A, B, C, or D, respectively

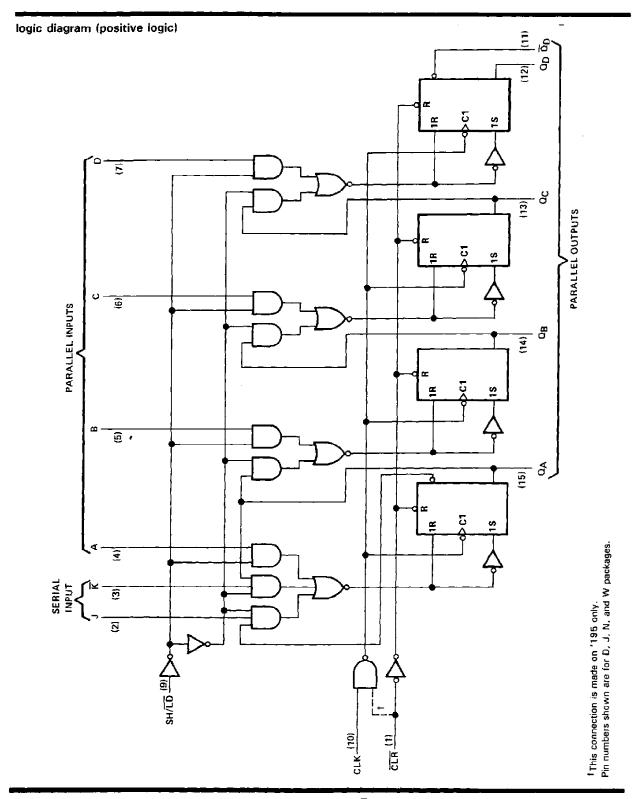
 $Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}$  = the level of  $Q_{A}, Q_{B}, Q_{C}$  or  $Q_{D}$ , respectively, before the indicated steady state input conditions

were established  $\alpha_{An}, \alpha_{Bn}, \alpha_{Cn}$  = the level of  $\alpha_{A}, \alpha_{B}$ , or  $\alpha_{C}$ ,

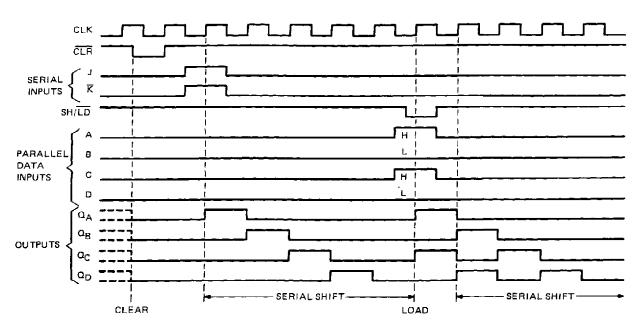
respectively, before the mostrecent transition of the clock

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

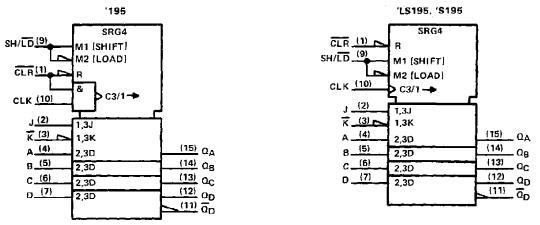




# typical clear, shift, and load sequences



# logic symbols†

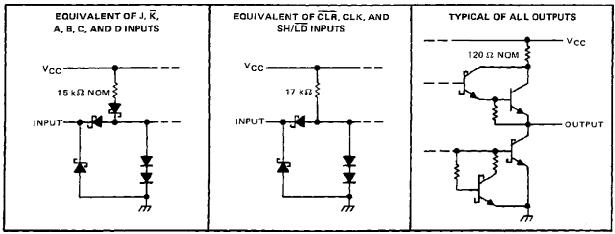


 $^7$ These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers are for D, J, N, and W packages.

# SN54195, SN54LS195A, SN54S195, SN74195, SN74LS195A, SN74S195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

# Schematics of inputs and outputs EQUIVALENT OF EACH INPUT TYPICAL OF ALL OUTPUTS VCC INPUT Clock input: Req = 4 kΩ NOM All other inputs: Feq = 6 kΩ NOM

'LS195A



S195

EQUIVALENT OF EACH INPUT

TYPICAL OF ALL OUTPUTS

VCC

50 Ω NDM

OUTPUT

CLR, SH/LD: Req = 4 kΩ NOM

All other inputs: Req = 2.8 kΩ NOM



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)						: .			,		7 V
Input voltage	<i></i>										5.5 V
Operating free-air temperature range:	SN54195										-55°C to 125°C
	SN74195	 									. 0°C to 70°C
Storage temperature range		 									-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

# recommended operating conditions

<del></del> -			SN5419	5	$\Box$	SN7419	5	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, VCC		4.5	5	5.5	4.75	5	5.25	٧
High-level output current, IOH				-800			-800	μА
Low-level output current, IQL				16			16	mA
Clock frequency, fclock		0		30	0		30	MHz
Width of clock input pulse, tw(clock)		16			16			пВ
Width of clear input pulse, tw(clear)		12			12			ns
	Shift/load	25			25			
Setup time, t <sub>su</sub> (see Figure 1)	Serial and parallel data	20			20			ns
	Clear inactive-state	25			25			
Shift/load release time, t <sub>release</sub> (see Figure 1)				10			10	n\$
Serial and parallel data hold time, th (see Figure 1)		0			0			ns
Operating free-air temperature, TA		-55		125	0		70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYPI	MAX	UNIT
ViH	High-level input voltage		2			V
VIL	Low-level input voltage			•	0.8	V
VIK	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 m <sup>2</sup>			-1.5	V
νон	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -800	μA 2.4	3.4		V
VOL	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V. I <sub>OL</sub> = 16 m/		0.2	0.4	V
T <sub>1</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>1</sub> = 5.5 V			1	mA
ЧН	High-level input current	V <sub>CC</sub> = MAX, V <sub>1</sub> = 2.4 V			40	μА
IIL	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-1.6	mA
loc	Short-circuit output current§	VCC = MAX SN5	19520		-57	
los_	Short-chedit bothot continu	VCC - MAA SN74	195 – 18		-57	mA
tcc	Supply current	V <sub>CC</sub> = MAX, See Note 2		39	63	mΑ

 $<sup>^\</sup>dagger$  For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions,

## switching characteristics, VCC = 5 V, TA = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
fmax	Maximum clock frequency	C <sub>1</sub> = 15 pF,	30	39		MHz
<sup>‡</sup> PHL	Propagation delay time, high-to-low-level output from clear	1 _ <del>-</del> i		19	30	Π5
<sup>t</sup> PLH	Propagation delay time, low-to-high-level output from clock	$R_{\perp} = 400 \Omega$ , See Figure 1		14	22	ns
tPHL	Propagation delay time, high-to-low-level output from clock	See Figure 1		17	26	ns



<sup>‡</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>§</sup>Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J. K, and data inputs. I<sub>CC</sub> is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

# SN54LS195A, SN74LS195A 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)			 	 				7 V
Input voltage			 	 				7 V
Operating free-air temperature range:	SN54LS195A		 	 				-55°C to 125°C
	SN74LS195A	,	 	 				0°C to 70°C
Storage temperature range			 	 				-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

### recommended operating conditions

		Si	154LS1	95A	SN	174LS1	95A	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
Supply voltage, VCC	· · · · · · · · · · · · · · · · · · ·	4.5	5	5,5	4.75	5	5.25	V
High-level output current, IOH				-400			-400	μА
Low-level output current, IOL		1		4			8	mA
Clock frequency, f <sub>clock</sub>		0		30	0		30	MHz
Width of clock or clear pulse, tw(clock)		16			16			ns
Width of clear input pulse, tw(clear)		12			12			ns
	Shift/load	25			25			
Setup time, t <sub>su</sub> (see Figure 1)	Serial and parallel data	15			15			ns
	Clear inactive-state	25			25			
Shift/load release time, t <sub>release</sub> (see Figure 1)				10			20	ns
Serial and parallel data hold time, th (see Figure 1)		0			0			ns
Operating free-air temperature, TA		-65		125	0		70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DAD ALLETED		ST CONDITIO	auct	SN	54LS19	5A	SN	74LS19	5A	
	PARAMETER	16.	SI COMDITIE	. 6817	MIN	TYP <sup>‡</sup>	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage	1			2			2			V
VIL	Low-level input voltage						0.7			0.8	V
VIK	Input clamp voltage	V <sub>CC</sub> = MIN,	lj = -18 mA		T		-1.5			<b>⊸1.5</b>	V
Vон	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = V <sub>IL</sub> max,	V <sub>IH</sub> = 2 V, I <sub>OH</sub> = -400	μΑ	2.5	3.4		2.7	3.4		٧.
1.		VCC = MIN,	V <sub>IH</sub> = 2 V,	I <sub>OL</sub> = 4 mA		0.25	0.4		0.25	0.4	V
AOL	Low-level output voltage	VIL = VIL max		IOL = 8 mA					0.35	0.5	•
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX,	V1 = 7 V				0.1			0.1	mA
44	High-level input current	VCC = MAX.	V <sub>1</sub> = 2.7 V				20			20	μА
1 <sub>1</sub> L	Low-level input current	VCC - MAX,	V <sub>I</sub> = 0.4 V				-0.4			-0.4	mA
los	Short-circuit output current §	V <sub>CC</sub> = MAX			-20		-100	-20		-100	mΑ
lcc	Supply current	V <sub>CC</sub> = MAX,	See Note 2			14	21		14	21	mA

<sup>&</sup>lt;sup>1</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# switching characteristics, VCC = 5 V, TA = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub> Maximum clack frequency	C <sub>1</sub> = 15 pF,	30	39		MHz
tPHL Propagation delay time, high-to-low-level output from clear	$R_1 = 2 k\Omega$		19	30	ns
tpLH Propagation delay time, low-to-high-level output from clock	See Figure 1		14	22	ns
tPHL Propagation delay time, high-to-low-level output from clock	Gee ( igure )		17	26	ns



<sup>\*</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25 C.

Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second,

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J. K, and data inputs, I<sub>CC</sub> is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground.

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1) .											7 V
Input voltage											
Operating free-air temperature range:	SN54S195										-55°C to 125°C
	SN74S195						 ,				. 0°C to 70°C
Storage temperature range									_		~65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

· · · · · · · · · · · · · · · · · · ·		S	N54S19	95	S	N74S19	95	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	OIST
Supply voltage, VCC		4.5	5	5.5	4.75	- 5	5.25	V
High-level output current, IOH	- <del></del>			-1			-1	mA
Low-level output current, IOL		1		20		·	20	mA
Clock frequency, f <sub>clock</sub>		0		70	0		70	MHz
Width of clock input pulse, tw(clock)		7			7			nş
Width of clear input pulse, tw(clear)		12	-		12			пş
	Shift/load	11			11			
Setup time, t <sub>su</sub> (see Figure 1)	Serial and parallel data	5			5			ns
	Clear inactive-state	9			9			
Shift/load release time, t <sub>release</sub> (see Figure 1)		1		2			6	ns
Serial and parallel data hold time, th (see Figure 1)		3			3			ns
Operating free-air temperature, TA		55		125	0		70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	1	TEST CONDITION	NST	MIN	TYP‡	MAX	UNIT
V <sub>IH</sub>	High-level input voltage				2			V
VIL	Low-level input voltage						8.0	٧
ViK	Input clamp voltage	VCC = MIN,	I <sub>I</sub> = -18 mA				-1.2	V
		V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V,	SN54S195	2.5	3.4		v
Vон	High-level output voltage	V <sub>IL</sub> = 0.8 V,	IOH = -1 mA	SN74S195	2.7	3.4		<b>_</b> _
		V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V,				0.5	V
VOL	Low-level output voltage	VIL = 0.8 V,	VIL = 0.8 V, IOL = 20 mA		ŀ		0.5	
1 <sub>1</sub>	Input current at maximum input voltage	V <sub>CC</sub> - MAX,	V <sub>1</sub> = 5.5 V				1	mA
ин	High-level input current	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.7 V				50	μА
IIL	Low-level input current	V <sub>CC</sub> = MAX.	V <sub>I</sub> = 0.5 V				-2	mΑ
los	Short-circuit output current §	V <sub>CC</sub> = MAX			-40		-100	mΑ
		V <sub>CC</sub> = MAX,	See Nee 2	SN54S195		70	99	
icc	Supply current		See Note 2	SN74S195		70	109	mΑ

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

## switching characteristics, VCC = 5 V, TA = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub> Maximum clock frequency	C <sub>1</sub> = 15 pF,	70	105		MHz
tpht Propagation delay time, high-to-low-level output from clear	R <sub>1</sub> = 280 Ω,		12.5	18.5	ns
tPLH Propagation delay time, low-to-high-level output from clock	See Figure 1		8	12	ns
tpHL Propagation delay time, high-to-low-level output from clock	Des l'igure i		11	16.5	F15

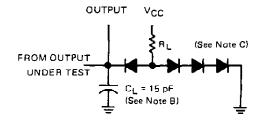


 $<sup>\</sup>ddagger$ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_{A} = 25^{\circ}\text{C}$ .

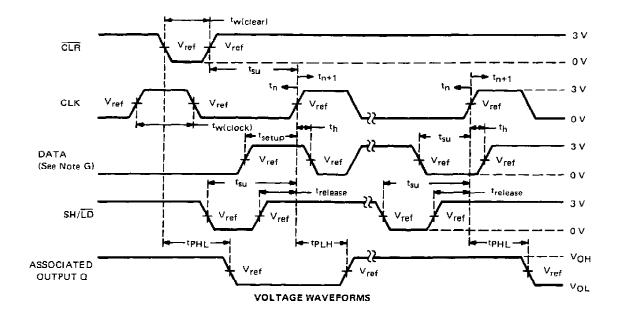
Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J. K, and data inputs, I<sub>CC</sub> is measured by applying a momentary ground, followed by 4.5 V, to clear, and then applying a momentary ground, followed by 4.5 V, to clock.

## PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST



NOTES: A. The clock pulse generator has the following characteristics:  $Z_{\text{out}} \approx 50~\Omega$  and PRR  $\leq$  1 MHz. For '195,  $t_{\text{f}} \leqslant$  7 ns and  $t_{\text{f}} \leqslant$  7 ns, For 'LS195A,  $t_{\text{f}} \leqslant$  15 ns and  $t_{\text{f}} \leqslant$  6 ns. For 'S195,  $t_{\text{f}} \approx$  2.5 ns and  $t_{\text{f}} =$  2.5 ns. When testing  $f_{\text{max}}$ , vary the clock PRR.

- B. C<sub>1</sub> includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.
- D. A clear pulse is applied prior to each test.
- E. For '195 and 'S195,  $V_{ref} = 1.5 V$ ; for 'LS195A,  $V_{ref} = 1.3 V$ .

  F. Propagation delay times (tplH and tpHL) are measured at  $t_{n+1}$ . Proper shifting of data is verified at  $t_{n+4}$  with a functional test.
- G. J and K inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.
- H.  $t_n$  = bit time before clocking transition.
  - t<sub>n+1</sub> = bit time after one clocking transition.
  - t<sub>n+4</sub> = bit time after four clocking transitions.

FIGURE 1-SWITCHING TIMES



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### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
	` '				, ,	(4)	(5)		. ,
JM38510/30602B2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30602B2A
JM38510/30602B2A.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30602B2A
JM38510/30602BEA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30602BEA
JM38510/30602BEA.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30602BEA
M38510/30602B2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30602B2A
M38510/30602BEA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30602BEA
SN54LS195AJ	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS195AJ
SN54LS195AJ.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS195AJ
SNJ54LS195AJ	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS195AJ
SNJ54LS195AJ.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS195AJ

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# **PACKAGE OPTION ADDENDUM**

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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# **PACKAGE MATERIALS INFORMATION**

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# **TUBE**



## \*All dimensions are nominal

	Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
	JM38510/30602B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
I	JM38510/30602B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
ĺ	M38510/30602B2A	FK	LCCC	20	55	506.98	12.06	2030	NA

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



**INSTRUMENTS** www.ti.com

## 14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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