







SN54HCT74, SN74HCT74 SCLS169G - DECEMBER 1982 - REVISED OCTOBER 2022

SNx4HCT74 Dual D-Type Positive-Edge-Triggered Flip-Flips With Clear and Preset

1 Features

- Operating voltage range of 4.5 V to 5.5 V
- Outputs can drive up to 10 LSTTL loads
- Low power consumption, 40-µA max I_{CC}
- Typical $t_{pd} = 17 \text{ ns}$
- ±4-mA output drive at 5 V
- Low input current of 1 µA max
- Inputs are TTL-voltage compatible

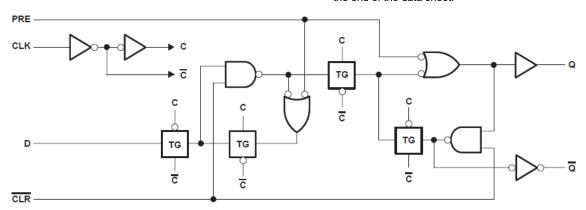
2 Description

The 'HCT74 devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

Device Information

| - | | | | | | | | | | | | |
|--------------|------------------------|--------------------|--|--|--|--|--|--|--|--|--|--|
| PART NUMBER | PACKAGE ⁽¹⁾ | BODY SIZE (NOM) | | | | | | | | | | |
| SN74HCT74D | SOIC (14) | 8.65 mm × 3.90 mm | | | | | | | | | | |
| SN74HCT74DB | SSOP (14) | 6.20 mm × 5.30 mm | | | | | | | | | | |
| SN74HCT74N | PDIP (14) | 19.31 mm × 6.35 mm | | | | | | | | | | |
| SN74HCT74NS | SO (14) | 10.20 mm × 5.30 mm | | | | | | | | | | |
| SN74HCT74PW | TSSOP (14) | 5.00 mm × 4.40 mm | | | | | | | | | | |
| SNJ54HCT74FK | LCCC (20) | 8.89 mm × 8.45 mm | | | | | | | | | | |
| SNJ54HCT74W | CFP (14) | 9.21 mm × 6.29 mm | | | | | | | | | | |
| SNJ54HCT74J | CDIP (14) | 19.55 mm × 6.71 mm | | | | | | | | | | |

For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram



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3 Revision History

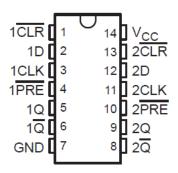
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (February 2022) to Revision G (October 2022)

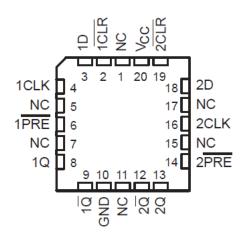
• Changed RθJA for packages: D (86 to 138.7); N (80 to 61.1); NS (76 to 88.4); PW (113 to 114.7)......4



4 Pin Configuration and Functions



J, W, D, DB, N, NS, or PW package 14-Pin CDIP, CFP, SOIC, SSOP, PDIP, SO, or TSSOP Top View



NC - No internal connection

FK Package 20-Pin LCCC Top View



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | · | MIN | MAX | UNIT | |
|------------------|---|-----------------------------|-------------|------|------|--|
| V _{CC} | Supply voltage range | Supply voltage range | | | | |
| I _{IK} | Input clamp current ⁽²⁾ | $V_I < 0$ or $V_I > V_{CC}$ | | ± 20 | mA | |
| I _{OK} | Output clamp current ⁽²⁾ | $V_O < 0$ or $V_O > V_{CC}$ | | ± 20 | mA | |
| Io | Continuous output current | $V_O = 0$ to V_{CC} | | ± 25 | mA | |
| | Continuous current through V _{CC} or GND | | | ± 50 | mA | |
| TJ | Junction temperature | | | 150 | °C | |
| T _{stg} | Storage temperature range | | – 65 | 150 | °C | |

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | SN54HCT74 ⁽²⁾ | | | SN | 74HCT74 | | UNIT |
|-----------------|---------------------------------|----------------------------------|--------------------------|-----|-----------------|-----|---------|-----------------|------|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | UNII |
| V _{CC} | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V _{IH} | High-level input voltage | V _{cc} = 4.5 V to 5.5 V | 2 | | | 2 | | | V |
| V _{IL} | Low-level input voltage | V _{cc} = 4.5 V to 5.5 V | | | 0.8 | | | 0.8 | V |
| VI | Input voltage | | 0 | | V _{CC} | 0 | | V _{CC} | V |
| Vo | Output voltage | | 0 | | V _{CC} | 0 | | V _{CC} | V |
| Δt/Δν | Input transition rise/fall time | | | | 500 | | | 500 | ns |
| T _A | Operating free-air temperatu | re | -55 | | 125 | -40 | | 85 | °C |

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.3 Thermal Information

| | | D (SOIC) | DB (SSOP) | N (PDIP) | NS (SO) | PW (TSSOP) | |
|------------------------|---|----------|-----------|----------|---------|------------|------|
| THERMAL | . METRIC | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | UNIT |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance ⁽¹⁾ | 138.7 | 109.8 | 61.1 | 88.4 | 114.7 | °C/W |
| R _{θJC (top)} | Junction-to-case (top) thermal resistance | 93.8 | 54.7 | 48.9 | 46 | 44.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 94.7 | 58.6 | 40.9 | 48.9 | 57.6 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 49.1 | 15.5 | 28.5 | 13.8 | 4.8 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 94.3 | 58 | 40.6 | 48.4 | 57 | °C/W |
| R _{0JC (bot)} | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | N/A | °C/W |

For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽²⁾ SN54HCT74 is in product preview.



5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CO | TEST CONDITIONS | | T | _A = 25°C | | SN54HCT74 ⁽²⁾ | | SN74HCT74 | | UNIT |
|----------------------|--|--------------------------|-----------------|------|---------------------|------|--------------------------|-------|-----------|-------|------|
| PARAMETER | 1231 00 | NDITIONS | V _{cc} | MIN | TYP | MAX | MIN | MAX | MIN | MAX | ONIT |
| V | | I _{OH} = -20 μA | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | V |
| V _{OH} | $V_{I} = V_{IH} \text{ or } V_{IL}$ | $I_{OH} = -4 \text{ mA}$ | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | V |
| V | V = V or V | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | V |
| V OL | V_{OL} $V_I = V_{IH} \text{ or } V_{IL}$ | $I_{OL} = 4 \text{ mA}$ | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | V |
| I _I | $V_I = V_{CC}$ or 0 | | 5.5 V | | ±0.1 | ±100 | | ±1000 | , | ±1000 | nA |
| I _{CC} | $V_i = V_{CC} \text{ or } 0,$ | I _O = 0 | 5.5 V | | | 4 | | 80 | , | 40 | μΑ |
| ΔI _{CC} (1) | One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC} | | 5.5 V | | 1.4 | 2.4 | | 3 | | 2.9 | mA |
| C _i | | | 4.5 V to 5.5 V | | 3 | 10 | | 10 | | 10 | pF |

- (1) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.
- (2) SN54HCT74 is in product preview.

5.5 Timing Requirements

overrecommended operating free-air temperature range (unless otherwise noted)

| | | | v | T _A = 2 | 5°C | SN54HC | T74 ⁽¹⁾ | SN74HC | T74 | UNIT | |
|------------------------------------|---------------------------|-----------------------|-----------------|--------------------|-----|--------|--------------------|--------|-----|---------|--|
| | | | V _{cc} | MIN | MAX | MIN | MAX | MIN | MAX | ONII | |
| f _{clock} Clock frequency | | | 4.5 V | | 27 | | 18 | | 22 | MHz | |
| f _{clock} | Clock frequency | | 5.5 V | | 30 | | 20 | | 24 | IVII IZ | |
| t _w Pulse duration | PRE or CLR low | 4.5 V | 16 | | 24 | | 20 | | | | |
| | Pulse duration | PRE OF CER IOW | 5.5 V | 14 | | 21 | | 18 | | ns | |
| | r dise duration | CLK high or low | 4.5 V | 18 | | 27 | | 23 | | | |
| | | | 5.5 V | 16 | | 24 | | 21 | | | |
| | | Data | 4.5 V | 12 | | 18 | | 15 | | | |
| | Setup time before CLK↑ | | 5.5 V | 11 | | 16 | | 14 | | 20 | |
| t _{su} | Setup time before CLN | PRE or CLR inactive | 4.5 V | 0 | | 0 | | 0 | | ns | |
| | | FIXE OF CERT INACTIVE | 5.5 V | 0 | | 0 | | 0 | | | |
| | Hold time data after CLK | 4# CI VA | | 0 | | 0 | | 0 | | | |
| t _h | Hold time, data after CLK | | 5.5 V | 0 | | 0 | | 0 | | ns | |

(1) SN54HCT74 is in product preview.



5.6 Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Parameter Measurement Information)

| PARAMETER | FROM | то | V _{cc} | T | = 25°C | | SN54HCT74 ⁽¹⁾ | | SN74HCT74 | | UNIT |
|------------------|------------|------------------------------|-----------------|-----|--------|-----|--------------------------|-----|-----------|-----|---------|
| PARAMETER | (INPUT) | (OUTPUT) | ▼CC | MIN | TYP | MAX | MIN | MAX | MIN | MAX | ONIT |
| f | | | 4.5 V | 27 | 40 | | 18 | | 22 | | MHz |
| f _{max} | | | 5.5 V | 30 | 46 | | 20 | | 24 | | IVII IZ |
| | PRE or CLR | Q or $\overline{\mathbb{Q}}$ | 4.5 V | | 21 | 35 | | 53 | | 44 | |
| | FRE OF CER | QUIQ | 5.5 V | | 17 | 31 | | 48 | | 40 | ns |
| t _{pd} | CLIK | CLK Q or Q | 4.5 V | | 20 | 28 | | 42 | | 35 | 115 |
| | CLK | | 5.5 V | | 18 | 25 | | 38 | | 31 | |
| | | O or $\overline{\square}$ | 4.5 V | | 8 | 15 | | 22 | | 19 | no |
| t _t | | Q or Q | 5.5 V | | 7 | 14 | | 20 | | 17 | ns |

⁽¹⁾ SN54HCT74 is in product preview.

5.7 Operating Characteristics

T_A = 25°C

| | PARAMETER | TEST CONDITIONS | TYP | UNIT |
|-----------------|---|-----------------|-----|------|
| C _{pd} | Power dissipation capacitance per flip-flop | No load | 35 | pF |

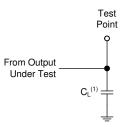


6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_t < 6 ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs

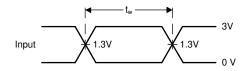


Figure 6-2. Voltage Waveforms, TTL-Compatible CMOS Inputs Pulse Duration

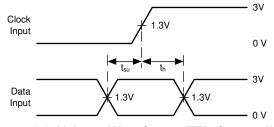
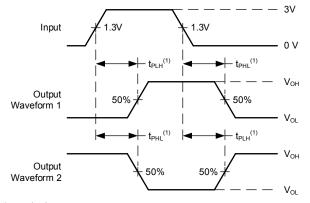


Figure 6-3. Voltage Waveforms, TTL-Compatible CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

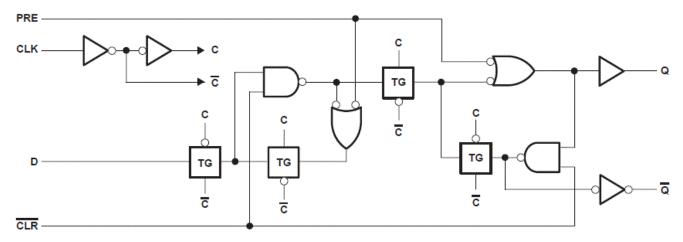
Figure 6-4. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

7 Detailed Description

7.1 Overview

The 'HCT74 devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) inputs sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

7.2 Functional Block Diagram



7.3 Device Functional Modes

Table 7-1. Function Table

| | INP | OUTPUT | | | | | | | | | |
|-----|-----|--------|---|------------------|------------------|--|--|--|--|--|--|
| PRE | CLR | CLK | D | Q | Q | | | | | | |
| L | Н | Х | Х | Н | L | | | | | | |
| Н | L | Х | Х | L | Н | | | | | | |
| L | L | Х | Х | H ⁽¹⁾ | H ⁽¹⁾ | | | | | | |
| Н | Н | 1 | Н | Н | L | | | | | | |
| Н | Н | 1 | L | L | Н | | | | | | |
| Н | Н | L | Х | Q ₀ | Q ₀ | | | | | | |

(1) This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.



8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.2 Layout

8.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type | Package Pins | Package qty Carrier | RoHS | Lead finish/ Ball material | MSL rating/ Peak reflow | Op temp (°C) | Part marking (6) |
|-----------------------|------------|---------------|-----------------|-----------------------|------|-------------------------------|----------------------------|--------------|----------------------|
| JM38510/65352B2A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65352B2A |
| JM38510/65352B2A.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65352B2A |
| JM38510/65352BCA | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65352BCA |
| JM38510/65352BCA.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65352BCA |
| JM38510/65352BDA | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65352BDA |
| JM38510/65352BDA.A | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65352BDA |
| M38510/65352B2A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65352B2A |
| M38510/65352BCA | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65352BCA |
| M38510/65352BDA | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65352BDA |
| SN74HCT74D | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | -40 to 85 | HCT74 |
| SN74HCT74DBR | Active | Production | SSOP (DB) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT74 |
| SN74HCT74DBR.A | Active | Production | SSOP (DB) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT74 |
| SN74HCT74DR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | HCT74 |
| SN74HCT74DR.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT74 |
| SN74HCT74DRE4 | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT74 |
| SN74HCT74DRE4.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT74 |
| SN74HCT74N | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HCT74N |
| SN74HCT74N.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HCT74N |
| SN74HCT74NE4 | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HCT74N |
| SN74HCT74NSR | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT74 |
| SN74HCT74NSR.A | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT74 |
| SN74HCT74PW | Obsolete | Production | TSSOP (PW) 14 | - | - | Call TI | Call TI | -40 to 85 | HT74 |

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| Orderable part number | Status | Material type | Package Pins | Package qty Carrier | RoHS | Lead finish/ Ball material | MSL rating/ Peak reflow | Op temp (°C) | Part marking (6) |
|-----------------------|--------|---------------|-----------------|-----------------------|------|-------------------------------|----------------------------|--------------|------------------|
| | (., | (=) | | | (0) | (4) | (5) | | (0) |
| SN74HCT74PWR | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | HT74 |
| SN74HCT74PWR.A | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT74 |
| SN74HCT74PWRG4 | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT74 |

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HCT74, SN74HCT74:

Catalog: SN74HCT74

Military: SN54HCT74

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications



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TAPE AND REEL INFORMATION





| A0 | Dimension designed to accommodate the component width |
|----|---|
| В0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|-----------------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| SN74HCT74DBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74HCT74DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCT74DRE4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCT74NSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HCT74PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HCT74PWRG4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HCT74PWRG4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |



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*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HCT74DBR | SSOP | DB | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74HCT74DR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74HCT74DRE4 | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74HCT74NSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74HCT74PWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HCT74PWRG4 | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HCT74PWRG4 | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |



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TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|--------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| JM38510/65352B2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| JM38510/65352B2A.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| JM38510/65352BDA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| JM38510/65352BDA.A | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| M38510/65352B2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| M38510/65352BDA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74HCT74N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HCT74N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HCT74N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HCT74N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HCT74NE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HCT74NE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4040083-5/G





CERAMIC DUAL IN LINE PACKAGE



- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
 Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
 Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE INTEGRATED CIRCUIT



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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