







**SN54HCT04, SN74HCT04** 

SCLS042F - JULY 1986 - REVISED OCTOBER 2022

## **SNx4HCT04 Hex Inverters**

#### 1 Features

- Operating voltage range of 4.5V to 5.5V
- Outputs can drive up to 10 LSTTL loads
- Low power consumption, 20-µA max I<sub>CC</sub>
- Typical  $t_{pd}$  = 13ns
- ±4-mA output drive at 5V
- Low input current of 1µA max
- Inputs are TTL-Voltage compatible

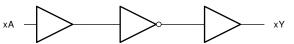
### 2 Description

These devices contain six independent inverters. They perform the Boolean function  $Y = \overline{A}$  in positive logic.

## **Device Information**(1)

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PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HCT04PW	TSSOP (14)	5.00 mm × 4.40 mm
SN74HCT04D	SOIC (14)	8.65 mm × 3.90 mm
SN74HCT04N	PDIP (14)	19.31 mm × 6.35 mm
SN74HCT04NSR	SO (14)	10.20 mm × 5.30 mm
SNJ54HCT04FK	LCCC (20)	8.89 mm × 8.89 mm
SNJ54HCT04J	CDIP (14)	19.55 mm × 6.71 mm

For all available packages, see the orderable addendum at the end of the data sheet.



**Functional Block Diagram** 



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<b>3 Revision History</b> NOTE: Page numbers for previous revisions may differ t	rom page numbers in the current version.
Changes from Revision E (February 2022) to Revision	on F (October 2022) Page
<ul> <li>Increased RθJA for packages: D (86 to 138.7); N (80</li> </ul>	to 62.7); NS (76 to 90.9); PW (113 to 117.6)4

## Changes from Revision D (July 2003) to Revision E (February 2022)

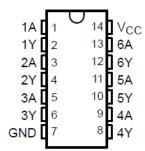
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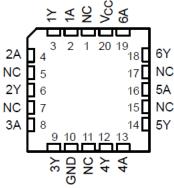
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## **4 Pin Configuration and Functions**



J, D, N, NS, or PW Package 14-Pin CDIP, SOIC, PDIP, SO, or TSSOP Top View



FK Package 20-Pin LCCC Top View

## **5 Specifications**

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	$(V_1 < 0 \text{ or } V_1 > V_{CC})$		±20	mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	$(V_O < 0 \text{ or } V_O > V_{CC})$		±20	mA
Io	Continuous output current	(V <sub>O</sub> = 0 to V <sub>CC</sub> )		±25	mA
V <sub>CC</sub> or GND	Continuous current through Vo	c or GND		±50	mA
TJ	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 5.2 Recommended Operating Conditions<sup>(1)</sup>

			SN	SN54HCT04			SN74HCT04			
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
V <sub>CC</sub> Supply voltage				5	5.5	4.5	5	5.5	V	
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2			2			V	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V			0.8			0.8	V	
VI	Input voltage		0		V <sub>CC</sub>	0		V <sub>CC</sub>	V	
V <sub>O</sub> Output voltage			0		V <sub>CC</sub>	0		V <sub>CC</sub>	V	
Δt/Δv Input transition rise/fall time					500			500	ns	
T <sub>A</sub>	T <sub>A</sub> Operating free-air temperature				125	-40		85	°C	

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating SMOS Inputs, literature number SCBA004.

#### 5.3 Thermal Information

		D (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	
THERMAL	METRIC	14 PINS	14 PINS	14 PINS	14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>	138.7	62.7	90.9	117.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.8	50.5	48.5	46.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	42.5	51.5	60.6	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	49.1	30.1	15.9	5.6	°C/W
ΨЈВ	Junction-to-case (bottom) thermal resistance	94.3	42.2	51	60	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

Product Folder Links: SN54HCT04 SN74HCT04

<sup>(2)</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



#### **5.4 Electrical Characteristics**

	PARAMETER	TEST CONDITIONS(1)	V <sub>cc</sub>	T,	<sub>A</sub> = 25°C		SN54H	CT04	SN74H	CT04	UNIT
	PARAIVIETER	TEST CONDITIONS	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V	High-level output voltage	I <sub>OH</sub> = – 20 μA	4.5	4.4	4.499		4.4		4.4		V
V <sub>OH</sub> High-level output voltage		I <sub>OH</sub> = – 4 mA	4.5	3.98	4.3		3.7		3.84		V
V	Low-level output voltage	I <sub>OL</sub> = 20 μA	5.5		0.001	0.1		0.1		0.1	V
V <sub>OL</sub> Low-level output voltage		I <sub>OL</sub> = 4 mA	3.3		0.17	0.26		0.4		0.33	, v
I <sub>I</sub>	Input hold current	V <sub>I</sub> = V <sub>CC</sub> or 0	5.5		±0.1	±100		±1000		±1000	nA
I <sub>CC</sub>	Supply current	$V_I = V_{CC}$ or 0. $I_O = 0$	5.5			2		40		20	μΑ
ΔICC <sup>(2)</sup>	Supply-current change	One input at 0.5V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>	5.5		1.4	2.4		3		2.9	mA
Ci	Input capacitance		4.5 to 5.5		3	10		10		10	pF

<sup>(1)</sup>  $V_I = V_{IH}$  or  $V_{IL}$ , unless otherwise noted.

### **5.5 Switching Characteristics**

C<sub>I</sub> = 50 pF. See Parameter Measurement Information

	PARAMETER	FROM (INPUT)	TO		TΔ	T <sub>A</sub> = 25°C			CT04	SN74HCT04			
TAKAMETEK	TROM (INFOT)	(OUTPUT)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX			
	Dronagation dolay	A or B	A or D	V	4.5		14	20		30		25	no
t <sub>pd</sub> Propagation delay	AUB	r	5.5		13	18		27		23	ns		
t Transition time			Υ	4.5		9	15		22		19	no	
t <sub>t</sub> Transition time		5.5			8	14		20		17	ns		

## **5.6 Operating Characteristics**

 $T_A = 25^{\circ}C$ 

		Test Conditions	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load	20	pF

<sup>(2)</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

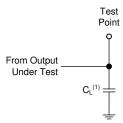


#### **6 Parameter Measurement Information**

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O$  = 50  $\Omega$ ,  $t_t$  < 6 ns.

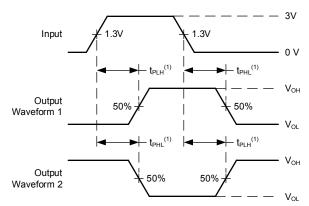
For clock inputs,  $f_{\text{max}}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C<sub>L</sub> includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

Figure 6-2. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

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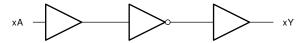


## 7 Detailed Description

## 7.1 Overview

These devices contain six independent inverters. They perform the Boolean function  $Y = \overline{A}$  in positive logic.

## 7.2 Functional Block Diagram



#### 7.3 Device Functional Modes

**Table 7-1. Function Table** (each inverter)

Input A	Output Y
Н	L
L	Н

## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V<sub>CC</sub> terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

### 9 Layout

#### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.



## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### **10.1 Documentation Support**

#### 10.1.1 Related Documentation

#### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 10.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 10.4 Trademarks

TI E2E<sup>™</sup> is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

#### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 10.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-89747012A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 89747012A SNJ54HCT 04FK
5962-8974701CA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974701CA SNJ54HCT04J
5962-8974701VCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974701VC A SNV54HCT04J
5962-8974701VCA.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974701VC A SNV54HCT04J
5962-8974701VDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974701VD A SNV54HCT04W
5962-8974701VDA.A	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974701VD A SNV54HCT04W
JM38510/65751BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65751BCA
JM38510/65751BCA.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65751BCA
M38510/65751BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65751BCA
SN54HCT04J	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HCT04J
SN54HCT04J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HCT04J
SN74HCT04D	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 85	HCT04
SN74HCT04DR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	HCT04
SN74HCT04DR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT04
SN74HCT04DRE4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT04
SN74HCT04DRG4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT04
SN74HCT04DRG4.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT04
SN74HCT04DT	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 85	HCT04



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5962-8974701CA SNJ54HCT04J



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Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	(3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74HCT04N	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT04N
SN74HCT04N.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT04N
SN74HCT04NE4	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT04N
SN74HCT04NSR	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT04
SN74HCT04NSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT04
SN74HCT04PW	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	-40 to 85	HT04
SN74HCT04PWR	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	HT04
SN74HCT04PWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT04
SN74HCT04PWRG4.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT04
SN74HCT04PWT	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	-40 to 85	HT04
SNJ54HCT04FK	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 89747012A SNJ54HCT 04FK
SNJ54HCT04FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 89747012A SNJ54HCT 04FK
SNJ54HCT04J	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974701CA SNJ54HCT04J

Active

SNJ54HCT04J.A

No

**SNPB** 

N/A for Pkg Type

-55 to 125

25 | TUBE

CDIP (J) | 14

Production

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## PACKAGE OPTION ADDENDUM

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(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN54HCT04, SN54HCT04-SP, SN74HCT04:

Catalog: SN74HCT04, SN54HCT04

Enhanced Product: SN74HCT04-EP, SN74HCT04-EP

Military: SN54HCT04

Space : SN54HCT04-SP

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## **PACKAGE MATERIALS INFORMATION**

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### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT04DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT04DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT04NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74HCT04NSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74HCT04PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



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#### \*All dimensions are nominal

7 111 41111011010110 410 11011111141							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT04DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74HCT04DRG4	SOIC	D	14	2500	353.0	353.0	32.0
SN74HCT04NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74HCT04NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74HCT04PWR	TSSOP	PW	14	2000	356.0	356.0	35.0



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### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-89747012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8974701VDA	W	CFP	14	25	506.98	26.16	6220	NA
5962-8974701VDA.A	W	CFP	14	25	506.98	26.16	6220	NA
SN74HCT04N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT04N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT04N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT04N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT04NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT04NE4	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54HCT04FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HCT04FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4040083-5/G





CERAMIC DUAL IN LINE PACKAGE



- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
   Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
   Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE



# N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SMALL OUTLINE PACKAGE



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE INTEGRATED CIRCUIT



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



## **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



# W (R-GDFP-F14)

## CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14



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