









SN54HC573A, SN74HC573A SCLS147G - DECEMBER 1982 - REVISED APRIL 2022

# SNx4HC573A Octal Transparent D-Type Latches With 3-State Outputs

### 1 Features

- Wide Operating Voltage Range from 2 V to 6 V
- High-Current 3-State Outputs Drive Bus Lines Directly up to 15 LSTTL Loads
- Low Power Consumption: 80-µA Maximum I<sub>CC</sub>
- Typical  $t_{pd}$  = 21 ns
- ±6-mA Output Drive at 5 V
- Low Input Current: 1 µA (Maximum)
- **Bus-Structured Pinout**

# 2 Applications

- **Buffer Registers**
- **Bidirectional Bus Drivers**
- Working Registers

# 3 Description

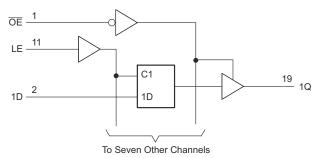
The SNx4HC573A devices are octal transparent D-type latches that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN54HC573AJ	CDIP (20)	26.92 mm × 6.92 mm
SN54HC573AW	CFP (20)	13.72 mm × 6.92 mm
SN54HC573AFK	LCCC (20)	8.89 mm × 8.89 mm
SN74HC573AN	PDIP (20)	25.40 mm × 6.35 mm
SN74HC573ADW	SOIC (20)	12.80 mm × 7.50 mm
SN74HC573ADB	SSOP (20)	7.20 mm × 5.30 mm
SN74HC573APW	TSSOP (20)	5.00 mm × 4.40 mm

For all available packages, see the orderable addendum at the end of the data sheet.



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**Logic Diagram (Positive Logic)** 



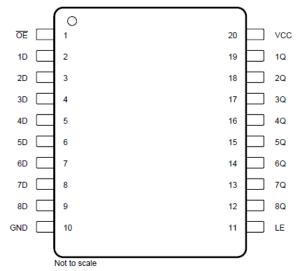
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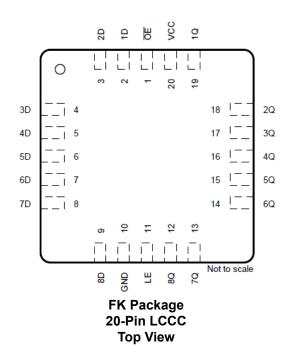
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Changes from Revision E (September 2003) to Revision F (October 2016)	Page	
Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section		
Changes from Revision F (October 2016) to Revision G (April 2022)	Page	
Updated ESD ratings table to modern TI standards	4	
• Changed Package thermal impedance, R <sub>0.IA</sub> , values from 92.5 to 122.7 (DB), from 78.3 to 109.1 (D	W), from	
49.1 to 84.6 (N), and from 101.1 to 131.8 (PW)		



# **5 Pin Configuration and Functions**



DB, DW, J, N, PW, or W Packages 20-Pin SSOP, SOIC, CDIP, PDIP, TSSOP, or CFP Top View



### **Pin Functions**

PIN		I/O <sup>(1)</sup>	DESCRIPTION
NO.	NAME		DESCRIPTION
1	ŌĒ	I	Output enable
2	1D	I	1D input
3	2D	I	2D input
4	3D	I	3D input
5	4D	I	4D input
6	5D	I	5D input
7	6D	I	6D input
8	7D	I	7D input
9	8D	I	8D input
10	GND	_	Ground
11	LE	I	Latch enable input
12	8Q	0	8Q output
13	7Q	0	7Q output
14	6Q	0	6Q output
15	5Q	0	5Q output
16	4Q	0	4Q output
17	3Q	0	3Q output
18	2Q	0	2Q output
19	1Q	0	1Q output
20	V <sub>CC</sub>	_	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.



# **6 Specifications**

# 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	$V_{l} < 0$ or $V_{l} > V_{CC}$		±20	mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
Io	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±35	mA
	Continuous current through V <sub>CC</sub> or GND			±70	mA
TJ	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

# 6.2 ESD Ratings

			VALUE	UNIT
	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±3500	\/
V <sub>(ESD)</sub>	Electrostatic discriarge	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

# **6.3 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2	5	6	V
		V <sub>CC</sub> = 2 V	1.5			
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V	3.15			V
		V <sub>CC</sub> = 6 V	4.2			
	Low-level input voltage	V <sub>CC</sub> = 2 V		-	0.5	
V <sub>IL</sub>		V <sub>CC</sub> = 4.5 V			1.35	V
		V <sub>CC</sub> = 6 V			1.8	
VI	Input voltage		0		V <sub>CC</sub>	V
Vo	Output voltage		0		V <sub>CC</sub>	V
		V <sub>CC</sub> = 2 V			1000	
t <sub>t</sub>	Input transition (rise and fall) time	V <sub>CC</sub> = 4.5 V			500	ns
		V <sub>CC</sub> = 6 V			400	
т	Operating free-air temperature	SN54HC573A	<b>–</b> 55		125	°C
T <sub>A</sub>	Operating nee-an temperature	SN74HC573A	-40	-	85	C

All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report (SCBA004).

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<sup>(2)</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



### **6.4 Thermal Information**

		DW (SOIC)	DB (SSOP)	N (PDIP)	PW (TSSOP)	
THERMAL METRIC		20 PINS	20 PINS	20 PINS	20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>	109.1	122.7	84.6	131.8	°C/W
R <sub>θJC (top)</sub>	Junction-to-case (top) thermal resistance	76	81.6	72.5	72.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	77.5	65.3	82.8	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	51.5	46.1	55.3	21.5	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	77.1	77.1	65.2	82.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

### 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
			V <sub>CC</sub> = 2 V	1.9	1.998		
		I <sub>OH</sub> = -20 μA	V <sub>CC</sub> = 4.5 V	4.4	4.499		
			V <sub>CC</sub> = 6 V	5.9	5.999		
			T <sub>A</sub> = 25°C	3.98	4.3		
V <sub>OH</sub> V <sub>OL</sub> I <sub>I</sub> I <sub>OZ</sub>	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -6 \text{ mA}, V_{CC} = 4.5 \text{ V}$	SN54HC573A	3.7			V
			SN74HC573A	3.84			
			T <sub>A</sub> = 25°C	5.48	5.8		
		$I_{OH} = -7.8 \text{ mA}, V_{CC} = 6 \text{ V}$	SN54HC573A	5.2			
			SN74HC573A	5.34			
			V <sub>CC</sub> = 2 V		0.002	0.1	
	$V_{I} = V_{IH}$ or $V_{IL}$	Ι <sub>ΟL</sub> = 20 μΑ	V <sub>CC</sub> = 4.5 V		0.001	0.1	
			V <sub>CC</sub> = 6 V		0.001	0.1	
		I <sub>OL</sub> = 6 mA, V <sub>CC</sub> = 4.5 V	T <sub>A</sub> = 25°C		0.17	0.26	
V <sub>OL</sub>			SN54HC573A			0.4	
			SN74HC573A			0.33	
		I <sub>OL</sub> = 7.8 mA, V <sub>CC</sub> = 6 V	T <sub>A</sub> = 25°C		0.15	0.26	
			SN54HC573A			0.4	
			SN74HC573A			0.33	
1	$V_1 = V_{CC}$ or 0, $V_{CC}$	- 6 V	T <sub>A</sub> = 25°C		±0.1	±100	nA
1	VI - VCC OI O, VCC	_ O V	SNx4HC573A			±1000	IIA
			T <sub>A</sub> = 25°C		±0.01	±0.5	
I <sub>OZ</sub>	$V_O = V_{CC}$ or 0, $V_{CC}$	<sub>C</sub> = 6 V	SN54HC573A			±10	μA
			SN74HC573A			±5	
			T <sub>A</sub> = 25°C			8	
Icc	$V_1 = V_{CC} \text{ or } 0, I_0 = 0, V_{CC} = 6 \text{ V}$		SN54HC573A			160	μΑ
			SN74HC573A			80	
C <sub>i</sub>	V <sub>CC</sub> = 2 V to 6 V				3	10	pF



over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C <sub>pd</sub>	Power dissipation capacitance per latch	T <sub>A</sub> = 25°C, no load		50		pF

# **6.6 Timing Requirements**

over operating free-air temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
			T <sub>A</sub> = 25°C	80			
		V <sub>CC</sub> = 2 V	SN54HC573A	120			
			SN74HC573A	100			
			T <sub>A</sub> = 25°C	16			
w Pulse duration, LE high	Pulse duration, LE high	V <sub>CC</sub> = 4.5 V	SN54HC573A	24			ns
			SN74HC573A	20			
			T <sub>A</sub> = 25°C	14			
		V <sub>CC</sub> = 6 V	SN54HC573A	20			
			SN74HC573A	17			
			T <sub>A</sub> = 25°C	50			
		V <sub>CC</sub> = 2 V	SN54HC573A	75			
			SN74HC573A	63			
		V <sub>CC</sub> = 4.5 V	T <sub>A</sub> = 25°C	10			
su	Setup time, data before LE↓		SN54HC573A	15			ns
			SN74HC573A	13			
			T <sub>A</sub> = 25°C	9			
		V <sub>CC</sub> = 6 V	SN54HC573A	13			
			SN74HC573A	11			
		V - 2 V	T <sub>A</sub> = 25°C	20			
	Hold time data after LT	V <sub>CC</sub> - 2 V	V <sub>CC</sub> = 2 V SNx4HC573A				20
h	Hold time, data after LE↓	V <sub>CC</sub> = 4.5 V		5			ns
		V <sub>CC</sub> = 6 V	V <sub>CC</sub> = 6 V				



# **6.7 Switching Characteristics**

over operating free-air temperature range (unless otherwise noted; see Figure 7-1)

PARAMETER	TI	EST CONDITIONS	,	MIN	TYP	MAX	UNIT
			T <sub>A</sub> = 25°C		77	175	
		V <sub>CC</sub> = 2 V	SN54HC573A			265	
			SN74HC573A			220	
			T <sub>A</sub> = 25°C		26	35	
	$C_L = 50 \text{ pF, from D (input)}$ to Q (output)	V <sub>CC</sub> = 4.5 V	SN54HC573A			53	
	to a (output)		SN74HC573A			44	
			T <sub>A</sub> = 25°C		23	30	
		V <sub>CC</sub> = 6 V	SN54HC573A			45	
			SN74HC573A			38	
t <sub>pd</sub>			T <sub>A</sub> = 25°C		87	175	ns
		V <sub>CC</sub> = 2 V	SN54HC573A			265	
			SN74HC573A			220	
			T <sub>A</sub> = 25°C		27	35	
	$C_L$ = 50 pF, from LE (input) to any Q (output)	V <sub>CC</sub> = 4.5 V	SN54HC573A			53	
	to any & (output)		SN74HC573A			44	
		V <sub>CC</sub> = 6 V	T <sub>A</sub> = 25°C		23	30	
			SN54HC573A			45	
			SN74HC573A			38	
			T <sub>A</sub> = 25°C		68	150	
		V <sub>CC</sub> = 2 V	SN54HC573A			225	
			SN74HC573A			190	
			T <sub>A</sub> = 25°C		24	30	
t <sub>en</sub>	$C_L = 50 \text{ pF, from } \overline{OE} \text{ (input)}$ to any Q (output)	V <sub>CC</sub> = 4.5 V	SN54HC573A			45	ns
	to arry & (output)		SN74HC573A			38	
			T <sub>A</sub> = 25°C		21	26	
		V <sub>CC</sub> = 6 V	SN54HC573A			38	
			SN74HC573A			32	
			T <sub>A</sub> = 25°C		47	150	
		V <sub>CC</sub> = 2 V	SN54HC573A			225	
			SN74HC573A			190	
			T <sub>A</sub> = 25°C		23	30	
t <sub>dis</sub>	$C_L = 50 \text{ pF, from } \overline{OE} \text{ (input)}$ to any Q (output)	V <sub>CC</sub> = 4.5 V	SN54HC573A			45	ns
	to any & (output)		SN74HC573A			38	
			T <sub>A</sub> = 25°C		21	26	
		V <sub>CC</sub> = 6 V	SN54HC573A			38	
			SN74HC573A		,	32	



over operating free-air temperature range (unless otherwise noted; see Figure 7-1)

PARAMETER	e-air temperature range (unless TE	ST CONDITIONS		MIN	TYP	MAX	UNIT	
			T <sub>A</sub> = 25°C		28	60		
		V <sub>CC</sub> = 2 V	SN54HC573A			90		
			SN74HC573A			75		
			T <sub>A</sub> = 25°C		8	12		
t <sub>t</sub>	C <sub>L</sub> = 50 pF to any Q (output)	V <sub>CC</sub> = 4.5 V	SN54HC573A			18	ns	
			SN74HC573A			15		
			T <sub>A</sub> = 25°C		6	10		
		V <sub>CC</sub> = 6 V	SN54HC573A			15		
			SN74HC573A			13		
			T <sub>A</sub> = 25°C		95	200		
		V <sub>CC</sub> = 2 V	SN54HC573A			300		
			SN74HC573A			250		
			T <sub>A</sub> = 25°C		33	40		
	$C_L = 150 \text{ pF, from D (input)}$	V <sub>CC</sub> = 4.5 V	SN54HC573A			60		
	to Q (output)		SN74HC573A			50		
			T <sub>A</sub> = 25°C		21	34		
		V <sub>CC</sub> = 6 V	SN54HC573A			51		
		1.00	SN74HC573A			43		
pd			T <sub>A</sub> = 25°C		103	225	ns	
	$C_L$ = 150 pF, from LE (input) to any Q (output)	V <sub>CC</sub> = 2 V	SN54HC573A			335		
			SN74HC573A			285		
		V <sub>CC</sub> = 4.5 V	T <sub>A</sub> = 25°C		33	45		
			SN54HC573A			67		
			SN74HC573A			57		
		V <sub>CC</sub> = 6 V	T <sub>A</sub> = 25°C		29	40		
			SN54HC573A			60		
			SN74HC573A			50		
			T <sub>A</sub> = 25°C		85	200		
		V <sub>CC</sub> = 2 V	SN54HC573A		- 00	300		
		VCC - Z V	SN74HC573A					
			T <sub>A</sub> = 25°C		29	250 40		
	$C_L = 150 \text{ pF, from } \overline{OE} \text{ (input)}$	\\ - 4 E \\	SN54HC573A			60	20	
en	to any Q (output)	V <sub>CC</sub> = 4.5 V					ns	
			SN74HC573A			50		
		V - C V	T <sub>A</sub> = 25°C		26	34		
		V <sub>CC</sub> = 6 V	SN54HC573A			51		
			SN74HC573A			43		
		., .,	T <sub>A</sub> = 25°C		60	210		
		V <sub>CC</sub> = 2 V	SN54HC573A			315		
			SN74HC573A			265		
			T <sub>A</sub> = 25°C		17	42		
t	C <sub>L</sub> = 150 pF to any Q (output)	V <sub>CC</sub> = 4.5 V	SN54HC573A			63	ns	
			SN74HC573A			53		
			T <sub>A</sub> = 25°C		14	36		
		V <sub>CC</sub> = 6 V	SN54HC573A			53		
			SN74HC573A			45		



# **6.8 Typical Characteristics**

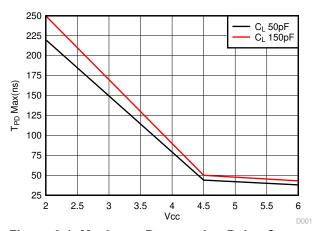
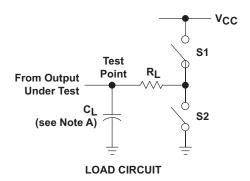


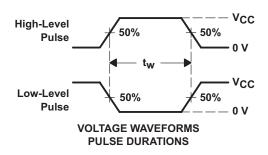
Figure 6-1. Maximum Propagation Delay Curves

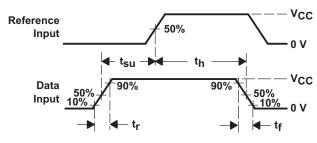


### 7 Parameter Measurement Information

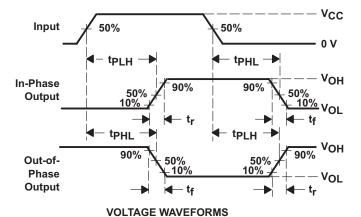


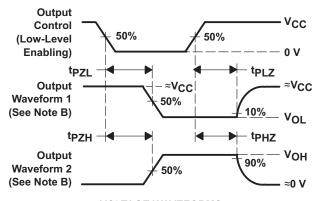
PARA	METER	RL	CL	S1	S2	
IAKA	1	I'\L		_		
t <sub>en</sub>	tPZH	1 kΩ	50 pF or	Open	Closed	
en	tPZL T K12		150 pF	Closed	Open	
	tPHZ			Open	Closed	
<sup>t</sup> dis	tPLZ	<b>1 k</b> Ω	50 pF	Closed	Open	
t <sub>pd</sub> or	t <sub>pd</sub> or t <sub>t</sub>		50 pF or 150 pF	Open	Open	





**VOLTAGE WAVEFORMS** SETUP AND HOLD AND INPUT RISE AND FALL TIMES





PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

**VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS** 

- C<sub>L</sub> includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
- The outputs are measured one at a time with one input transition per measurement. D.
- t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.

Figure 7-1. Load Circuit and Voltage Waveforms

# 8 Detailed Description

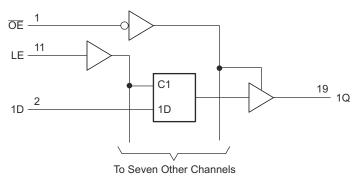
### 8.1 Overview

The SNx4HC573A devices are octal transparent D-type latches that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  must be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

 $\overline{\text{OE}}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

### 8.2 Functional Block Diagram



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Figure 8-1. Logic Diagram (Positive Logic)

### 8.3 Feature Description

The SNx4HC573A is a high current 3-state output device which can drive bus lines directly or up to 15 LSTTL loads. It has low power consumption up to  $80-\mu A$  maximum  $I_{CC}$ . The high speed CMOS family has typical propagation delay of 21 ns with  $\pm 6$ -mA output drive at 5 V. The input leakage current is a very low  $1-\mu A$  (maximum).

### 8.4 Device Functional Modes

Table 8-1 lists the functional modes of the SNx4HC573A.

**INPUTS OUTPUT** ŌΕ LE D Q Н Н Н L Н L L L L Χ  $Q_0$ Н Х Χ Hi-Z

**Table 8-1. Function Table (Each Latch)** 

# 9 Application and Implementation

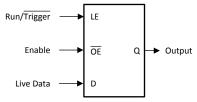
#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  must be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.  $\overline{\text{OE}}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state. The SNx4HC573A latches can be used to store 8 bits of data. Figure 9-1 shows a typical application. A low trigger event latches the output to preserve the event for processing later. With latch input high, this acts as a buffer which follows the live data at the D input when output enable pin held is low.

## 9.2 Typical Application



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Figure 9-1. Typical Application Schematic

#### 9.2.1 Design Requirements

The SNx4HC573A device uses CMOS technology and has balanced output drive (±7.8-mA). Take care to avoid bus contention, because it can drive currents that would exceed maximum limits.

### 9.2.2 Detailed Design Procedure

Design requirements must adhere to the Section 6.3 and must never exceed the Section 6.1.

The inputs must have a ramp time less than input transition time mentioned in the *Section 6.3*. Slow inputs can cause oscillations at the output, false triggering, and increased current consumption. TI recommends a Schmitt trigger device like SN74HC14 which can tolerate slower signals.

The inputs and outputs must never exceed  $V_{CC}$  to not forward bias the internal ESD diodes. The maximum frequency supported by this device is 28 MHz.



### 9.2.3 Application Curve

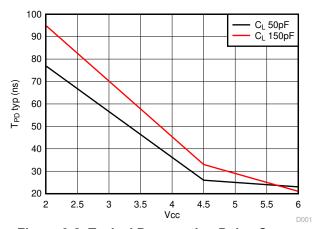


Figure 9-2. Typical Propagation Delay Curves

# 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Section 6.3 table. The total current through Ground or  $V_{CC}$  must not exceed  $\pm 70$  mA as per Section 6.1 table.

Each  $V_{CC}$  pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1- $\mu$ F capacitor; if there are multiple  $V_{CC}$  pins, then TI recommends 0.01- $\mu$ F or 0.022- $\mu$ F capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1- $\mu$ F and 1- $\mu$ F capacitor are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.



### 11 Layout

# 11.1 Layout Guidelines

When using multiple-bit logic devices, inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input and the gate are used, or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 11-1 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, they are tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This does not disable the input section of the I/Os, so they cannot float when disabled.

### 11.2 Layout Example

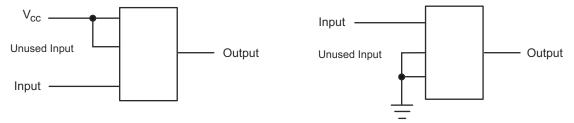


Figure 11-1. Layout Diagram



# 12 Device and Documentation Support

### **12.1 Documentation Support**

### 12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs (SCBA004)

#### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC573A	Click here	Click here	Click here	Click here	Click here
SN74HC573A	Click here	Click here	Click here	Click here	Click here

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

### 12.5 Trademarks

TI E2E<sup>™</sup> is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

#### 12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.7 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

### 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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# **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-8512801VRA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8512801VR A SNV54HC573AJ
5962-8512801VRA.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8512801VR A SNV54HC573AJ
85128012A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	85128012A SNJ54HC 573AFK
8512801RA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8512801RA SNJ54HC573AJ
8512801SA	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8512801SA SNJ54HC573AW
JM38510/65406BRA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65406BRA
JM38510/65406BRA.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65406BRA
M38510/65406BRA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65406BRA
SN54HC573AJ	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC573AJ
SN54HC573AJ.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC573AJ
SN74HC573ADBR	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC573A
SN74HC573ADBR.A	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC573A
SN74HC573ADW	Obsolete	Production	SOIC (DW)   20	-	=	Call TI	Call TI	-40 to 85	HC573A
SN74HC573ADWR	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC573A
SN74HC573ADWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC573A
SN74HC573ADWRG4	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC573A
SN74HC573AN	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC573AN
SN74HC573AN.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC573AN
SN74HC573AN.B	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC573AN
SN74HC573ANE4	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC573AN
SN74HC573APWR	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC573A



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Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74HC573APWR.A	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC573A
SN74HC573APWR.B	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC573A
SN74HC573APWRG4	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC573A
SN74HC573APWT	Obsolete	Production	TSSOP (PW)   20	-	-	Call TI	Call TI	-40 to 85	HC573A
SNJ54HC573AFK	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	85128012A SNJ54HC 573AFK
SNJ54HC573AFK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	85128012A SNJ54HC 573AFK
SNJ54HC573AJ	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8512801RA SNJ54HC573AJ
SNJ54HC573AJ.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8512801RA SNJ54HC573AJ
SNJ54HC573AW	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8512801SA SNJ54HC573AW
SNJ54HC573AW.A	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8512801SA SNJ54HC573AW

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# PACKAGE OPTION ADDENDUM

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN54HC573A, SN54HC573A-SP, SN74HC573A:

Catalog: SN74HC573A, SN54HC573A

Automotive: SN74HC573A-Q1, SN74HC573A-Q1

Military: SN54HC573A

Space: SN54HC573A-SP

#### NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application

# **PACKAGE MATERIALS INFORMATION**

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### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC573ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HC573ADWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HC573APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

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## \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC573ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74HC573ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74HC573APWR	TSSOP	PW	20	2000	353.0	353.0	32.0

# **PACKAGE MATERIALS INFORMATION**

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### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
85128012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8512801SA	W	CFP	20	25	506.98	26.16	6220	NA
SN74HC573AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC573AN.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC573AN.B	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC573ANE4	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54HC573AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC573AFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC573AW	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54HC573AW.A	W	CFP	20	25	506.98	26.16	6220	NA

# W (R-GDFP-F20)

# CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

  D. Index point is provided on cap for terminal identification only.

  E. Falls within Mil—Std 1835 GDFP2—F20







### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



### 14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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