

SNx4BCT374 Octal Edge-Triggered D-Type Latches With 3-State Outputs

1 Features

- Operating Voltage Range of 4.5 V to 5.5 V
- BiCMOS Design Significantly Reduces I_{CCZ} Over TTL Designs
- Full Parallel Access for Loading
- **Buffered Control Inputs**
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers

2 Applications

- **Buffer Registers**
- I/O Ports
- **Bus Drivers**
- Working Registers

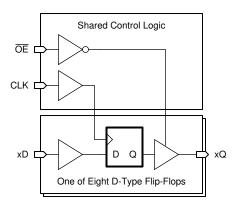
3 Description

The SNx4BCT374 devices contain eight channels of D-type flip-flops with a shared clock (CLK) and output enable (OE) pin.

Device Information (1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|--------------|-----------|--------------------|
| SN74BCT374N | PDIP (20) | 25.40 mm × 6.35 mm |
| SN74BCT374DW | SOIC (20) | 12.80 mm × 7.50 mm |
| SN74BCT374NS | SOP (20) | 12.60 mm × 5.30 mm |
| SN74BCT374DB | SSOP (20) | 7.20 mm × 5.30 mm |
| SN54BCT374J | CDIP (20) | 26.92 mm × 6.92 mm |
| SN54BCT374W | CFP (20) | 13.72 mm × 6.92 mm |
| SN54BCT374FK | LCCC (20) | 8.89 mm × 8.89 mm |

For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram



Page

Page

Table of Contents

| 1 Features | 1 | 8.3 Feature Description | 8 |
|--|----|--|----|
| 2 Applications | | 8.4 Device Functional Modes | |
| 3 Description | | 9 Application and Implementation | 10 |
| 4 Revision History | | 9.1 Application Information | |
| 5 Pin Configuration and Functions | | 9.2 Typical Application | |
| 6 Specifications | | 10 Power Supply Recommendations | |
| 6.1 Absolute Maximum Ratings (1) | | 11 Layout | |
| 6.2 ESD Ratings | | 11.1 Layout Guidelines | |
| 6.3 Recommended Operating Conditions (1) | | 11.2 Layout Example | |
| 6.4 Thermal Information | | 12 Device and Documentation Support | |
| 6.5 Electrical Characteristics | | 12.1 Documentation Support | |
| 6.6 Timing Requirements | .6 | 12.2 Receiving Notification of Documentation Updates | |
| 6.7 Switching Characteristics | | 12.3 Support Resources | |
| 6.8 Typical Characteristics | .6 | 12.4 Trademarks | |
| 7 Parameter Measurement Information | | 12.5 Electrostatic Discharge Caution | 13 |
| 8 Detailed Description | 8 | 12.6 Glossary | |
| 8.1 Overview | | 13 Mechanical, Packaging, and Orderable | |
| 8.2 Functional Block Diagram | | Information | 13 |
| · · | | | |

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2003) to Revision D (February 2021)

Changes from Revision A (November 1993) to Revision B (April 1994)

| • | Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
|---|--|----------------|
| • | Added new applications to the Applications section | 1 |
| • | Removed Ordering Information and Function tables from the Description section | 1 |
| • | Added the Device Information table to the Description section | 1 |
| • | Moved package thermal impedance, Θ _{JA} for the DW, N, and NS packages to Section 6.4 | 4 |
| • | Added ESD Ratings section | 4 |
| • | Added Thermal Information section | 5 |
| • | Changed I _{OS} (min) value From: –100 mA To: –50 mA | 5 |
| • | Added Timing Requirements, Switching Characteristics, and Typical Characteristics sections | <mark>6</mark> |
| • | Added Detailed Description section | 8 |
| • | Added Application and Implementation section | 10 |
| • | Added Power Supply Recommendations and Layout sections | 12 |
| С | hanges from Revision B (April 1994) to Revision C (March 2003) | Page |
| • | Added Ordering Information table to the Description section | 1 |
| • | Added package thermal impedance, Θ_{JA} for the DW, N, and NS packages | 4 |
| _ | | |



5 Pin Configuration and Functions

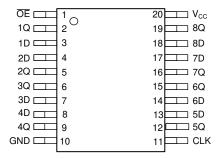


Figure 5-1. DB, DW, N, NS, J, or W Package 20-Pin SSOP, SOIC, PDIP, SO, CDIP, or CFP Top View

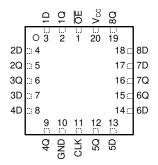


Figure 5-2. FK Package 20-Pin LCCC Transparent Top View

Table 5-1. Pin Functions

| PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|-----------------|-----|--------------------|------------------------------|
| NAME | NO. | - 1/0(1/ | DESCRIPTION |
| ŌĒ | 1 | ı | Output enable, active low |
| 1Q | 2 | 0 | Channel 1 output |
| 1D | 3 | I | Channel 1 input |
| 2D | 4 | I | Channel 2 input |
| 2Q | 5 | 0 | Channel 2 output |
| 3Q | 6 | 0 | Channel 3 output |
| 3D | 7 | I | Channel 3 input |
| 4D | 8 | ı | Channel 4 input |
| 4Q | 9 | 0 | Channel 4 output |
| GND | 10 | G | Ground |
| CLK | 11 | ı | Clock, rising edge triggered |
| 5Q | 12 | 0 | Channel 5 output |
| 5D | 13 | I | Channel 5 input |
| 6D | 14 | I | Channel 6 input |
| 6Q | 15 | 0 | Channel 6 output |
| 7Q | 16 | 0 | Channel 7 output |
| 7D | 17 | ı | Channel 7 input |
| 8D | 18 | ı | Channel 8 input |
| 8Q | 19 | 0 | Channel 8 output |
| V _{CC} | 20 | Р | Positive supply |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|------------------|--|------|------|-----------------|------|
| V _{CC} | Supply voltage range | | -0.5 | 7 | V |
| VI | Input voltage range ⁽²⁾ | | -0.5 | 7 | V |
| Vo | Voltage range applied to any output in the disabled or power-off state | | -0.5 | 5.5 | V |
| Vo | Voltage range applied to any output in the high state | | -0.5 | V _{CC} | V |
| I _{IK} | Input clamp current | | | -30 | mA |
| | SN54BC | T374 | | 96 | m A |
| IOL | Current into any output in the low state SN74BCT374 | | | | mA |
| T _{stg} | Storage temperature range ⁽³⁾ | | -65 | 150 | °C |

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| | | | VALUE | UNIT |
|---------|---------------------------|--|-------|------|
| V | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ¹ | ±2000 | \/ |
| V (ESD) | Electrostatic discridinge | Charged-device model (CDM), per JEDEC specification JESD22-C101 ² | ±1000 | V |

6.3 Recommended Operating Conditions (1)

| | Operating free-air temperature (T _A) | | | | | | |
|---|--|----------|-------------------|-----|-----|------|----|
| | -55° | C to 125 | °C ⁽²⁾ | 0°0 |) | UNIT | |
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V _{IH} High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I _{IK} Input clamp current | | | -18 | | | -18 | mA |
| Гон | | | -2 | | | -15 | mA |
| I _{OL} Low-level output current | | | 48 | | | 64 | mA |
| T _A Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

⁽¹⁾ All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs.

Product Folder Links: SN74BCT374

⁽²⁾ The negative input voltage rating may be exceeded if the input clamp current rating is observed.

⁽³⁾ Long-term high-temperature storage and extended use at maximum recommended operating conditions or both may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

⁽²⁾ Applies to SN54BCT374 devices only

⁽³⁾ Applies to SN74BCT374 devices only

6.4 Thermal Information

| THERMA | THERMAL METRIC ⁽¹⁾ | | | N (PDIP) | NS (SO) | UNIT |
|-----------------------|--|---------|---------|----------|---------|------|
| | | 20 PINS | 20 PINS | 20 PINS | 20 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 84.4 | 73.4 | 59.7 | 71.2 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 40.1 | 41.9 | 40.6 | 36.2 | °C/W |
| Ψ ЈТ | Junction-to-top characterization parameter | 6.2 | 14.6 | 24.9 | 7.6 | °C/W |
| Ψ ЈВ | Junction-to-board characterization parameter | 39.5 | 41.4 | 40.3 | 35.9 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 36.8 | 38.8 | 50.0 | 34.3 | °C/W |

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| | | | Operating free-air temperature (T _A) | | | | | | ۷) | |
|---------------------|--|--------------------------|--|-------------------------------|------|-----|----------------------------|-------------------|------|----|
| PARAMETER | TEST CONDITIONS | | | -55°C to 125°C ⁽³⁾ | | | 0°C to 70°C ⁽⁴⁾ | | | |
| | | | MIN | TYP ⁽¹⁾ | MAX | MIN | T | YP ⁽¹⁾ | MAX | |
| V _{IK} | V _{CC} = 4.5 V, I _I = -18 mA | | | | -1.2 | | | | -1.2 | V |
| | | I _{OH} = –3 mA | 2.4 | 3.3 | | 2 | 2.4 | 3.3 | | |
| V _{OH} | V _{CC} = 4.5 V | I _{OH} = -12 mA | 2 | 3.2 | | | | | | V |
| | | I _{OH} = -15 mA | | | | | 2 | 3.1 | | |
| V | \\ - 4 E \\ | I _{OL} = 48 mA | | 0.38 | 0.55 | | | | | V |
| V _{OL} | V _{CC} = 4.5 V | I _{OL} = 64 mA | | | | | | 0.42 | 0.55 | |
| I _I | V _{CC} = 5.5 V, V _I = 5.5 V | - | | | 0.4 | | | | 0.4 | mA |
| I _{IH} | $V_{CC} = 5.5 \text{ V}, V_{I} = 2.7 \text{ V}$ | | | | 20 | | | | 20 | μΑ |
| I _{IL} | V _{CC} = 5.5 V, V _I = 0.5 V | | | | -0.6 | | | | -0.6 | mA |
| I _{OS} (2) | V _{CC} = 5.5 V, V _O = 0 V | | -50 | | -225 | _ | 50 | | -225 | mA |
| I _{OZH} | V _{CC} = 5.5 V, V _O = 2.7 V | | | | 50 | | | | 50 | μA |
| I _{OZL} | V _{CC} = 5.5 V, V _O = 0.5 V | | | | -50 | | | | -50 | μA |
| I _{CCL} | V _{CC} = 5.5 V | | | 37 | 60 | | | 37 | 60 | mA |
| Іссн | V _{CC} = 5.5 V | | | 2 | 5 | | | 2 | 5 | mA |
| I _{CCZ} | V _{CC} = 5.5 V | | | 5 | 8 | | | 5 | 8 | mA |
| Ci | V _{CC} = 5 V, V _I = 2.5 V or 0.5 V | | | 6 | | | | 6 | | pF |
| Co | V _{CC} = 5 V, V _O = 2.5 V or 0.5 V | | | 10 | | | | 10 | | pF |

- (1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
- (2) Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- (3) Applies to SN54BCT374 devices only
- (4) Applies to SN74BCT374 devices only



6.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

| | | Operating free-air temperature (T _A) | | | | | | | |
|--------------------|-------------------------|--|-----|------------------|----------|----------------------|----------|---------------------|------|
| | PARAMETER | | 25° | C ⁽¹⁾ | -55°C to | 125°C ⁽²⁾ | 0°C to 7 | 70°C ⁽³⁾ | UNIT |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | | | 70 | | 70 | | 70 | MHz |
| t _w | Pulse duration | CLK high | 7 | | 8 | | 7 | | ns |
| t _{su} | Setup time before CLK ↑ | Data high or low | 6.5 | | 6.5 | | 6.5 | | ns |
| t _h | Hold time after CLK ↑ | Data high or low | 0 | | 0 | | 0 | | ns |

- (1) $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$, applies to all SN54BCT374 and SN74BCT374 devices
- (2) Applies to SN54BCT374 devices only
- (3) Applies to SN74BCT374 devices only

6.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| | | | Operating free-air temperature (T _A) | | | | | | | |
|------------------|-----------------|----------------|--|---------------------|------|-----------------------------------|------|--------------------------------|------|------|
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | | 25°C ⁽¹⁾ | | -55°C to 125°C ^{(2) (3)} | | 0°C to 70°C ^{(2) (4)} | | UNIT |
| | (51) | (331131) | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f _{max} | | | 70 | | | 70 | | 70 | | MHz |
| t _{PLH} | CLK | Q | 2 | 7.2 | 9.1 | 2 | 11.6 | 2 | 10.6 | ns |
| t _{PHL} | CLK | CLK Q | 2 | 7.1 | 8.8 | 2 | 10.6 | 2 | 10 | 115 |
| t _{PZH} | ŌĒ | Q | 1 | 8.3 | 10.1 | 1 | 12.7 | 1 | 12.3 | ns |
| t _{PZL} | OL | l Q | 1 | 8.6 | 10.6 | 1 | 13 | 1 | 12.7 | 115 |
| t _{PHZ} | OE | Q | 1 | 4.7 | 6.3 | 1 | 7.1 | 1 | 6.8 | ns |
| t_{PLZ} | OL | Q | 1 | 4.8 | 6.3 | 1 | 7.5 | 1 | 6.8 | 115 |

- (1) $V_{CC} = 5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_1 = 500 \Omega$, $R_2 = 500 \Omega$, $T_A = 25^{\circ}\text{C}$, applies to all SN54BCT374 and SN74BCT374 devices
- (2) $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, C_L = 50 \text{ pF}, R_1 = 500 \Omega, R_2 = 500 \Omega$
- (3) Applies to SN54BCT374 devices only
- (4) Applies to SN74BCT374 devices only

6.8 Typical Characteristics

 $T_A = 25^{\circ}C$

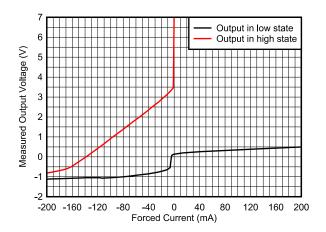
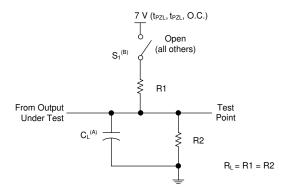


Figure 6-1. Typical output voltage versus output current for BCT family drivers

7 Parameter Measurement Information

All parameters and waveforms are not applicable to all devices.



- From Output Under Test

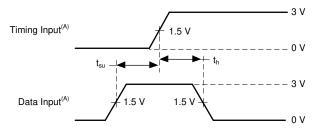
 C_L^(A)

 R1
- A. C_L includes probe and jig capacitance.

Figure 7-2. Load circuit for push-pull outputs

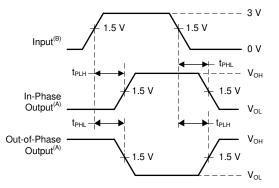
- A. C_L includes probe and jig capacitance.
- When measuring propagation delay times of 3-state outputs, switch S1 is open.

Figure 7-1. Load circuit for 3-state and open-collector outputs



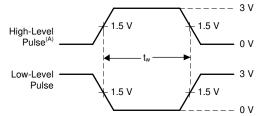
A. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $t_r = t_f \leq$ 2.5 ns, duty cycle = 50%.

Figure 7-3. Voltage waveforms Setup and hold times



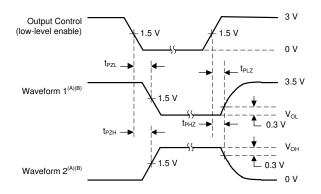
- The outputs are measured one at a time with one transition per measurement.
- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $t_r = t_f \leq$ 2.5 ns, duty cycle = 50%.

Figure 7-5. Voltage waveforms Propagation delay times



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, t_r = t_f ≤ 2.5 ns, duty cycle = 50%.

Figure 7-4. Voltage waveforms
Pulse duration



- A. The outputs are measured one at a time with one transition per measurement.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 7-6. Voltage waveforms Enable and disable times, 3-state outputs

8 Detailed Description

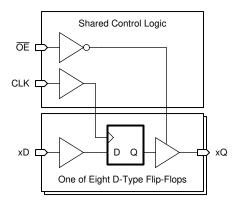
8.1 Overview

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the SNx4BCT374 devices are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. The output-enable (\overline{OE}) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bipolar Push-Pull Outputs

This device includes bipolar push-pull outputs. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused bipolar push-pull outputs should be left disconnected.

8.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law $(R = V \div I)$.

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in Implications of Slow or Floating CMOS Inputs.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors, however a 10-k Ω resistor is recommended and will typically meet all requirements.

8.3.3 Clamp Diode Structure

The inputs and outputs to this device have negative clamping diodes only as depicted in Figure 8-1.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

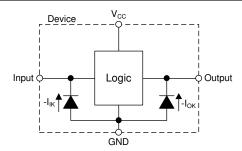


Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

The Function Table below lists the functional modes of the SNx4BCT374.

| | OUTPUT ⁽²⁾ | | | | | | | | |
|----|-----------------------|---|-------|--|--|--|--|--|--|
| ŌĒ | CLK | Q | | | | | | | |
| L | ↑ | Н | Н | | | | | | |
| L | ↑ | L | L | | | | | | |
| L | H or L | X | Q_0 | | | | | | |
| Н | X | X | Z | | | | | | |

Table 8-1. Function Table

- (1) L = Low input, H = High input, \uparrow = Low to high transition, X = Do not care.
- (2) L = Low output, H = High output, Q_0 = Previous state, Z = High impedance.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SNx4BCT374 contains multiple D-type flip-flops that are operated by the same clock. By connecting multiple channels together in series, a shift register can be formed. This produces a delay of a specific number of clock cycles for incoming data. The application schematic shown below gives an example of using three channels of the SNx4BCT374 to produce a delay of three clock cycles.

9.2 Typical Application

9.2.1 Application

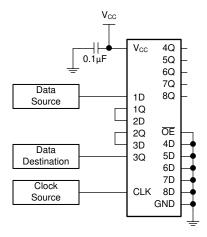


Figure 9-1. Typical application block diagram

9.2.2 Design Requirements

9.2.2.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SNx4BCT374 plus the maximum static supply current, I_{CC}, listed in *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SNx4BCT374 plus the maximum supply current, I_{CC}, listed in *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection.

The SNx4BCT374 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 50 pF.

Submit Document Feedback

Copyright © 2021 Texas Instruments Incorporated

The SNx4BCT374 can drive a load with total resistance described by $R_L \ge V_O$ / I_O , with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the high state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

9.2.2.2 Output Considerations

The positive supply voltage is used to produce the output high voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output low voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull bipolar outputs should never be connected directly together. This can cause excessive current and damage to the device.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to Feature Description section for additional information regarding the outputs for this device.

9.2.2.3 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic low, and $V_{IH(min)}$ to be considered a logic high. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. These can be directly connected if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of high, and a pull-down resistor is used for a default state of low. The resistor size is limited by drive current of the controller, leakage current into the SNx4BCT374, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-k Ω resistor value is often used due to these factors.

The SNx4BCT374 has CMOS inputs and thus requires fast input transitions to operate correctly. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the Feature Description section for additional information regarding the inputs for this device.

9.2.3 Detailed Design Procedure

- 1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the SNx4BCT374 and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
- 2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SNx4BCT374 to the receiving device(s).
- 3. Ensure the resistive load at the output is larger than (V_{CC} / I_{O(max)}) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
- 4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation.
- 5. This device includes D-type flip-flop circuits. The output of these circuits is unknown at system startup. Data must be clocked into each D-type flip-flop to initialize it into a known state.

Copyright © 2021 Texas Instruments Incorporated

Submit Document Feedback



9.2.4 Application Curves

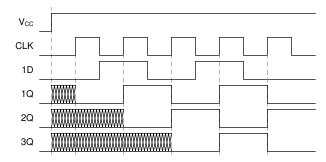


Figure 9-2. Application timing diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

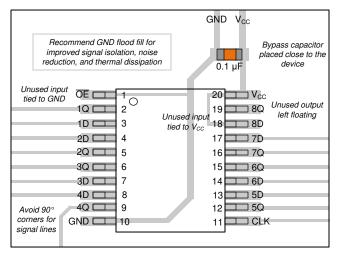


Figure 11-1. Example layout for the SN74BCT374.

Submit Document Feedback

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, Designing With Logic application report
- Texas Instruments, Input and Output Characteristics of Digital Integrated Circuits application report
- Texas Instruments, Implications of Slow or Floating CMOS Inputs application report
- Texas Instruments, Understanding and Interpreting Standard-Logic Data Sheets application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 9-Nov-2025

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type | Package Pins | Package qty Carrier | RoHS | Lead finish/ Ball material | MSL rating/ Peak reflow | Op temp (°C) | Part marking (6) |
|-----------------------|------------|---------------|----------------|-----------------------|------|-------------------------------|----------------------------|--------------|--|
| 5962-9051601M2A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9051601M2A SNJ54BCT 374FK |
| 5962-9051601MRA | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9051601MR A SNJ54BCT374J |
| 5962-9051601MSA | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9051601MS A SNJ54BCT374W |
| SN74BCT374DW | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | BCT374 |
| SN74BCT374DW.A | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | BCT374 |
| SN74BCT374N | Active | Production | PDIP (N) 20 | 20 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74BCT374N |
| SN74BCT374N.A | Active | Production | PDIP (N) 20 | 20 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74BCT374N |
| SN74BCT374NSR | Active | Production | SOP (NS) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | BCT374 |
| SN74BCT374NSR.A | Active | Production | SOP (NS) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | BCT374 |
| SNJ54BCT374FK | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9051601M2A SNJ54BCT 374FK |
| SNJ54BCT374FK.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9051601M2A SNJ54BCT 374FK |
| SNJ54BCT374J | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9051601MR A SNJ54BCT374J |
| SNJ54BCT374J.A | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9051601MR A SNJ54BCT374J |
| SNJ54BCT374W | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9051601MS A SNJ54BCT374W |



9-Nov-2025 www.ti.com

| Orderable part number | Status | Material type | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material | MSL rating/ Peak reflow | Op temp (°C) | Part marking (6) |
|-----------------------|--------|---------------|----------------|-----------------------|-----------------|-------------------------------|----------------------------|--------------|-------------------------------------|
| SNJ54BCT374W.A | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9051601MS A SNJ54BCT374W |

⁽¹⁾ Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54BCT374, SN74BCT374:

Catalog: SN74BCT374

Military: SN54BCT374

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.



PACKAGE OPTION ADDENDUM

www.ti.com 9-Nov-2025

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 23-Jul-2025

TAPE AND REEL INFORMATION





| A0 | Dimension designed to accommodate the component width |
|----|---|
| В0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|-----------------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| SN74BCT374NSR | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |

PACKAGE MATERIALS INFORMATION

www.ti.com 23-Jul-2025



*All dimensions are nominal

| | Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN | 174BCT374NSR | SOP | NS | 20 | 2000 | 356.0 | 356.0 | 45.0 |

PACKAGE MATERIALS INFORMATION

www.ti.com 23-Jul-2025

TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9051601M2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9051601MSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74BCT374DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74BCT374DW.A | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74BCT374N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74BCT374N.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54BCT374FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54BCT374FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54BCT374W | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54BCT374W.A | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |

14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

 D. Index point is provided on cap for terminal identification only.

 E. Falls within Mil—Std 1835 GDFP2—F20



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025