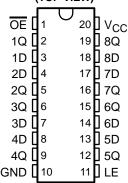
SCBS016D - SEPTEMBER 1988 - REVISED MARCH 2003

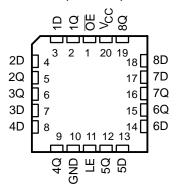
- Operating Voltage Range of 4.5 V to 5.5 V
- State-of-the-Art BiCMOS Design Significantly Reduces I<sub>CCZ</sub>
- Full Parallel Access for Loading

SN54BCT373...J OR W PACKAGE SN74BCT373...DB, DW, N, OR NS PACKAGE (TOP VIEW)



- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds JESD 22
   2000-V Human-Body Model (A114-A)

SN54BCT373 . . . FK PACKAGE (TOP VIEW)



### description/ordering information

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'BCT373 devices are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels that were set up at the D inputs.

A buffered output-enable  $(\overline{OE})$  input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

### ORDERING INFORMATION

TA	PACKA	GEŤ	ORDERABLE PART NUMBER	TOP-SIDE Marking
	PDIP – N Tube SN74BCT373N		SN74BCT373N	
	SOIC - DW	Tube	SN74BCT373DW	BCT373
0°C to 70°C	301C - DW	Tape and reel	SN74BCT373DWR	BC1373
	SOP - NS	Tape and reel	SN74BCT373NSR	BCT373
	SSOP – DB	Tape and reel	SN74BCT373DBR	BT373
	CDIP – J	Tube	SNJ54BCT373J	SNJ54BCT373J
–55°C to 125°C	CFP – W	Tube	SNJ54BCT373W	SNJ54BCT373W
	LCCC – FK Tube		SNJ54BCT373FK	SNJ54BCT373FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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### description/ordering information (continued)

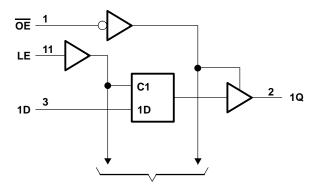
To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

# FUNCTION TABLE (each latch)

	INPUTS	OUTPUT	
Œ	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	$Q_0$
Н	X	Χ	Z

### logic diagram (positive logic)



To Seven Other Channels

### SN54BCT373, SN74BCT373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the disabled or power-off state,	V <sub>O</sub> –0.5 V to 5.5 V
Voltage range applied to any output in the high state, V <sub>O</sub>	–0.5 V to V <sub>CC</sub>
Input clamp current, I <sub>IK</sub>	–30 mA
Current into any output in the low state: SN54BCT373	96 mA
SN74BCT373	128 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

		SN54BCT373			SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
liK	Input clamp current			-18			-18	mA
ЮН	High-level output current			-12			-15	mA
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



## SN54BCT373, SN74BCT373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		SN	154BCT3	73	SN74BCT373			LINIT
PARAMETER	TEST CONDITIONS			TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	UNIT
VIK	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.2			-1.2	V
		IOH = -3  mA	2.4	3.3		2.4	3.3		
Voн	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -12 \text{ mA}$	2	3.2					V
		$I_{OH} = -15 \text{ mA}$				2	3.1		
Vo.	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA		0.38	0.55				٧
VOL	VCC = 4.5 V	I <sub>OL</sub> = 64 mA					0.42	0.55	V
lμ	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = 5.5 V			0.4			0.4	mA
lін	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = 2.7 V			20			20	μΑ
Ι <sub>ΙL</sub>	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = 0.5 V			-0.6			-0.6	mA
los <sup>‡</sup>	$V_{CC} = 5.5 \text{ V},$	VO = 0	-100		-225	-100		-225	mA
lozh	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			50			50	μΑ
lozL	$V_{CC} = 5.5 \text{ V},$	$V_0 = 0.5 V$			-50			-50	μΑ
ICCL	V <sub>CC</sub> = 5.5 V			37	60		37	60	mA
Іссн	V <sub>CC</sub> = 5.5 V			2	5		2	5	mA
lccz	V <sub>CC</sub> = 5.5 V			5	8		5	8	mA
C <sub>i</sub>	V <sub>CC</sub> = 5 V,	V <sub>I</sub> = 2.5 V or 0.5 V		6			6		pF
Co	V <sub>CC</sub> = 5 V,	V <sub>O</sub> = 2.5 V or 0.5 V		11			11		pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54BCT373		T373 SN74BCT373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>W</sub>	Pulse duration, LE high	7.5		7.5		7.5		ns
t <sub>su</sub>	Setup time, data before LE↓	2		2		2		ns
th	Hold time, data after LE↓	5.5		5.5		5.5		ns



<sup>‡</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

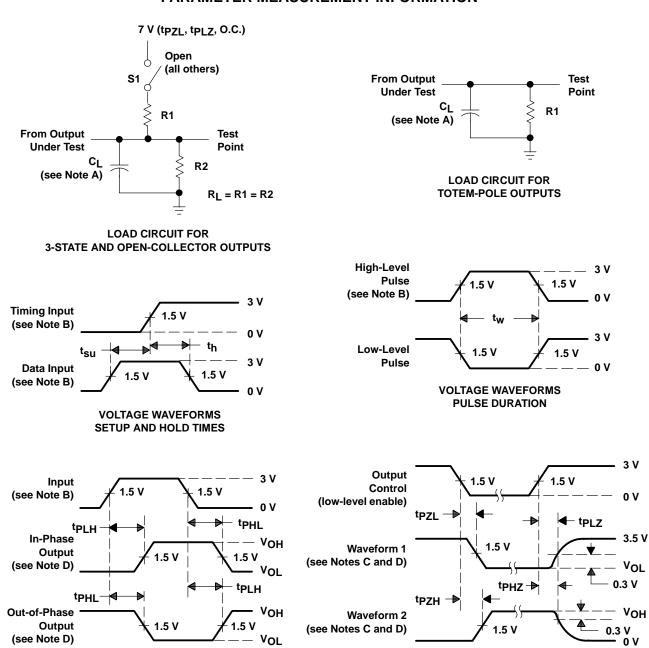
## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C <sub>I</sub> R1 R2 T <sub>A</sub>	$V_{CC}$ = 5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = 25°C		$C_L = 50 \text{ pF},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}C$ $T_A = MIN \text{ to } MAX^{\dagger}$						UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX			
<sup>t</sup> PLH	D	D Q	2	5.9	7.7	1.5	10.1	2	9.3	ns		
t <sub>PHL</sub>		D		2	6.7	8.5	1	10.3	1.5	9.5	115	
t <sub>PLH</sub>	LE	Q	2	6.2	8.2	2	10.1	2	9.3	ns		
<sup>t</sup> PHL	LE		2	5.9	7.8	2	9.2	2	8.8	115		
<sup>t</sup> PZH	ŌĒ	Q	1	7.8	9.6	1	12.3	1	11.8			
tPZL	OE		Q	1	8.2	10.2	1	12.5	1	12	ns	
<sup>t</sup> PHZ	ŌĒ	Q	1	4.9	6.6	1	7.4	1	7	no		
t <sub>PLZ</sub>			1	5	6.7	1	8.1	1	7.4	ns		

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

**VOLTAGE WAVEFORMS** 

PROPAGATION DELAY TIMES (see Note D)

B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $t_f = t_f \leq 2.5$  ns, duty cycle = 50%.

**VOLTAGE WAVEFORMS** 

**ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS** 

- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.
- E. When measuring propagation delay times of 3-state outputs, switch S1 is open.
- F. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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#### PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9074601M2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9074601M2A SNJ54BCT 373FK
5962-9074601MRA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9074601MR A SNJ54BCT373J
SNJ54BCT373FK	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9074601M2A SNJ54BCT 373FK
SNJ54BCT373FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9074601M2A SNJ54BCT 373FK
SNJ54BCT373J	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9074601MR A SNJ54BCT373J
SNJ54BCT373J.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9074601MR A SNJ54BCT373J

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.



# **PACKAGE OPTION ADDENDUM**

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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# **PACKAGE MATERIALS INFORMATION**

www.ti.com 23-May-2025

### **TUBE**



### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9074601M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54BCT373FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54BCT373FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

### 14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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