SDAS230A - DECEMBER 1983 - REVISED AUGUST 1995

- Functionally Equivalent to AMD's AM29821
- Provide Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State
- Buffered Control Inputs to Reduce dc Loading Effects
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

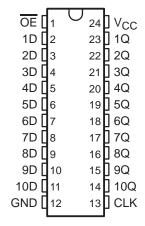
## description

These 10-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

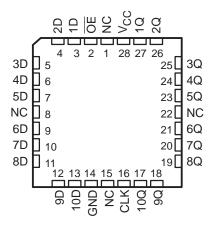
The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are true to the data (D) input.

A buffered output-enable  $(\overline{OE})$  input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

#### SN54AS821A . . . JT PACKAGE SN74AS821A . . . DW OR NT PACKAGE (TOP VIEW)



## SN54AS821A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

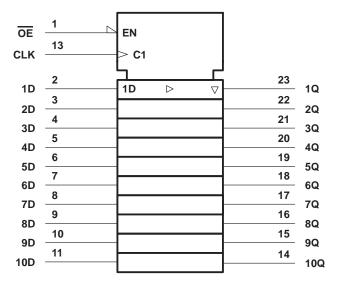
OE does not affect the internal operation of the flip-flops. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS821A is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to  $125^{\circ}$ C. The SN74AS821A is characterized for operation from  $0^{\circ}$ C to  $70^{\circ}$ C.

# FUNCTION TABLE (each flip-flop)

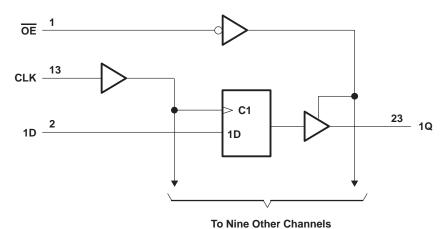
	INPUTS	OUTPUT	
OE	CLK	D	Q
L	1	Н	Н
L	$\uparrow$	L	L
L	L	Χ	Q <sub>0</sub>
Н	Х	Х	Z

## logic symbol†



 $<sup>\</sup>dagger$  This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, and NT packages.

## logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V <sub>CC</sub>	7 V
Input voltage, V <sub>I</sub>	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T <sub>A</sub> : SN54AS821A	−55°C to 125°C
SN74AS821A	0°C to 70°C
Storage temperature range	-65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



SDAS230A - DECEMBER 1983 - REVISED AUGUST 1995

## recommended operating conditions

		SN54AS821A		SN74AS821A			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
IOH	High-level output current			-24			-24	mA
lOL	Low-level output current			32			48	mA
t <sub>W</sub> *	Pulse duration, CLK high or low	9			8			ns
t <sub>su</sub> *	Setup time, data before CLK↑	7			6			ns
t <sub>h</sub> *	Hold time, data after CLK↑	0			0		·	ns
TA	Operating free-air temperature	-55		125	0		70	°C

On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN:	SN54AS821A			SN74AS821A		
PARAMETER	1531 (1	TEST CONDITIONS			MAX	MIN	TYP <sup>†</sup>	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	$I_{I} = -18 \text{ mA}$			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V <sub>CC</sub> -2			V <sub>CC</sub> -2			
Vон	V <sub>CC</sub> = 4.5 V	$I_{OH} = -15 \text{ mA}$	2.4	3.2		2.4	3.2		V
	VCC = 4.5 V	$I_{OH} = -24 \text{ mA}$	2			2			
V	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 32 mA		0.25	0.5				V
VOL	vCC = 4.5 v	I <sub>OL</sub> = 48 mA					0.35	0.5	V
lozh	$V_{CC} = 5.5 V,$	$V_0 = 2.7 \text{ V}$			50			50	μΑ
lozL	$V_{CC} = 5.5 V,$	V <sub>I</sub> = 0.4 V			-50			-50	μΑ
lį	$V_{CC} = 5.5 V,$	V <sub>I</sub> = 7 V			0.1			0.1	mA
lіН	$V_{CC} = 5.5 V,$	V <sub>I</sub> = 2.7 V			20			20	μΑ
Ι <sub>ΙL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V			-0.5			-0.5	mA
IO <sup>‡</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-30		-112	-30		-112	mA
		Outputs high		55	88		55	88	
ICC	V <sub>CC</sub> = 5.5 V	Outputs low		68	109		68	109	mA
		Outputs disabled		70	113		70	113	



<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C. ‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

## SN54AS821A, SN74AS821A 10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

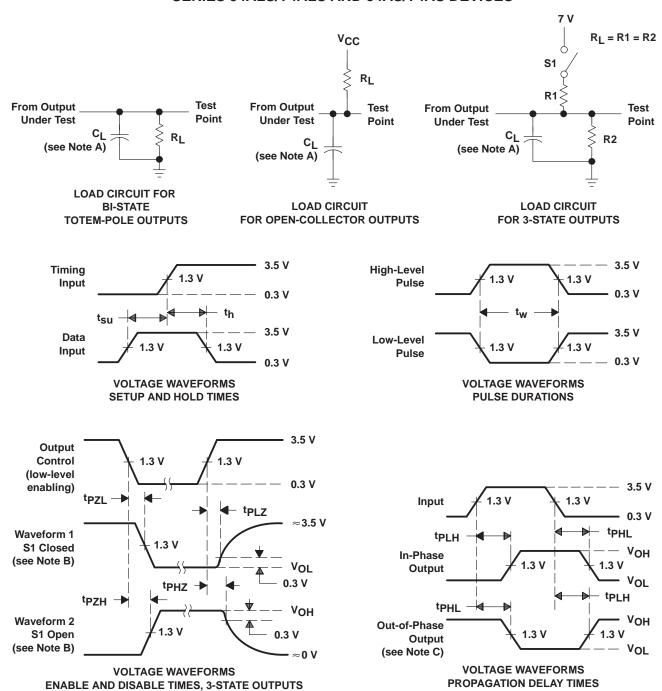
SDAS230A - DECEMBER 1983 - REVISED AUGUST 1995

## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX <sup>†</sup>				UNIT
			SN54AS821A		SN74AS821A		
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	CLK	Am. 0	3.5	9	3.5	7.5	ns
t <sub>PHL</sub>	OLK	Any Q	3.5	14	3.5	13	115
<sup>t</sup> PZH	ŌĒ	Any Q	4	12	3	11	ns
t <sub>PZL</sub>	OE		4	13	4	12	115
<sup>t</sup> PHZ	ŌĒ	Any Q	1	10	1	8	ns
t <sub>PLZ</sub>	)L	Ally Q	1	10	1	8	115

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR  $\leq$  1 MHz,  $t_{\Gamma}$  =  $t_{f}$  = 2 ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



www.ti.com 11-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
5962-9078001MLA	Active	Production	CDIP (JT)   24	15   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9078001ML A
									SNJ54AS821AJT
SN54AS821AJT	Active	Production	CDIP (JT)   24	15   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS821AJT
SN54AS821AJT.A	Active	Production	CDIP (JT)   24	15   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS821AJT
SNJ54AS821AJT	Active	Production	CDIP (JT)   24	15   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9078001ML A SNJ54AS821AJT
SNJ54AS821AJT.A	Active	Production	CDIP (JT)   24	15   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9078001ML A SNJ54AS821AJT

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



## PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2025

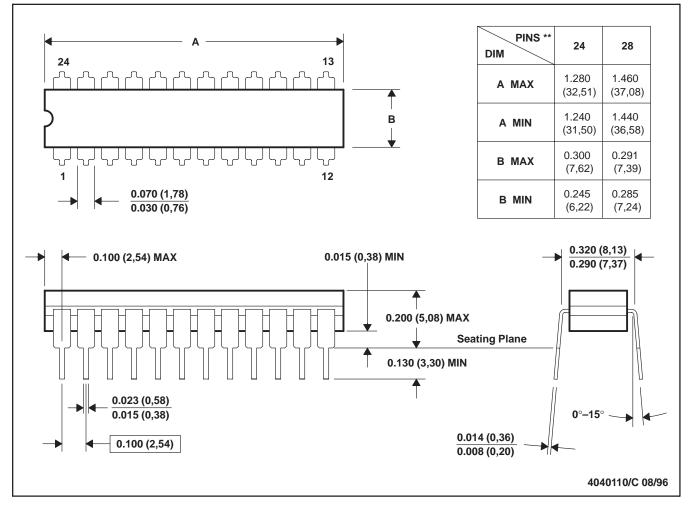
and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## JT (R-GDIP-T\*\*)

#### 24 LEADS SHOWN

#### **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025