SDAS098B - OCTOBER 1984 - REVISED JANUARY 1995

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- T/C Determines True or Complementary Data at Q Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

description

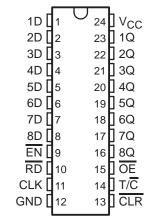
These 8-bit latches are designed specifically for storing the contents of the input data bus and providing the capability of reading back the stored data onto the input data bus. The Q outputs are designed with bus-driving capability.

The edge-triggered flip-flops enter the data on the low-to-high transition of the clock (CLK) input when the enable (\overline{EN}) input is low. Data can be read back onto the data inputs by taking the read (\overline{RD}) input low, in addition to having \overline{EN} low. When \overline{EN} is high, both the read-back and write modes are disabled. Transitions on \overline{EN} should only be made with CLK high to prevent false clocking.

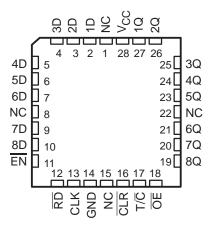
The polarity of the Q outputs can be controlled by the polarity (T/\overline{C}) input. When T/\overline{C} is high, Q is the same as is stored in the flip-flops. When T/\overline{C} is low, the output data is inverted. The Q outputs can be placed in the high-impedance state by taking the output-enable (\overline{OE}) input high. \overline{OE} does not affect the internal operation of the register. Old data can be retained or new data can be entered while the outputs are off.

A low level at the clear ($\overline{\text{CLR}}$) input resets the internal registers low. The clear function is asynchronous and overrides all other register functions.

SN54ALS996 . . . JT PACKAGE SN74ALS996 . . . DW OR NT PACKAGE (TOP VIEW)



SN54ALS996 . . . FK PACKAGE (TOP VIEW)

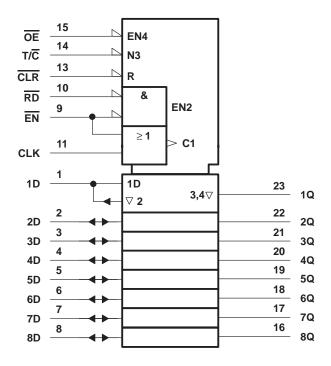


NC - No internal connection

The -1 version of the SN74ALS996 is identical to the standard version, except that the recommended maximum I_{OL} for the -1 version is increased to 48 mA. There is no -1 version of the SN54ALS996.

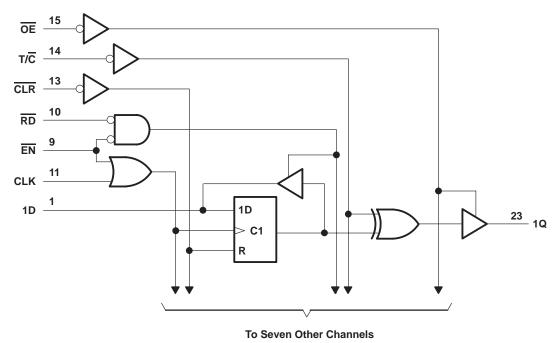
The SN54ALS996 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74ALS996 is characterized for operation from 0°C to 70°C.

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (positive logic)

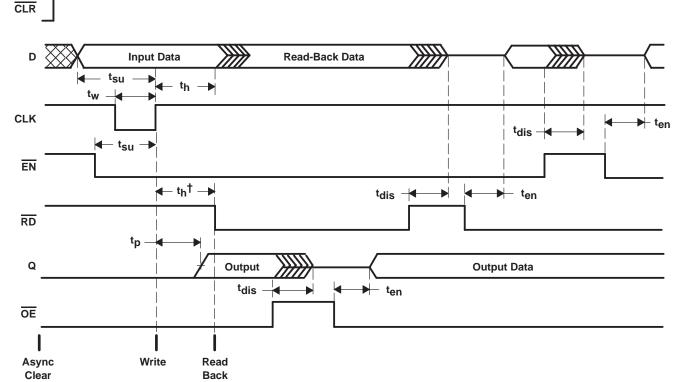


Pin numbers shown are for the DW, JT, and NT packages.



timing diagram

(T/C = H)



[†] This hold time ensures that the read-back circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{CC}	7 V
Input voltage, V _I (OE, RD, EN, CLK, CLR, and T/C)	7 V
Voltage applied to D inputs and to disabled 3-state outputs	5.5 V
Operating free-air temperature range, T _A : SN54ALS996	-55°C to 125°C
SN74ALS996	0°C to 70°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN54ALS996, SN74ALS996 8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

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recommended operating conditions

			SN	54ALS9	96	SN	74ALS9	96	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
		All inputs				2			
۷ _{IH}	High-level input voltage	All inputs except OE, RD	2						V
		ŌE, RD	2.2						
V_{IL}	Low-level input voltage				8.0			8.0	V
	LPak lavel sytematics	Q			-1			-2.6	4
ЮН	High-level output current	D			-0.4			-0.4	mA
					12			24	
loL	Low-level output current	Q						48†	mA
		D			8			8	<u>]</u>
fclock	Clock frequency		0		35	0		35	MHZ
		CLR low	10			10			
t _W	Pulse duration	CLK low	14.5			14.5			ns
		CLK high				14.5			
		Data before CLK↑	15			15			
	Catum times	EN low before CLK↑	10			10			
t _{su}	Setup time	CLK high before EN↑‡	15			15			ns
		CLR high (inactive) before CLK↑	10			10			
		Data after CLK↑	1			0			
t _h	Hold time	EN low after CLK↑	5			5			ns
		RD high after CLK↑§ 5				5			
TA	Operating free-air temperatur	e	-55		125	0		70	°C

[†] Applies only to the -1 version and only if V_{CC} is maintained between 4.75 V and 5.25 V † This setup time ensures that EN will not false clock the data register. § This hold time ensures that there will be no conflict on the input data bus.

SN54ALS996, SN74ALS996 8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER			SN	54ALS9	96	SN				
P/	ARAMETER	TEST C	ONDITIONS	MIN	TYP†	MAX	MIN	TYP [†]	MAX	UNIT
VIK		V _{CC} = 4.5 V,	I _I = –18 mA			-1.2			-1.2	V
	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2	2		V _{CC} -2	2		
∨он		V 45V	I _{OH} = – 1 mA	2.4	3.2					V
	Q	V _{CC} = 4.5 V	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
	D	\\ 45\\	$I_{OL} = 4 \text{ mA}$		0.25	0.4				
	D	V _{CC} = 4.5 V	$I_{OL} = 8 \text{ mA}$					0.35	0.5	
VOL			$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V
	Q	V _{CC} = 4.5 V	$I_{OL} = 24 \text{ mA}$					0.35	0.5	
			$I_{OL} = 48 \text{ mA}^{\ddagger}$					0.35	0.5	
lozh	Q	V _{CC} = 5.5 V,	V _O = 2.7 V			20			20	μΑ
lozL	Q	$V_{CC} = 5.5 V,$	V _O = 0.4 V			-20			-20	μΑ
	D inputs	\/ F.5.\/	V _I = 5.5 V			0.1			0.1	A
1 ₁	All others	V _{CC} = 5.5 V	V _I = 7 V			0.1			0.1	mA
Livia	D inputs§	V 55V				20			20	^
۱н	All others	$V_{CC} = 5.5 \text{ V},$	$V_1 = 2.7 \text{ V}$			20			20	μΑ
	D inputs§	§ 7				-0.1			-0.1	0
I _I L	All others	$V_{CC} = 5.5 \text{ V},$	$V_{I} = 0.4 \text{ V}$		-0.1				-0.1	mA
IOI		$\frac{V_{CC}}{CLR} = 5.5 \text{ V},$	V _O = 2.25 V	-20		-112	-30		-112	mA
			Outputs high		35	55		35	55	
ICC		$\frac{\text{V}_{CC}}{\text{EN, RD low}}$	Outputs low		55	85		55	85	mA
		ETT, NO IOW	Outputs disabled		42	65		42	65	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] Applies only to the -1 version and only if V_{CC} is maintained between 4.75 V and 5.25 V

 $[\]mbox{\$ For I/O ports (Q}_{\mbox{A}}$ thru Q}_{\mbox{H}}), the parameters I}_{\mbox{IH}} and I}_{\mbox{IL}} include the off-state output current.

The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

SN54ALS996, SN74ALS996 8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

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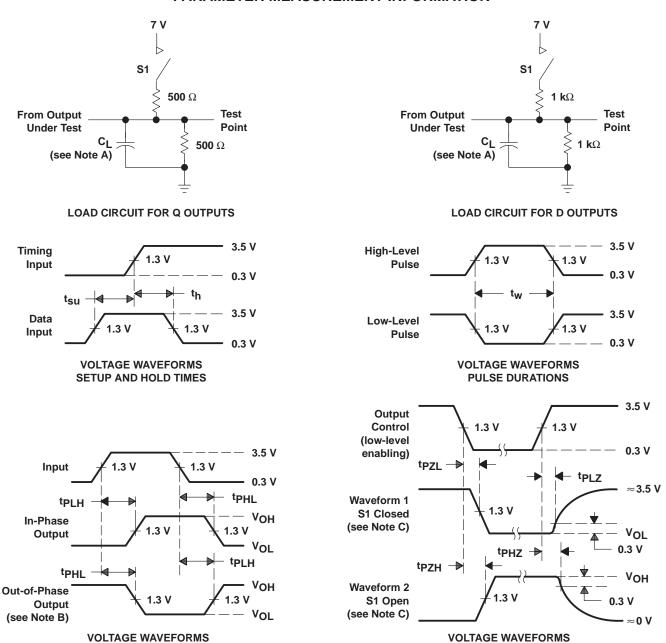
switching characteristics (see Figure 1)

PARAMETER	FROM	то	V _C C _L T _A	UNIT			
	(INPUT)	(OUTPUT)	SN54A	LS996	SN74A		
			MIN	MAX	MIN	MAX	
f _{max}			35		35		MHz
^t PLH	CLK (T/C = H or L)	0	5	30	5	28	
^t PHL		Q	5	24	5	28	ns
^t PLH	$\overline{\text{CLR}} (T/\overline{\text{C}} = \text{L})$	Q	5	27	7	27	20
^t PHL	$\overline{\text{CLR}} (T/\overline{\text{C}} = \text{H})$	Q	5	23	7	23	ns
^t PLH	T/C	0	4	23	5	23	20
^t PHL		Q	5	23	5	23	ns
t _{PHL}	CLR	D	5	30	8	30	ns
t _{en} ‡			2	18	3	16	
t _{dis} §	RD	D	1	19	3	19	ns
t _{en} ‡		6	2	17	3	16	
t _{dis} §	ĒN	D	1	19	3	19	ns
t _{en} ‡	ŌĒ	Q	2	15	4	15	nc
t _{dis} §	OE .	3	1	11	1	10	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. ‡ ten = tpzh or tpzL § tdis = tphz or tpLz

ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

PROPAGATION DELAY TIMES

- B. When measuring propagation delay times of 3-state outputs, switch S1 is open.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. All input pulses have the following characteristics: PRR \leq 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.

Figure 1. Load Circuits and Voltage Waveforms

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-89945013A	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 89945013A SNJ54ALS 996FK
5962-8994501LA	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8994501LA SNJ54ALS996JT
SN74ALS996DW	Obsolete	Production	SOIC (DW) 24	-	-	Call TI	Call TI	0 to 70	ALS996
SN74ALS996DWR	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS996
SN74ALS996DWR.A	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS996
SNJ54ALS996FK	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 89945013A SNJ54ALS 996FK
SNJ54ALS996FK.A	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 89945013A SNJ54ALS 996FK
SNJ54ALS996JT	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8994501LA SNJ54ALS996JT
SNJ54ALS996JT.A	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8994501LA SNJ54ALS996JT

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OPTION ADDENDUM

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(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54ALS996, SN74ALS996:

Catalog: SN74ALS996

Military: SN54ALS996

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS996DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74ALS996DWR	SOIC	DW	24	2000	350.0	350.0	43.0	

JT (R-GDIP-T**)

24 LEADS SHOWN

CERAMIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



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Last updated 10/2025