SDAS036D - APRIL 1982 - REVISED AUGUST 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

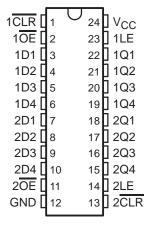
description

These dual 4-bit D-type latches feature 3-state outputs designed specifically for bus driving. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

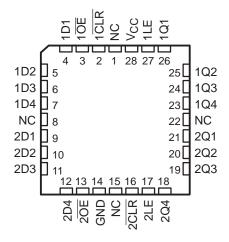
The dual 4-bit latches are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs in true form, according to the function table. When LE is low, the outputs are latched. When the clear (\overline{CLR}) input goes low, the Q outputs go low independently of LE. The outputs are in the high-impedance state when the output-enable (\overline{OE}) input is at a high logic level.

The SN54ALS873B and SN54AS873A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS873B and SN74AS873A are characterized for operation from 0°C to 70°C.

SN54ALS873B, SN54AS873A . . . JT PACKAGE SN74ALS873B, SN74AS873A . . . DW OR NT PACKAGE (TOP VIEW)



SN54ALS873B, SN54AS873A . . . FK PACKAGE (TOP VIEW)



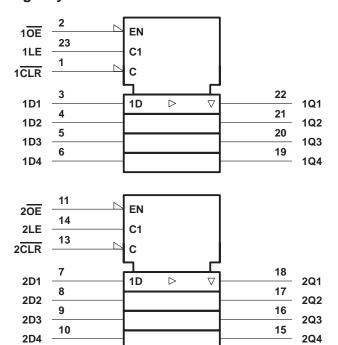
NC - No internal connection

FUNCTION TABLE (each latch)

	INPU	JTS		OUTPUT
ŌĒ	CLR	LE	D	Q
L	L	Χ	Х	L
L	Н	Н	Н	Н
L	Н	Н	L	L
L	Н	L	Χ	Q_0
Н	X	Χ	Χ	Z

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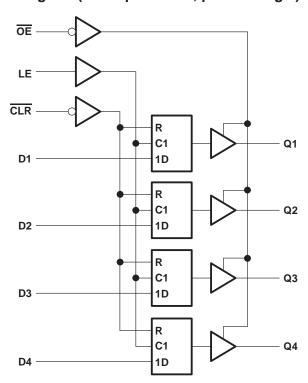
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (each quad latch, positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{CC}	$\dots \dots $
Input voltage, V _I	7 V
Voltage applied to a disabled 3-state output	
Operating free-air temperature range, T _A : SN54ALS873B	55°C to 125°C
SN74ALS873B	0°C to 70°C
Storage temperature range	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SNS	4ALS87	'3B	SN74ALS873B			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			-1			-2.6	mA
loL	Low-level output current			12			24	mA
TA	Operating free-air temperature	-55		125	0		70	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

24244555	TEST CONDITIONS		SN5	4ALS87	'3B	SN7	3B	LINUT	
PARAMETER	TEST CO	ONDITIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2	!		V _{CC} -2	2		
∨он	V 45 V	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V
	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
.,	V _{CC} = 4.5 V	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	٧
VOL		I _{OL} = 24 mA					0.35	0.5	V
lozh	V _{CC} = 5.5 V,	V _O = 2.7 V			20			20	μΑ
lozL	V _{CC} = 5.5 V,	V _O = 0.4 V			-20			-20	μΑ
Ι _Ι	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
lін	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
I _{IL}	V _{CC} = 5.5 V,	V _I = 0.4 V			- 0.2			- 0.2	mA
1 ₀ ‡	$V_{CC} = 5.5 \text{ V},$	V _O = 2.25 V	-20		-112	-30		-112	mA
		Outputs high		11	21		11	21	mA
Icc	V _{CC} = 5.5 V	Outputs low		16	29		16	29	
		Outputs disabled		20	31		20	31	

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54AL	S873B	SN74AL		
			MIN	MAX	MIN	MAX	UNIT
	Pulse duration	CLR low	15		15		
t _W		LE high	10		10		ns
t _{su}	Setup time, data before LE↓		10		10		ns
th	Hold time, data after LE↓		7		7		ns

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L : R1 : R2 :	C = 4.5 V = 50 pF, = 500 Ω , = 500 Ω , = MIN to			UNIT
			SN54ALS873B		SN74AL	S873B	
			MIN	MAX	MIN	MAX	
t _{PLH}	D	0	2	23	2	14	20
^t PHL	D	Q	2	17	2	14	ns
tPLH		0	8	31	8	22	
^t PHL	LE	Q	8	26	8	21	ns
^t PHL	CLR	Q	6	27	6	20	ns
^t PZH	ŌĒ	_	4	24	4	18	
t _{PZL}	OE	Q	4	23	4	18	ns
^t PHZ	ŌĒ	Q	2	12	2	10	nc
t _{PLZ}	OE	ď	2	30	2	15	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{CC}	7 V
Input voltage, V _I	7 V
Voltage applied to a disabled 3-state output	
Operating free-air temperature range, T _A : SN54AS873A	. −55°C to 125°C
SN74AS873A	0°C to 70°C
Storage temperature range	. −65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN	54AS873	3A	SN74AS873A			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			8.0			0.8	V
ІОН	High-level output current			-12			-15	mA
lOL	Low-level output current			32			48	mA
TA	Operating free-air temperature	-55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

242445752	TEST CONDITIONS		SN	54AS87	3A	SN	74AS873	BA	UNIT
PARAMETER	TEST C	ONDITIONS	MIN	TYP	MAX	MIN	TYP†	MAX	UNII
VIK	$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -2	2		VCC-2	2		
∨он	V 45.V	I _{OH} = -12 mA	2.4	3.2					V
	V _{CC} = 4.5 V	I _{OH} = -15 mA				2.4	3.3		
V	V _{CC} = 4.5 V	I _{OL} = 32 mA		0.25	0.5				.,
V _{OL}		I _{OL} = 48 mA					0.35	0.5	V
lozh	V _{CC} = 5.5 V,	V _O = 2.7 V			50			50	μΑ
I _{OZL}	V _{CC} = 5.5 V,	V _O = 0.4 V			-50			-50	μΑ
lį	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
lін	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
I _{IL}	V _{CC} = 5.5 V,	V _I = 0.4 V			- 0.5			- 0.5	mA
I _O ‡	$V_{CC} = 5.5 \text{ V},$	V _O = 2.25 V	-30		-112	-30		-112	mA
		Outputs high		68	110		68	110	⊣ I
ICC	V _{CC} = 5.5 V	Outputs low		67	109		67	109	
		Outputs disabled		80	129		80	129	

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54AS	8873A	SN74AS	S873A	
			MIN	MAX	MIN	MAX	UNIT
. *		R low	5		5		
t _W *	Pulse duration LE	high	6		5		ns
t _{su} *	Setup time, data before LE↓		2		2		ns
th*	Hold time, data after LE↓	·	4.5		4.5		ns

^{*} On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

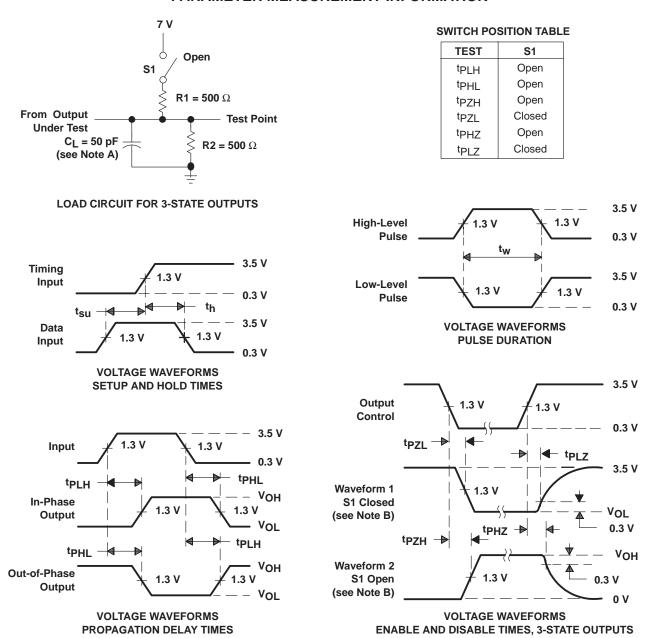
SN54ALS873B, SN54AS873A, SN74ALS873B, SN74AS873A DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS SDAS036D - APRIL 1982 - REVISED AUGUST 1995

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _C C _L R1 R2 T _A	UNIT			
			SN54A	S873A	SN74A	S873A	
			MIN	MAX	MIN	MAX	
t _{PLH}	- D	0	3	12.5	3	9.5	ns
^t PHL		Q	3	8.5	3	7.5	
^t PLH		0	6	15.5	6	13	
^t PHL	LE	Q	4	9	4	7.5	ns
^t PHL	CLR	Q	3	10.5	3	9	ns
^t PZH	ŌĒ	0	2	8	2	6.5	
t _{PZL}	OE	Q	4	11	4	10.5	ns
^t PHZ	ŌĒ	Q	2	8	2	7.5	ns
^t PLZ	OE	Q Q	2	8.5	2	7.5	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq 2$ ns. $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
84032013A	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84032013A SNJ54ALS 873BFK
8403201LA	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8403201LA SNJ54ALS873BJT
SN74ALS873BDW	Obsolete	Production	SOIC (DW) 24	-	-	Call TI	Call TI	0 to 70	ALS873B
SN74ALS873BDWR	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS873B
SN74ALS873BDWR.A	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS873B
SNJ54ALS873BFK	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84032013A SNJ54ALS 873BFK
SNJ54ALS873BFK.A	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84032013A SNJ54ALS 873BFK
SNJ54ALS873BJT	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8403201LA SNJ54ALS873BJT
SNJ54ALS873BJT.A	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8403201LA SNJ54ALS873BJT

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

PACKAGE OPTION ADDENDUM

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54ALS873B, SN74ALS873B:

Catalog: SN74ALS873B

Military: SN54ALS873B

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

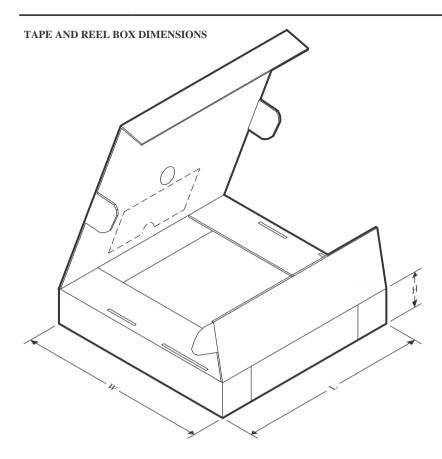


*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS873BDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS873BDWR	SOIC	DW	24	2000	350.0	350.0	43.0

JT (R-GDIP-T**)

24 LEADS SHOWN

CERAMIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



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