

SN54ALS580B, SN74ALS580B, SN74AS580 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SDAS277 – JANUARY 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Inverting-Logic Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N) and Ceramic (J) 300-mil DIPs, and Ceramic Flat (W) Packages

description

These octal D-type transparent latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

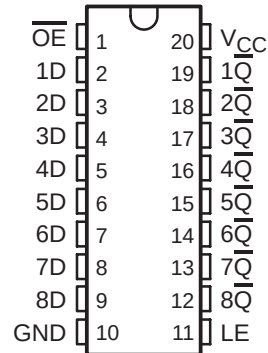
While the latch-enable (LE) input is high, outputs ($\overline{Q}$) respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

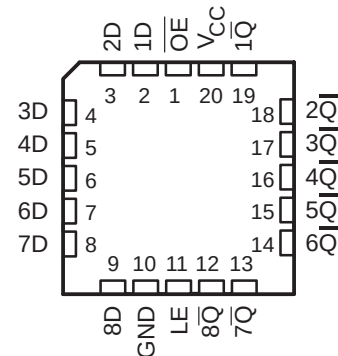
$\overline{OE}$ does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS580B is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS580B and SN74AS580 are characterized for operation from 0°C to 70°C .

SN54ALS580B . . . J OR W PACKAGE
SN74ALS580B, SN74AS580 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS580B . . . FK PACKAGE
(TOP VIEW)

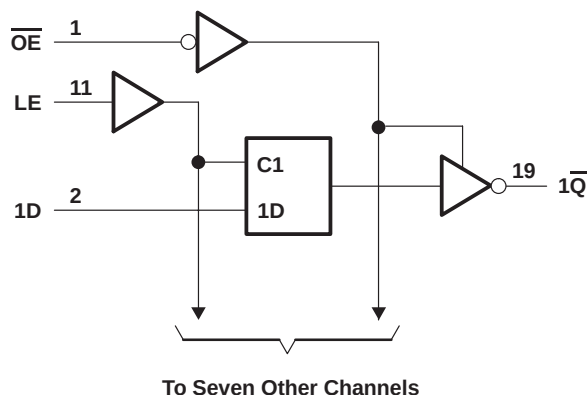
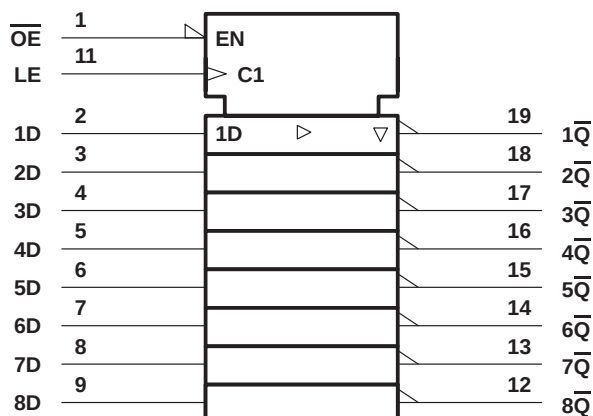


FUNCTION TABLE
(each latch)

INPUTS			OUTPUT $\overline{Q}$
$\overline{OE}$	LE	D	
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN54ALS580B	-55°C to 125°C
SN74ALS580B	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS580B			SN74ALS580B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			−1			−2.6	mA
I _{OL}	Low-level output current			12			24	mA
t _w	Pulse duration, LE high	15			15			ns
t _{su}	Setup time, data before LE↓	20			10			ns
t _h	Hold time, data after LE↓	12			10			ns
T _A	Operating free-air temperature	−55		125	0		70	°C

SN54ALS580B, SN74ALS580B, SN74AS580

OCTAL D-TYPE TRANSPARENT LATCHES

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS580B			SN74ALS580B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = −18 mA		−1.2			−1.2			V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = −0.4 mA		V _{CC} − 2			V _{CC} − 2			V
	V _{CC} = 4.5 V	I _{OH} = −1 mA	2.4 3.3						
		I _{OH} = −2.6 mA			2.4 3.2				
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25 0.4		0.25 0.4		V		
		I _{OL} = 24 mA			0.35 0.5				
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V	20			20			μA	
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V	−20			−20			μA	
I _I	V _{CC} = 5.5 V, V _I = 7 V	0.1			0.1			mA	
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V	20			20			μA	
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V	−0.13			−0.1			mA	
I _O [‡]	V _{CC} = 5.5 V, V _O = 2.25 V	−20	−112		−30	−112		mA	
I _{CC}	V _{CC} = 5.5 V	Outputs high	10 17		10 17		mA		
		Outputs low	16 26		16 26				
		Outputs disabled	17 29		17 29				

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX§				UNIT
			SN54ALS580B		SN74ALS580B		
			MIN	MAX	MIN	MAX	
t _{PLH}	D	Q	3	26	3	18	ns
t _{PHL}			3	15	3	14	
t _{PLH}	LE	Q	8	29	6	22	ns
t _{PHL}			4	22	6	21	
t _{PZH}	OE	Q	4	25	3	18	ns
t _{PZL}			4	21	4	18	
t _{PHZ}	OE	Q	2	12	1	10	ns
t _{PLZ}			3	22	1	15	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS580B, SN74ALS580B, SN74AS580

OCTAL D-TYPE TRANSPARENT LATCHES

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN74AS580	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN74AS580			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			48	mA
t_W^*	Pulse duration, LE high	2			ns
t_{su}^*	Setup time, data before LE↓	2			ns
t_h^*	Hold time, data after LE↓	3			ns
T_A	Operating free-air temperature	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN74AS580			UNIT
		MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -2$ mA	$V_{CC} - 2$			V
	$V_{CC} = 4.5$ V, $I_{OH} = -15$ mA	2.4	3.3		
V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 48$ mA		0.33	0.5	V
I_{OZH}	$V_{CC} = 5.5$ V, $V_O = 2.7$ V			50	μA
I_{OZL}	$V_{CC} = 5.5$ V, $V_O = 0.4$ V			–50	μA
I_I	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20	μA
I_{IL}	$V_{CC} = 5.5$ V, $V_I = 0.4$ V			–0.5	mA
$I_O^§$	$V_{CC} = 5.5$ V, $V_O = 2.25$ V	–30		–112	mA
I_{CC}	$V_{CC} = 5.5$ V	Outputs high		62	mA
		Outputs low		65	
		Outputs disabled		71	

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .



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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†		UNIT
			SN74AS580		
			MIN	MAX	
t _{PLH}	D	$\overline{Q}$	3	7.5	ns
t _{PHL}			3	7	
t _{PLH}	LE	$\overline{Q}$	5	9	ns
t _{PHL}			4	8	
t _{PZH}	$\overline{OE}$	$\overline{Q}$	2	6.5	ns
t _{PZL}			4	9.5	
t _{PHZ}	$\overline{OE}$	$\overline{Q}$	2	6.5	ns
t _{PLZ}			2	7	

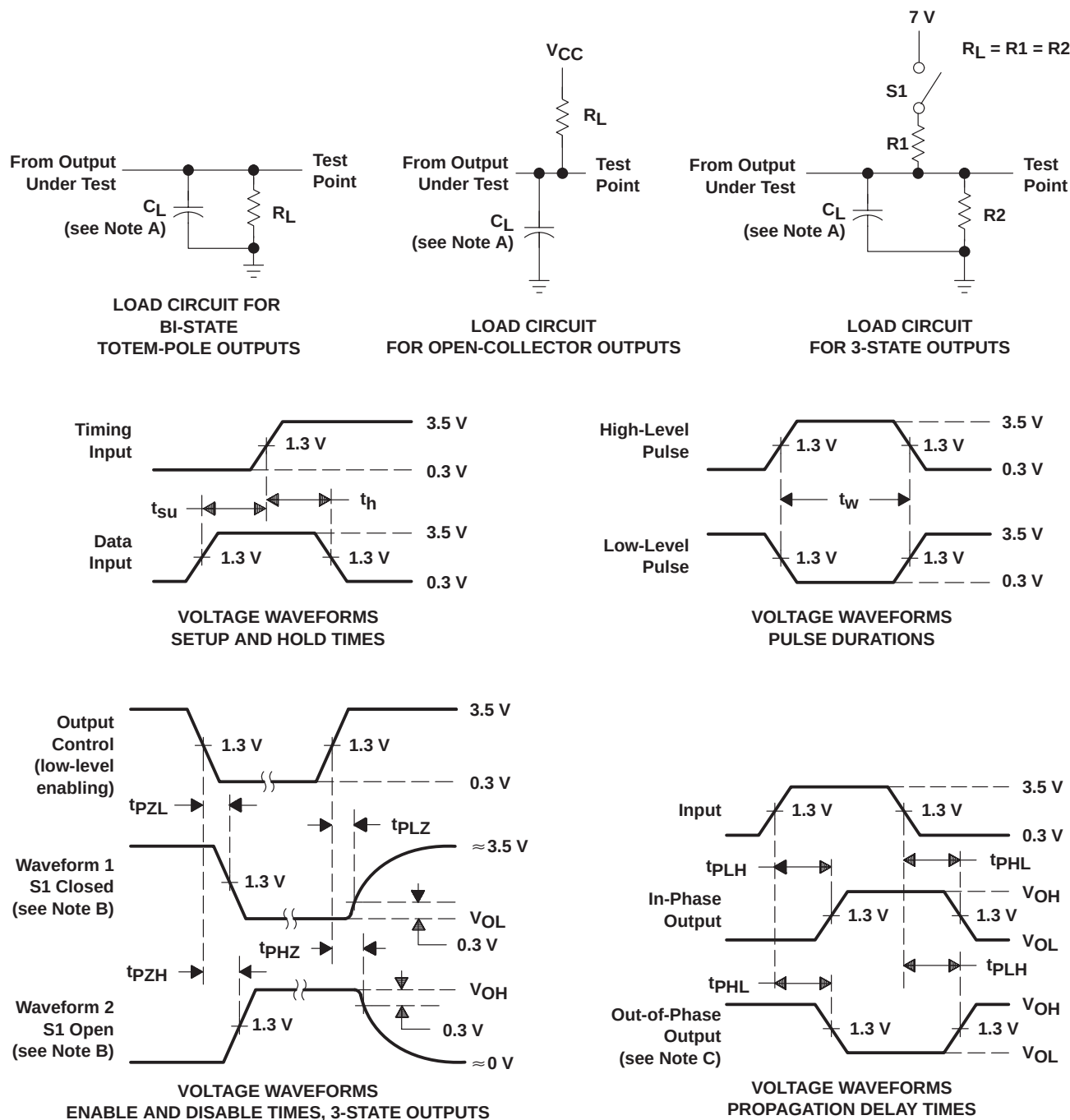
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS580B, SN74ALS580B, SN74AS580 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: PRR $\leq$ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
84012022A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84012022A SNJ54ALS 580BFBK
8401202RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8401202RA SNJ54ALS580BJ
8401202SA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8401202SA SNJ54ALS580BW
SN54ALS580BJ	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS580BJ
SN54ALS580BJ.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS580BJ
SN74ALS580BN	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS580BN
SN74ALS580BN.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS580BN
SNJ54ALS580BFBK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84012022A SNJ54ALS 580BFBK
SNJ54ALS580BFBK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84012022A SNJ54ALS 580BFBK
SNJ54ALS580BJ	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8401202RA SNJ54ALS580BJ
SNJ54ALS580BJ.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8401202RA SNJ54ALS580BJ
SNJ54ALS580BW	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8401202SA SNJ54ALS580BW
SNJ54ALS580BW.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8401202SA SNJ54ALS580BW

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54ALS580B, SN74ALS580B :

- Catalog : [SN74ALS580B](#)
- Military : [SN54ALS580B](#)

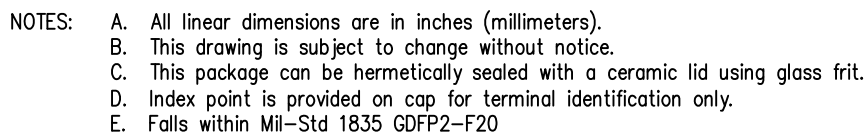
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE


*All dimensions are nominal

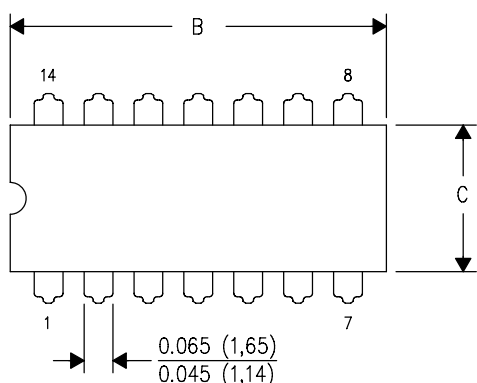
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
84012022A	FK	LCCC	20	55	506.98	12.06	2030	NA
8401202SA	W	CFP	20	25	506.98	26.16	6220	NA
SN74ALS580BN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS580BN.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ALS580BFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS580BFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS580BW	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54ALS580BW.A	W	CFP	20	25	506.98	26.16	6220	NA



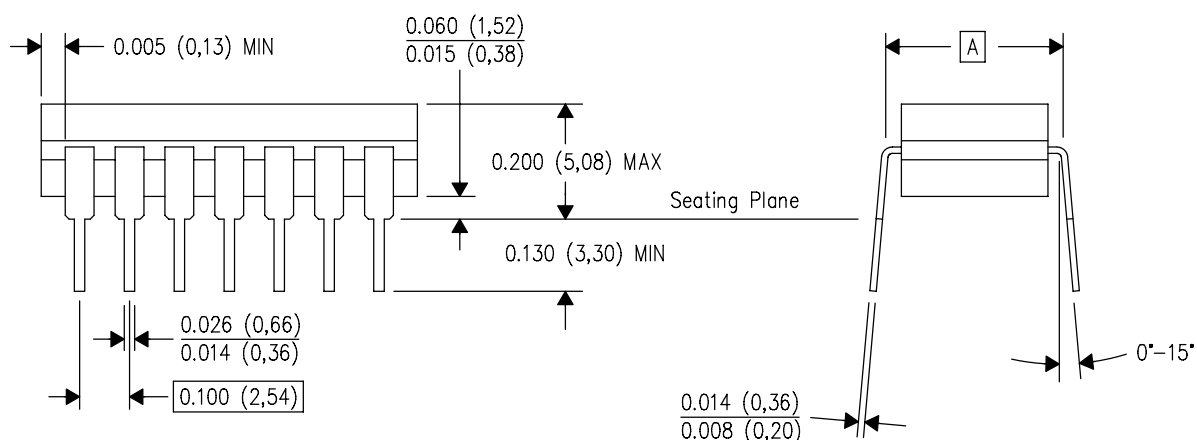
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

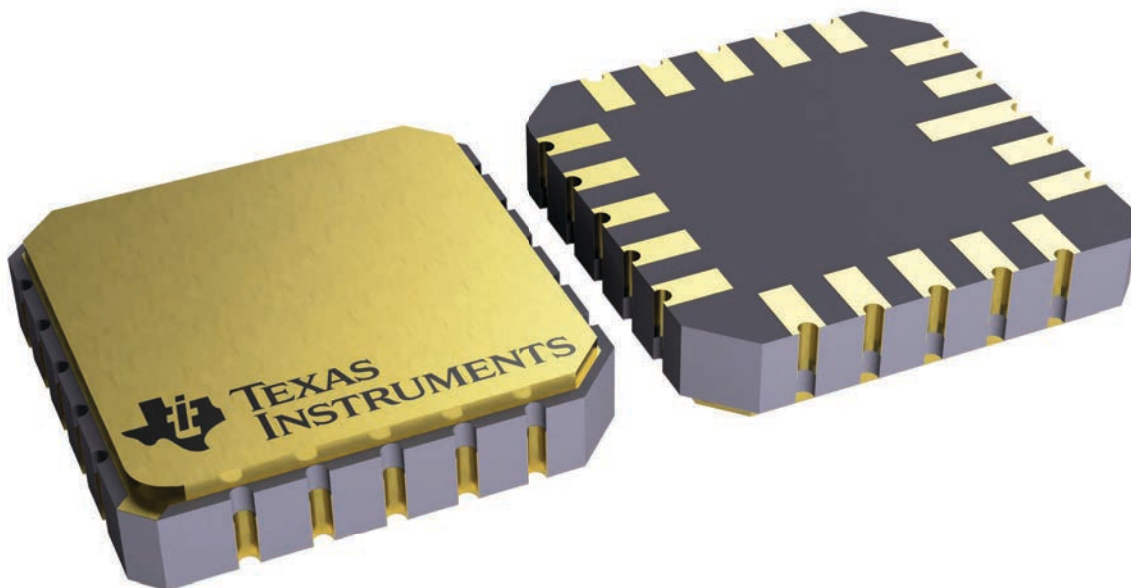
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

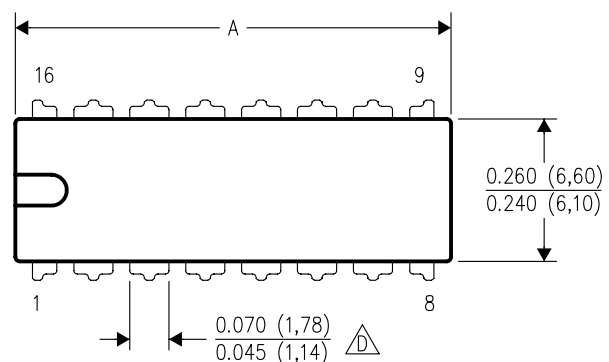


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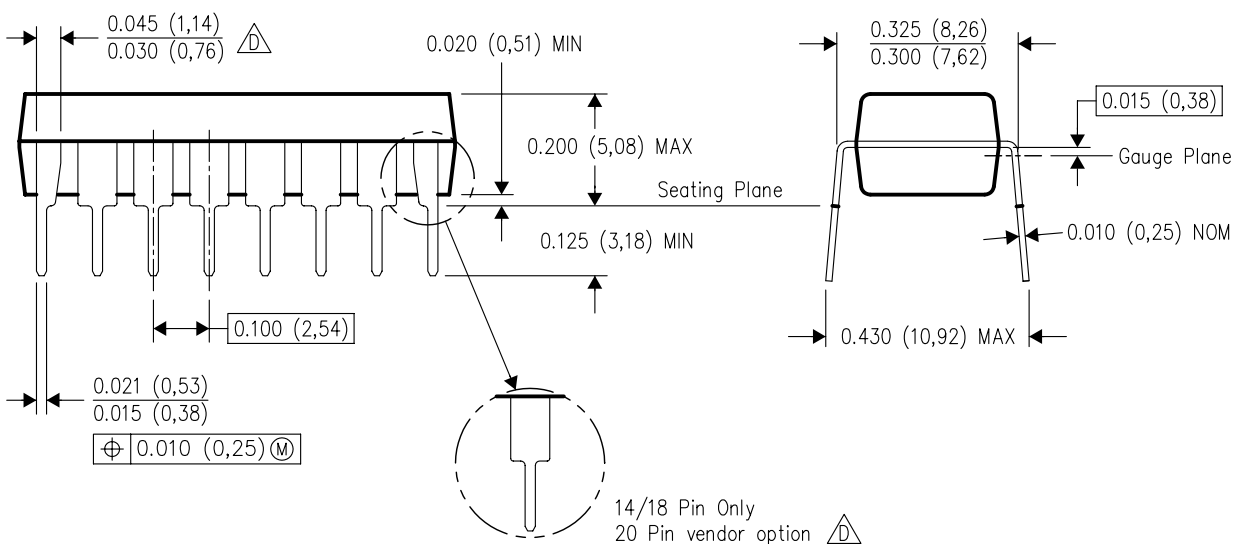
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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