## SN54ALS564B, SN74ALS564B OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS164B - APRIL 1982 - REVISED JANUARY 1995

- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Buffered Control Inputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N) and Ceramic (J) 300-mil DIPs, and Ceramic Flat (W) Packages

#### description

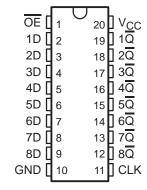
These octal D-type edge-triggered flip-flops feature inverting 3-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops enter data on the low-to-high transition of the clock (CLK) input.

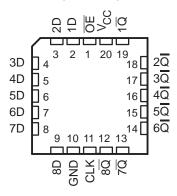
The output-enable  $(\overline{OE})$  input does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS564B is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ALS564B is characterized for operation from 0°C to 70°C.

SN54ALS564B...J OR W PACKAGE SN74ALS564B...DW OR N PACKAGE (TOP VIEW)



SN54ALS564B . . . FK PACKAGE (TOP VIEW)



## FUNCTION TABLE (each flip-flop)

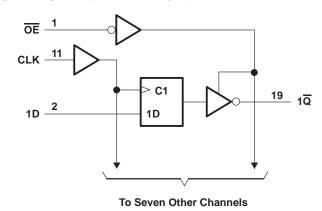
	INPUTS	OUTPUT	
OE	CLK	D	Q
L	$\uparrow$	Н	L
L	$\uparrow$	L	Н
L	L	Χ	$\overline{Q}_0$
Н	X	Χ	Z

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#### logic symbol<sup>†</sup>

#### OE ΕN CLK > C1 2 19 1D 1Q 1D 18 3 2D 2Q 17 4 3Q 3D 5 16 4D 4Q 15 6 5D 5Q 7 14 6D 6Q 8 13 7Q 7D 9 12 8Q 8D

#### logic diagram (positive logic)



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V <sub>CC</sub>	7 V
Input voltage, V <sub>I</sub>	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T <sub>A</sub> : SN54ALS564B	−55°C to 125°C
SN74ALS564B	0°C to 70°C
Storage temperature range	-65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN54ALS564B		SN7	4ALS56	4B	UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vсс	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
IOH	High-level output current			-1			-2.6	mA
loL	Low-level output current			12			24	mA
fclock	Clock frequency	0		22	0		30	MHz
t <sub>W</sub>	Pulse duration, CLK high or low	25			14			ns
t <sub>su</sub>	Setup time, data before CLK↑	15			15			ns
th	Hold time, data after CLK↑	4			0			ns
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

## SN54ALS564B, SN74ALS564B OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS **WITH 3-STATE OUTPUTS**

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			4ALS56	4B	SN7	4ALS56	4B	UNIT	
PARAWETER	lESI CC	MUITIONS	MIN	TYP <sup>†</sup>	MAX	MIN	TYP†	MAX	UNIT	
VIK	V <sub>CC</sub> = 4.5 V,	$I_{I} = -18 \text{ mA}$			-1.2			-1.2	V	
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V <sub>CC</sub> -2	2		V <sub>CC</sub> -2				
Voн	V <sub>CC</sub> = 4.5 V	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V	
	vCC = 4.5 v	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2			
Vai	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 12 mA		0.25	0.4		0.25	0.4	V	
VOL	VCC = 4.5 V	I <sub>OL</sub> = 24 mA					0.35	0.5	٧	
lozh	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			20			20	μΑ	
lozL	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.4 V			-20			-20	μΑ	
l <sub>l</sub>	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = 7 V			0.1			0.1	mA	
lіН	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = 2.7 V			20			20	μΑ	
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V			-0.2			-0.2	mA	
I <sub>O</sub> ‡	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-20		-112	-30		-112	mA	
		Outputs high		10	18		10	18		
Icc	V <sub>CC</sub> = 5.5 V	Outputs low		15	24		15	24	mA	
		Outputs disabled		16	30		16	30		

#### switching characteristics (see Figure 1)

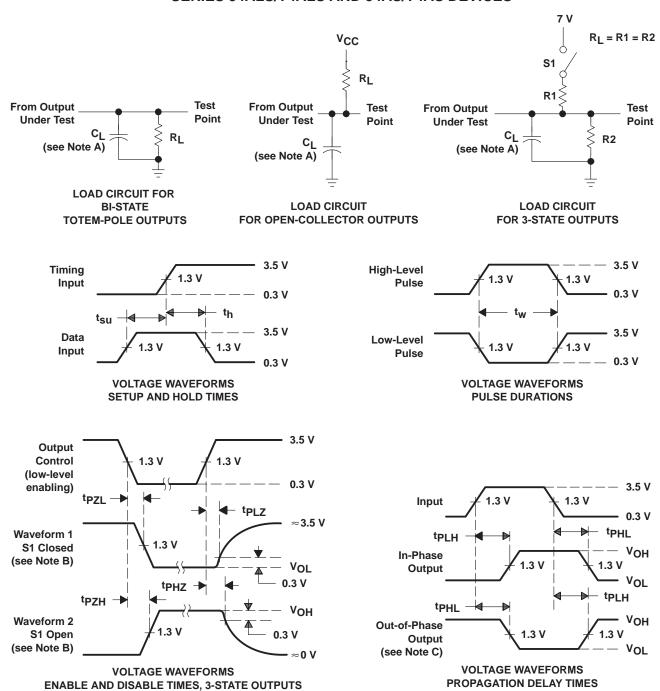
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C <sub>L</sub> R1 R2	_ = 50 pF   = 500	2,	,	UNIT	
			SN54AL	S564B	SN74AL			
			MIN	MAX	MIN	MAX		
f <sub>max</sub>			22		30		MHz	
tPLH	CLK	A	4	24	3	14	ns	
t <sub>PHL</sub>	OLK	Any Q	4	20	4	14	115	
<sup>t</sup> PZH	ŌĒ	Any Q	4	24	3	18	ns	
t <sub>PZL</sub>	OE	Any Q	3	23	4	18	115	
<sup>t</sup> PHZ	ŌĒ	Any Q	2	14	1	10		
t <sub>PLZ</sub>	OL .	Ally Q	3	29	2	15	ns	

<sup>§</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C. ‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

#### PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
  - D. All input pulses have the following characteristics:  $PRR \le 1$  MHz,  $t_f = t_f = 2$  ns, duty cycle = 50%.
  - E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
5962-8872801RA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8872801RA SNJ54ALS564BJ
SN74ALS564BDW	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS564B
SN74ALS564BDW.A	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS564B
SN74ALS564BN	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS564BN
SN74ALS564BN.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS564BN
SN74ALS564BNSR	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS564B
SN74ALS564BNSR.A	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS564B
SNJ54ALS564BJ	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8872801RA SNJ54ALS564BJ
SNJ54ALS564BJ.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8872801RA SNJ54ALS564BJ

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

### **PACKAGE OPTION ADDENDUM**

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#### OTHER QUALIFIED VERSIONS OF SN54ALS564B, SN74ALS564B:

Catalog : SN74ALS564B

Military: SN54ALS564B

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

## **PACKAGE MATERIALS INFORMATION**

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#### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS564BNSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

## **PACKAGE MATERIALS INFORMATION**

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#### \*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
I	SN74ALS564BNSR	SOP	NS	20	2000	356.0	356.0	45.0

## **PACKAGE MATERIALS INFORMATION**

www.ti.com 24-Jul-2025

#### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ALS564BDW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS564BDW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS564BN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS564BN.A	N	PDIP	20	20	506	13.97	11230	4.32

#### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



#### **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

## 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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