SN54ALS299, SN74ALS299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

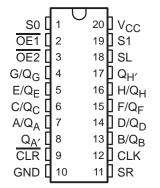
SDAS220B - DECEMBER 1982 - REVISED DECEMBER 1994

- Multiplexed I/O Ports Provide Improved Bit Density
- Four Modes of Operation:
 - Hold (Store)
 - Shift Right
 - Shift Left
 - Load Data
- Operate With Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for n-Bit Word Lengths
- Direct Overriding Clear
- Applications:
 - Stacked or Push-Down Registers
 - Buffer Storage
 - Accumulator Registers
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

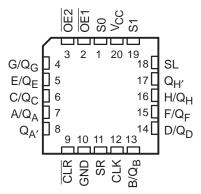
description

These 8-bit universal shift/storage registers feature multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select (S0, S1) inputs and two outputenable (OE1, OE2) inputs can be used to choose the modes of operation listed in the function table.

SN54ALS299 . . . J PACKAGE SN74ALS299 . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS299 . . . FK PACKAGE (TOP VIEW)



Synchronous parallel loading is accomplished by taking both S0 and S1 high. This places the 3-state outputs in the high-impedance state and permits data applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously when the clear (CLR) input is low. Taking either OE1 or OE2 high disables the outputs, but has no effect on clearing, shifting, or storing data.

The SN54ALS299 is characterized for operation over the full military temperature range of -55° C to 125° C. The SN74ALS299 is characterized for operation from 0° C to 70° C.

SN54ALS299, SN74ALS299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

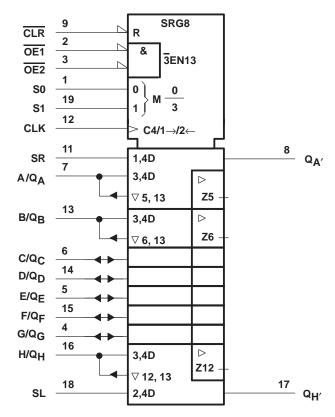
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FUNCTION TABLE

MODE				INP	UTS							I/O P	ORTS				OUTI	PUTS
MODE	CLR	S 1	S0	OE1†	OE2†	CLK	SL	SR	A/Q _A	B/QB	C/QC	D/QD	E/QE	F/Q _F	G/Q _G	H/Q _H	$Q_{\textbf{A}'}$	$Q_{H'}$
Clear	L L L	X L H	L X H	L L X	L L X	X X X	X X X	X X X	L L X	L L L	Г Г							
Hold	H H	L X	L X	L L	L L	X L	X X	X X	Q _{A0} Q _{A0}	Q _{B0} Q _{B0}	Q _{C0}	Q _{D0} Q _{D0}	Q _{E0} Q _{E0}	Q _{F0} Q _{F0}	Q _{G0} Q _{G0}	Q _{H0} Q _{H0}	Q _{A0} Q _{A0}	Q _{H0} Q _{H0}
Shift Right	H H	L L	H H	L L	L L	↑ ↑	X X	H L	H L	Q _{An} Q _{An}	Q _{Bn} Q _{Bn}	Q _{Cn} Q _{Cn}	Q _{Dn} Q _{Dn}	Q _{En} Q _{En}	Q _{Fn} Q _{Fn}	Q _{Gn} Q _{Gn}	H L	Q _{Gn} Q _{Gn}
Shift Left	H H	H H	L L	L L	L L	↑ ↑	H L	X X	Q _{Bn} Q _{Bn}	Q _{Cn} Q _{Cn}	Q _{Dn} Q _{Dn}	Q _{En} Q _{En}	Q _{Fn} Q _{Fn}	Q _{Gn} Q _{Gn}	Q _{Hn} Q _{Hn}	H L	Q _{Bn} Q _{Bn}	H L
Load	Н	Н	Н	Χ	Χ	1	Х	Х	а	b	С	d	е	f	g	h	а	h

NOTE: a . . . h = the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

logic symbol[‡]

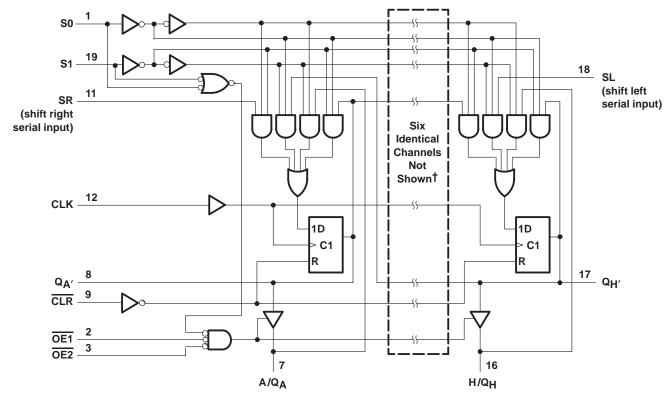


[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



[†] When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

logic diagram (positive logic)



 \dagger I/O ports not shown: B/QB (13), C/QC (6), D/QD (14), E/QE (5), F/QF (15), and G/QG (4).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{CC}		7 V
Input voltage, V _I : All inputs		7 V
I/O ports		5.5 V
Operating free-air temperature range, T _A : \$	SN54ALS299	. −55°C to 125°C
	SN74ALS299	0°C to 70°C
Storage temperature range		. −65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN54ALS299, SN74ALS299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

SDAS220B - DECEMBER 1982 - REVISED DECEMBER 1994

recommended operating conditions

				SN	SN54ALS299			SN74ALS299		
						MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
VIH High-level input voltage			2			2			V	
VIL	Low-level input voltage					0.7			0.8	V
la	High-level output current	QA' or QH'				-0.4			-0.4	mA
IOH	r light-level output current	$Q_A - Q_H$				-1			-2.6	IIIA
la.	Low lovel output current	Q _A ' or Q _H '				4			8	mA
IOL	Low-level output current	Q _A – Q _H				12			24	IIIA
TA	Operating free-air temperature			-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CO	MOITIONS	SN	54ALS2	99	SN74ALS299			UNIT
		1251 00	NDITIONS	MIN	TYP†	MAX	MIN	TYP [†]	MAX	UNII
VIK		V _{CC} = 4.5 V,	$I_{I} = -18 \text{ mA}$			-1.5			-1.5	V
	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2	2		V _{CC} -2	2		
Vон	Q _A – Q _H	V _{CC} = 4.5 V	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V
	QA - QH	VCC = 4.5 V	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
	Q _A , or Q _H ,	V _{CC} = 4.5 V	$I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	
\/o;	QA' OI QH'	VCC = 4.5 V	$I_{OL} = 8 \text{ mA}$					0.35	0.5	V
V _{OL} Q _A – Q _H	0. 0	V _{CC} = 4.5 V	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	v
	TQA - QH	VCC = 4.5 V	I _{OL} = 24 mA				0.35		0.5	
1.	A – H	V _{CC} = 5.5 V	V _I = 5.5 V			0.1			0.1	mA
Ħ	Any others	VCC = 5.5 V	V _I = 7 V		0.1				0.1	IIIA
l _{IH} ‡		V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
. +	S0, S1, SR, SL	V 55V	V- 0.4.V			-0.2			-0.2	A
I _{IL} ‡	Any others	$V_{CC} = 5.5 \text{ V},$	V _I = 0.4 V		-0.1				-0.1	mA
	Q _A ' or Q _H '	Vac 55V	Va 2.25 V	-15		-70	-15		-70	mA
IO§	Q _A – Q _H	V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	-20	-20 -112		-30		-112	mA
			Outputs high		15	28		15	28	mA
ICC		V _{CC} = 5.5 V	Outputs low		22	38		22	38	
			Outputs disabled		23	40		23	40	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

 $[\]ddagger$ For I/O ports (Q_A-Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

^{\$} The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

					LS299	SN74A	UNIT			
			MIN	MAX	MIN	MAX	UNII			
f _{clock} Clock frequency (at 50% duty cycle)						0	30	MHz		
·	Pulse duration	CLK high or low		22		16.5				
t _W	Fulse duration	CLR low		12		10		ns		
		S0 or S1	25		20					
 _	Setup time before CLK↑	Carial as seculal data	High	18		16				
t _{su}		Serial or parallel data	15		6		ns			
	Inactive-state setup time before CLK↑†	CLR	15		15]			
4.	Hold time after CLK↑	S0 or S1	0		0		ns			
^t h	HOIG LITTLE AILER CLK I	Serial or parallel data	0		0		113			

[†] Inactive-state setup time is also referred to as recovery time.

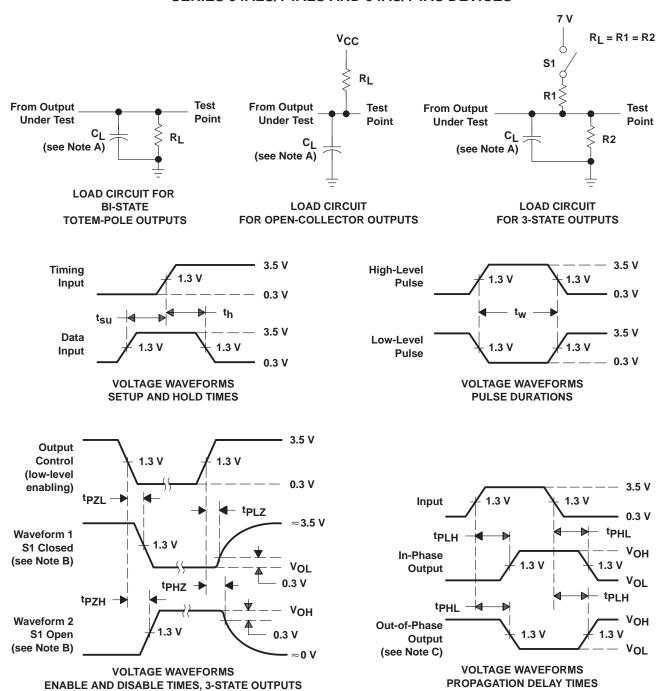
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω , R2 = 500 Ω , T_A = MIN to MAX [‡]				
			SN54A	LS299	SN74ALS299			
			MIN	MAX	MIN	MAX		
f _{max}			17		30		MHz	
^t PLH	CLK	0. 0	2	19	4	13	ns	
^t PHL	CLN	Q _A –Q _H	4	25	7	19	115	
^t PLH	CLK	00.0	2	21	5	15	ns	
^t PHL	CLN	Q _A ′ or Q _H ′	4	25	8	18		
t =	CLR	Q_A-Q_H	6	29	6	22	ns	
^t PHL	CLR	Q _A ′ or Q _H ′	6	29	6	22	115	
^t PZH	OE1, OE2	0 0	5	22	6	16	ns	
t _{PZL}	OE1, OE2	$Q_A - Q_H$	6	27	8	22		
^t PZH	00.04	0. 0.	5	27	7	17	no	
t _{PZL}	S0, S1	Q_A-Q_H	6	26	8	22	ns	
^t PHZ	OE1, OE2	0. 0	1	15	1	8	ns	
^t PLZ	UE1, UE2	Q_A-Q_H	4	38	5	15		
^t PHZ	S0, S1	Q _A -Q _H	1	16	1	12	ns	
^t PLZ	50, 51	VA−VH	4	34	8	25		

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR \leq 1 MHz, t_{Γ} = t_{f} = 2 ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
83021012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83021012A SNJ54ALS 299FK
8302101RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302101RA SNJ54ALS299J
8302101SA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302101SA SNJ54ALS299W
SN74ALS299DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS299
SN74ALS299DW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS299
SN74ALS299N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS299N
SN74ALS299N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS299N
SNJ54ALS299FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83021012A SNJ54ALS 299FK
SNJ54ALS299FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83021012A SNJ54ALS 299FK
SNJ54ALS299J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302101RA SNJ54ALS299J
SNJ54ALS299J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302101RA SNJ54ALS299J
SNJ54ALS299W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302101SA SNJ54ALS299W
SNJ54ALS299W.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302101SA SNJ54ALS299W

⁽¹⁾ **Status:** For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

PACKAGE OPTION ADDENDUM

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(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54ALS299, SN74ALS299:

Catalog: SN74ALS299

Military: SN54ALS299

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
83021012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8302101SA	W	CFP	20	25	506.98	26.16	6220	NA
SN74ALS299DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS299DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS299N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS299N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ALS299FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS299FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS299W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54ALS299W.A	W	CFP	20	25	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

 D. Index point is provided on cap for terminal identification only.

 E. Falls within Mil—Std 1835 GDFP2—F20



14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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