

# SNx4AHC373 Octal Transparent D-Type Latches With 3-State Outputs

## 1 Features

- Operating range of 2V to 5.5V  $V_{CC}$
- Latch-up performance exceeds 250mA per JESD 17
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## 2 Applications

- Enable or disable a digital signal
- Controlling an indicator LED
- Translation between communication modules and system controllers

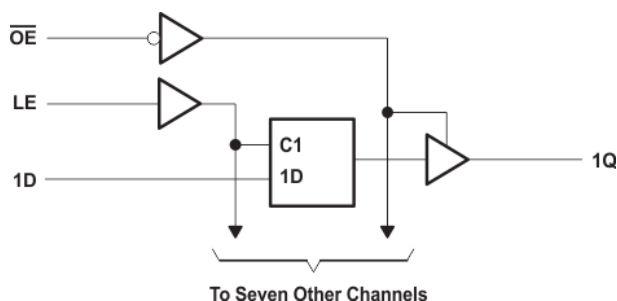
## 3 Description

The SNx4AHC373 devices are octal transparent D-type latches designed for 2V to 5.5V  $V_{CC}$  operation.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE <sup>(3)</sup>
SNx4AHC373	J (CDIP, 20)	24.2mm × 7.62mm	24.2mm × 6.92mm
	W (CFP, 20)	13.09mm × 8.13mm	13.09mm × 6.92mm
	FK (LCCC, 20)	8.89mm × 8.89mm	8.89 mm × 8.89 mm
	DB (SSOP, 20)	7.2mm × 7.8mm	7.50mm × 5.30mm
	DGV (TVSOP, 20)	5.00mm × 6.4mm	5.00mm × 4.40mm
	DW (SOIC, 20)	12.80mm × 10.3mm	12.8mm × 7.5mm
	NS (SOP, 20)	12.60mm × 7.8mm	12.6mm × 5.30mm
	N (PDIP, 20)	24.33mm × 9.4mm	25.40mm × 6.35mm
	PW (TSSOP, 20)	6.50mm × 6.4mm	6.50mm × 4.40mm

- For more information, see [Mechanical, Packaging, and Orderable Information](#).
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



To Seven Other Channels  
**Logic Diagram (Positive Logic)**

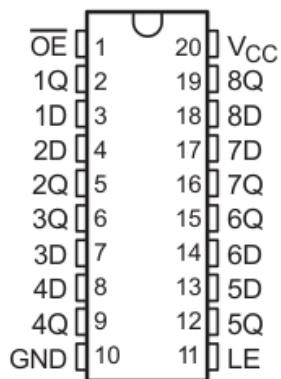


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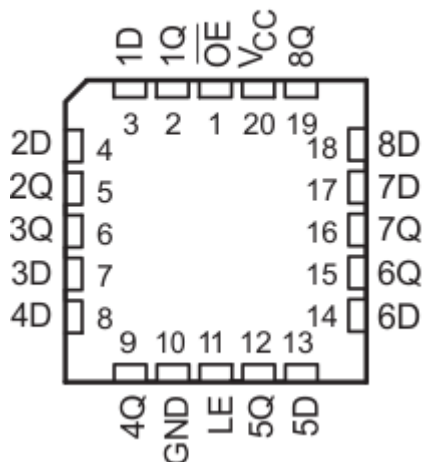
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## 4 Pin Configuration and Functions

**SN54AHC373 . . . J OR W PACKAGE**  
**SN74AHC373 . . . DB, DGV, DW, N, NS, OR PW PACKAGE**  
(TOP VIEW)



**SN54AHC373 . . . FK PACKAGE**  
(TOP VIEW)



**Table 4-1. Pin Functions**

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OE	I	Output Enable
2	1Q	O	1Q Output
3	1D	I	1D Input
4	2D	I	2D Input
5	2Q	O	2Q Output
6	3Q	O	3Q Output
7	3D	I	3D Input
8	4D	I	4D Input
9	4Q	O	4Q Output
10	GND	—	Ground
11	LE	I	Latch Enable
12	5Q	O	5Q Output
13	5D	I	5D Input
14	6D	I	6D Input
15	6Q	O	6Q Output
16	7Q	O	7Q Output
17	7D	I	7D Input
18	8D	I	8D Input
19	8Q	O	8Q Output
20	V <sub>CC</sub>	—	Power Pin

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	−0.5	7	V
$V_I$	Input voltage range <sup>(1)</sup>	−0.5	7	V
$V_O$	Output voltage range <sup>(1)</sup>	−0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	−20	mA
$I_{OK}$	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$	±20	mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$	±25	mA
	Continuous current through $V_{CC}$ or GND		±75	mA
$T_{stg}$	Storage temperature	−65	150	°C

(1) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

		Value	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			SN54AHC373		SN74AHC373		UNIT
			MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage		2	5.5	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5		1.5		V
		$V_{CC} = 3\text{ V}$	2.1		2.1		
		$V_{CC} = 5.5\text{ V}$	3.85		3.85		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$		0.5		0.5	V
		$V_{CC} = 3\text{ V}$		0.9		0.9	
		$V_{CC} = 5.5\text{ V}$		1.65		1.65	
$V_I$	Input voltage		0	5.5	0	5.5	V
$V_O$	Output voltage		0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2\text{ V}$		−50		−50	μA
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		−4		−4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		−8		−8	
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$		50		50	μA
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		4		4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		100		100	ns/V
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		20		20	
$T_A$	Operating free-air temperature		−55	125	−40	85	°C

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74AHC373						UNIT	
	DW	DB	DGV	N	NS	PW		
	20 PINS							
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	58	70	92	69	60	116.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHC373		SN74AHC373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V	1.9			1.9		1.9		V
		3 V	2.9			2.9		2.9		
		4.5 V	4.4			4.4		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.5		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.5		0.44	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1 <sup>(1)</sup>		±1	μA
I <sub>OZ</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±2.5		±2.5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40		40	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10				10	pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		6						pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

## 5.6 Timing Requirements, V<sub>CC</sub> = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER		T <sub>A</sub> = 25°C		SN54AHC373		SN74AHC373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	5		5		5		ns
t <sub>su</sub>	Setup time, data before LE↓	4		4		4		ns
t <sub>h</sub>	Hold time, data after LE↓	1		1		1		ns

## 5.7 Timing Requirements, V<sub>CC</sub> = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER		T <sub>A</sub> = 25°C		SN54AHC373		SN74AHC373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	5		5		5		ns
t <sub>su</sub>	Setup time, data before LE↓	4		4		4		ns
t <sub>h</sub>	Hold time, data after LE↓	1		1		1		ns

## 5.8 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$		SN54AHC373		SN74AHC373		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	Q	$C_L = 15\text{ pF}$	7.3 <sup>(1)</sup>	11.4 <sup>(1)</sup>	1 <sup>(1)</sup>	13.5 <sup>(1)</sup>	1	13.5	ns
$t_{PHL}$				7.3 <sup>(1)</sup>	11.4 <sup>(1)</sup>	1 <sup>(1)</sup>	13.5 <sup>(1)</sup>	1	13.5	
$t_{PLH}$	LE	Q	$C_L = 15\text{ pF}$	7 <sup>(1)</sup>	11 <sup>(1)</sup>	1 <sup>(1)</sup>	13 <sup>(1)</sup>	1	13	ns
$t_{PHL}$				7 <sup>(1)</sup>	11 <sup>(1)</sup>	1 <sup>(1)</sup>	13 <sup>(1)</sup>	1	13	
$t_{PZH}$	$\overline{OE}$	Q	$C_L = 15\text{ pF}$	7.3 <sup>(1)</sup>	11.4 <sup>(1)</sup>	1 <sup>(1)</sup>	13.5 <sup>(1)</sup>	1	13.5	ns
$t_{PZL}$				7.3 <sup>(1)</sup>	11.4 <sup>(1)</sup>	1 <sup>(1)</sup>	13.5 <sup>(1)</sup>	1	13.5	
$t_{PHZ}$	$\overline{OE}$	Q	$C_L = 15\text{ pF}$	7 <sup>(1)</sup>	10 <sup>(1)</sup>	1 <sup>(1)</sup>	12 <sup>(1)</sup>	1	12	ns
$t_{PLZ}$				7 <sup>(1)</sup>	10 <sup>(1)</sup>	1 <sup>(1)</sup>	12 <sup>(1)</sup>	1	12	
$t_{PLH}$	D	Q	$C_L = 50\text{ pF}$	9.8	14.9	1	17	1	17	ns
$t_{PHL}$				9.8	14.9	1	17	1	17	
$t_{PLH}$	LE	Q	$C_L = 50\text{ pF}$	9.5	14.5	1	16.5	1	16.5	ns
$t_{PHL}$				9.5	14.5	1	16.5	1	16.5	
$t_{PZH}$	$\overline{OE}$	Q	$C_L = 50\text{ pF}$	9.8	14.9	1	17	1	17	ns
$t_{PZL}$				9.8	14.9	1	17	1	17	
$t_{PHZ}$	$\overline{OE}$	Q	$C_L = 50\text{ pF}$	9.5	13.2	1	15	1	15	ns
$t_{PLZ}$				9.5	13.2	1	15	1	15	
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1.5 <sup>(2)</sup>				1.5	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 5.9 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$		SN54AHC373		SN74AHC373		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	Q	$C_L = 15\text{ pF}$	5 <sup>(1)</sup>	7.2 <sup>(1)</sup>	1 <sup>(1)</sup>	8.5 <sup>(1)</sup>	1	8.5	ns
$t_{PHL}$				5 <sup>(1)</sup>	7.2 <sup>(1)</sup>	1 <sup>(1)</sup>	8.5 <sup>(1)</sup>	1	8.5	
$t_{PLH}$	LE	Q	$C_L = 15\text{ pF}$	4.9 <sup>(1)</sup>	7.2 <sup>(1)</sup>	1 <sup>(1)</sup>	8.5 <sup>(1)</sup>	1	8.5	ns
$t_{PHL}$				4.9 <sup>(1)</sup>	7.2 <sup>(1)</sup>	1 <sup>(1)</sup>	8.5 <sup>(1)</sup>	1	8.5	
$t_{PZH}$	$\overline{OE}$	Q	$C_L = 15\text{ pF}$	5.5 <sup>(1)</sup>	8.1 <sup>(1)</sup>	1 <sup>(1)</sup>	9.5 <sup>(1)</sup>	1	9.5	ns
$t_{PZL}$				5.5 <sup>(1)</sup>	8.1 <sup>(1)</sup>	1 <sup>(1)</sup>	9.5 <sup>(1)</sup>	1	9.5	
$t_{PHZ}$	$\overline{OE}$	Q	$C_L = 15\text{ pF}$	5 <sup>(1)</sup>	7.2 <sup>(1)</sup>	1 <sup>(1)</sup>	8.5 <sup>(1)</sup>	1	8.5	ns
$t_{PLZ}$				5 <sup>(1)</sup>	7.2 <sup>(1)</sup>	1 <sup>(1)</sup>	8.5 <sup>(1)</sup>	1	8.5	
$t_{PLH}$	D	Q	$C_L = 50\text{ pF}$	6.5	9.2	1	10.5	1	10.5	ns
$t_{PHL}$				6.5	9.2	1	10.5	1	10.5	
$t_{PLH}$	LE	Q	$C_L = 50\text{ pF}$	6.4	9.2	1	10.5	1	10.5	ns
$t_{PHL}$				6.4	9.2	1	10.5	1	10.5	
$t_{PZH}$	$\overline{OE}$	Q	$C_L = 50\text{ pF}$	7	10.1	1	11.5	1	11.5	ns
$t_{PZL}$				7	10.1	1	11.5	1	11.5	
$t_{PHZ}$	$\overline{OE}$	Q	$C_L = 50\text{ pF}$	6.5	9.2	1	10.5	1	10.5	ns
$t_{PLZ}$				6.5	9.2	1	10.5	1	10.5	
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1 <sup>(2)</sup>				1	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 5.10 Noise Characteristics

$V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ <sup>(1)</sup>

PARAMETER		SN74AHC373		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$	4.1		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

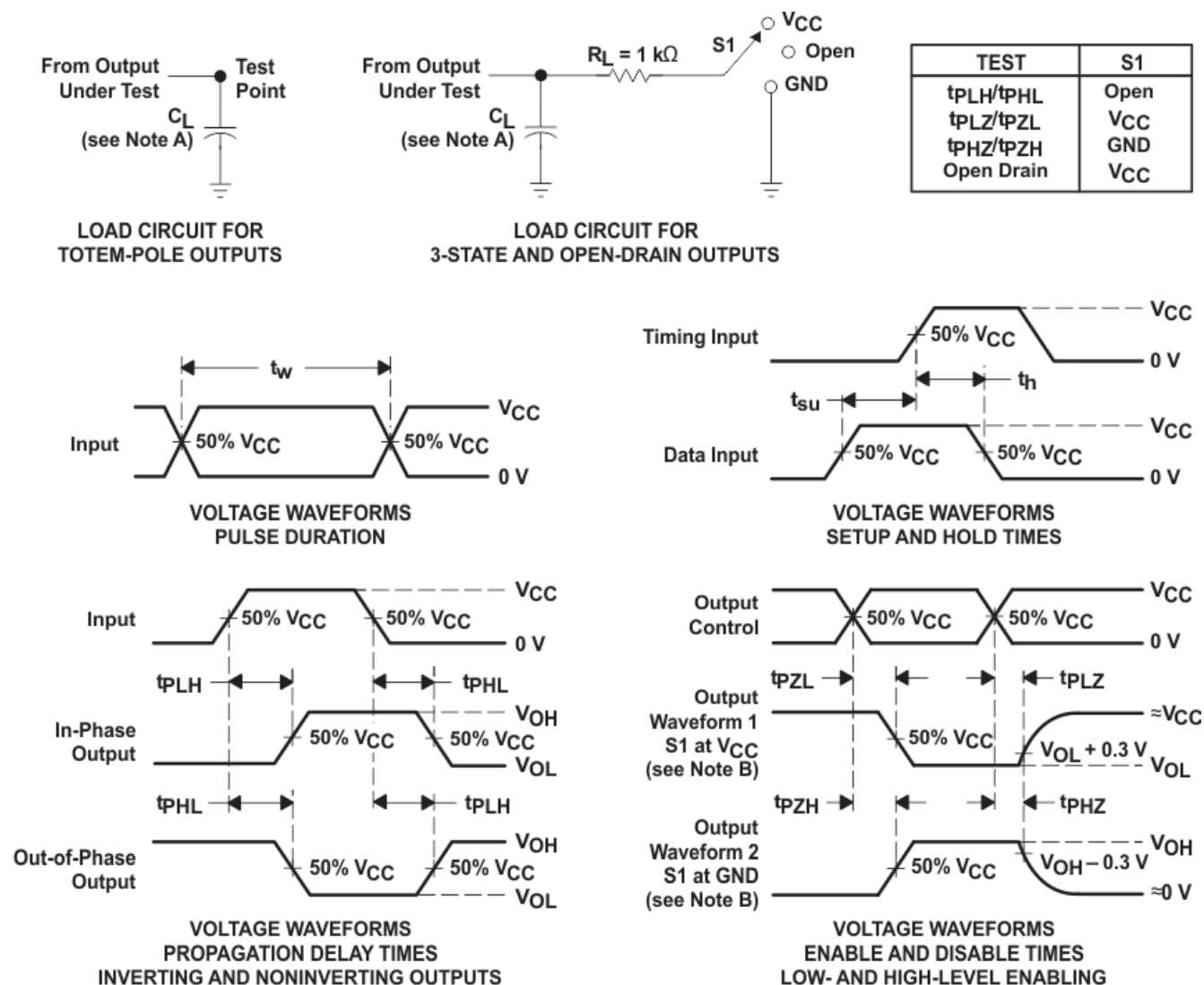
(1) Characteristics are for surface-mount packages only.

## 5.11 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load,	$f = 1\text{ MHz}$	18	pF

## 6 Parameter Measurement Information



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms



## 7 Detailed Description

### 7.1 Overview

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

For the specified high-impedance state during power up or power down,  $\overline{OE}$  must be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 7.2 Functional Block Diagram

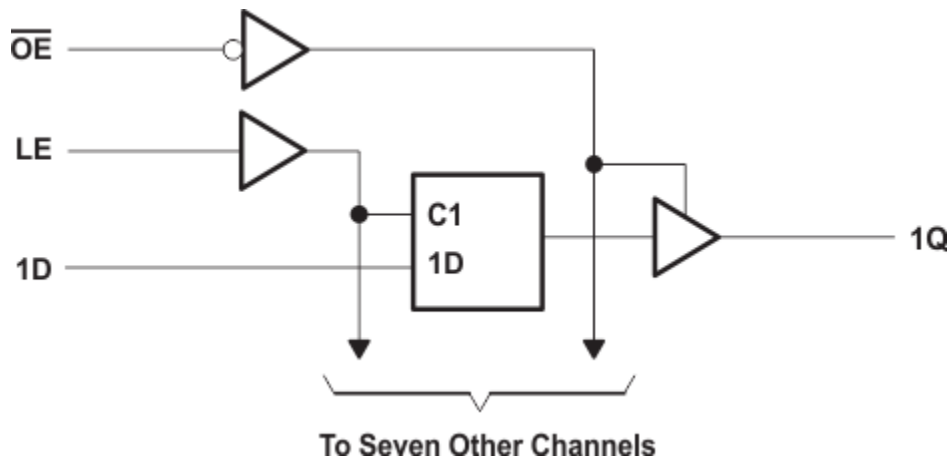


Figure 7-1. Logic Diagram (Positive Logic)

### 7.3 Device Functional Modes

Table 7-1. Function Table  
(Each Latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

## 8 Application and Implementation

### 8.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

### 8.2 Layout

#### 8.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

##### 8.2.1.1 Layout Example

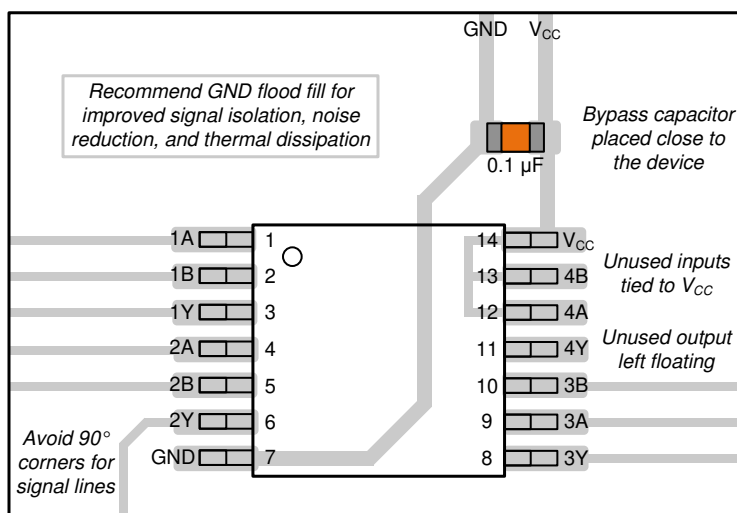


Figure 8-1. Example Layout for the SN74AHC373

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 9-1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC373	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74AHC373	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 9.4 Trademarks

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All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision J (August 2023) to Revision K (July 2024) Page

- Updated RθJA values: PW = 83 to 116.8, all values in °C/W .....5

### Changes from Revision I (July 2003) to Revision J (August 2023) Page

- Added *Applications*, *Package Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes*, *Application and Implementation* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.....1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-9686601Q2A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9686601Q2A SNJ54AHC 373FK
<a href="#">5962-9686601QRA</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686601QR A SNJ54AHC373J
<a href="#">5962-9686601QSA</a>	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686601QS A SNJ54AHC373W
<a href="#">SN74AHC373DBR</a>	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA373
SN74AHC373DBR.A	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA373
<a href="#">SN74AHC373DGSR</a>	Active	Production	VSSOP (DGS)   20	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC373
<a href="#">SN74AHC373DGVR</a>	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA373
SN74AHC373DGVR.A	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA373
<a href="#">SN74AHC373DW</a>	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	-40 to 85	AHC373
<a href="#">SN74AHC373DWR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC373
SN74AHC373DWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC373
<a href="#">SN74AHC373N</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHC373N
SN74AHC373N.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHC373N
<a href="#">SN74AHC373NSR</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC373
SN74AHC373NSR.A	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC373
<a href="#">SN74AHC373PW</a>	Obsolete	Production	TSSOP (PW)   20	-	-	Call TI	Call TI	-40 to 85	HA373
<a href="#">SN74AHC373PWR</a>	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA373
SN74AHC373PWR.A	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA373
<a href="#">SN74AHC373RKSR</a>	Active	Production	VQFN (RKS)   20	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC373
<a href="#">SNJ54AHC373FK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9686601Q2A SNJ54AHC 373FK

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54AHC373FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9686601Q2A SNJ54AHC 373FK
<a href="#">SNJ54AHC373J</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686601QR A SNJ54AHC373J
SNJ54AHC373J.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686601QR A SNJ54AHC373J
<a href="#">SNJ54AHC373W</a>	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686601QS A SNJ54AHC373W
SNJ54AHC373W.A	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686601QS A SNJ54AHC373W

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54AHC373, SN74AHC373 :**

- Catalog : [SN74AHC373](#)
- Automotive : [SN74AHC373-Q1](#), [SN74AHC373-Q1](#)
- Military : [SN54AHC373](#)

**NOTE:** Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC373DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHC373DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74AHC373DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC373DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHC373NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHC373PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHC373RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC373DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74AHC373DGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74AHC373DGV	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74AHC373DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHC373NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74AHC373PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHC373RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

## TUBE

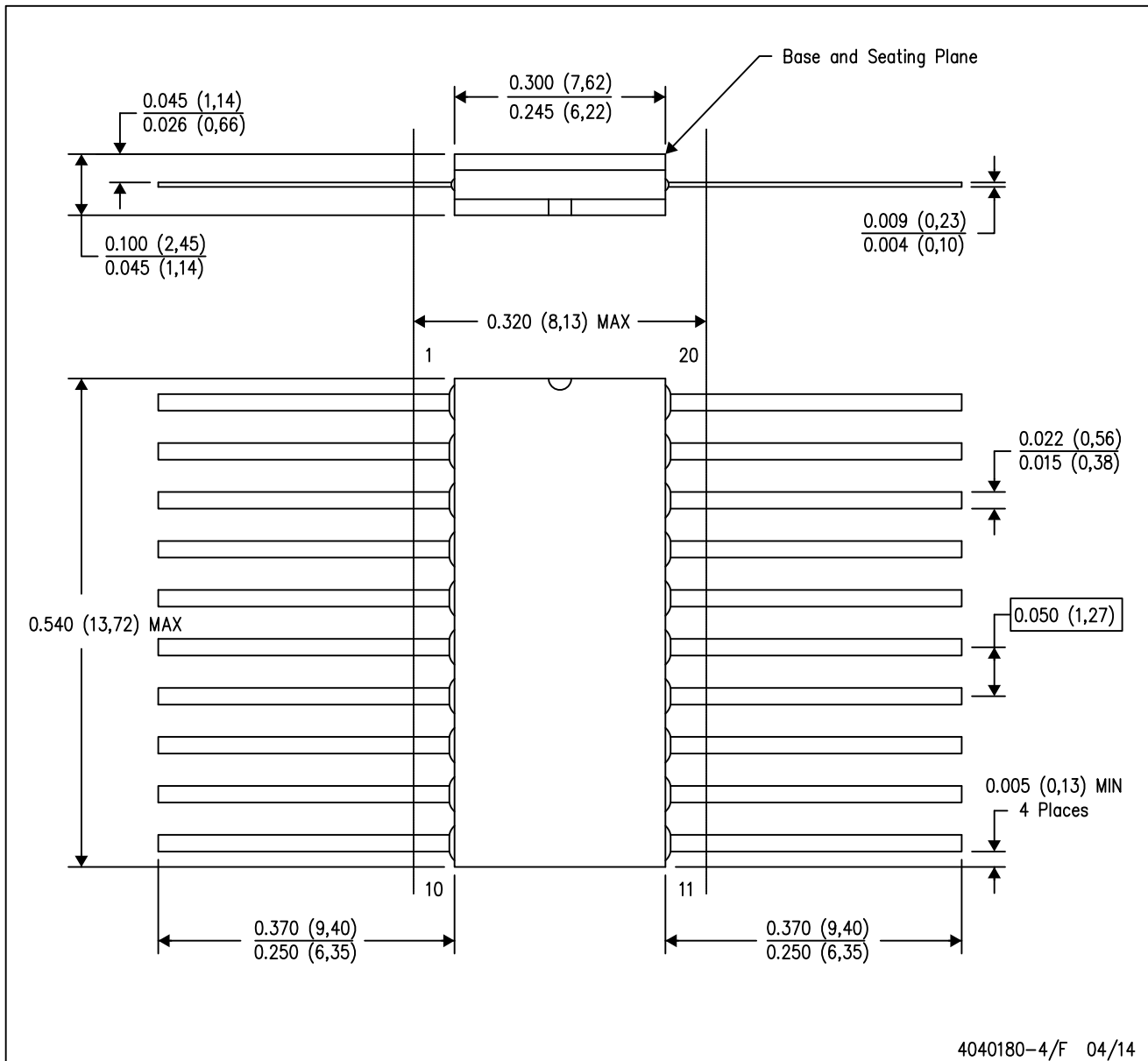


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9686601Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9686601QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHC373N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AHC373N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHC373FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC373FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC373W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54AHC373W.A	W	CFP	20	25	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20



4220206/A 02/2017

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4226367/A 10/2020

## NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



# EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



4214851/B 08/2019

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**RKS 20**

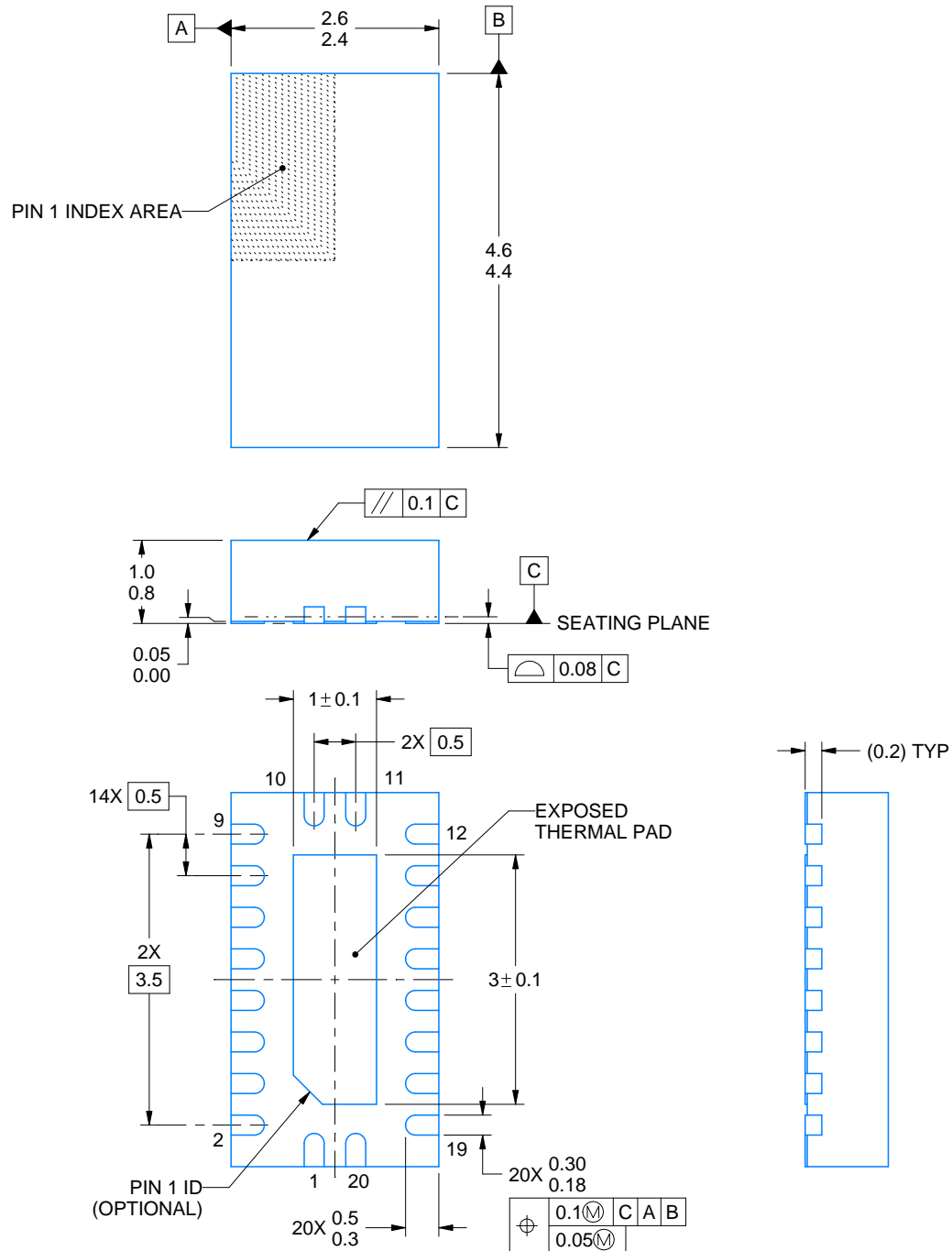
**VQFN - 1 mm max height**

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.





4222490/B 02/2021

## NOTES:

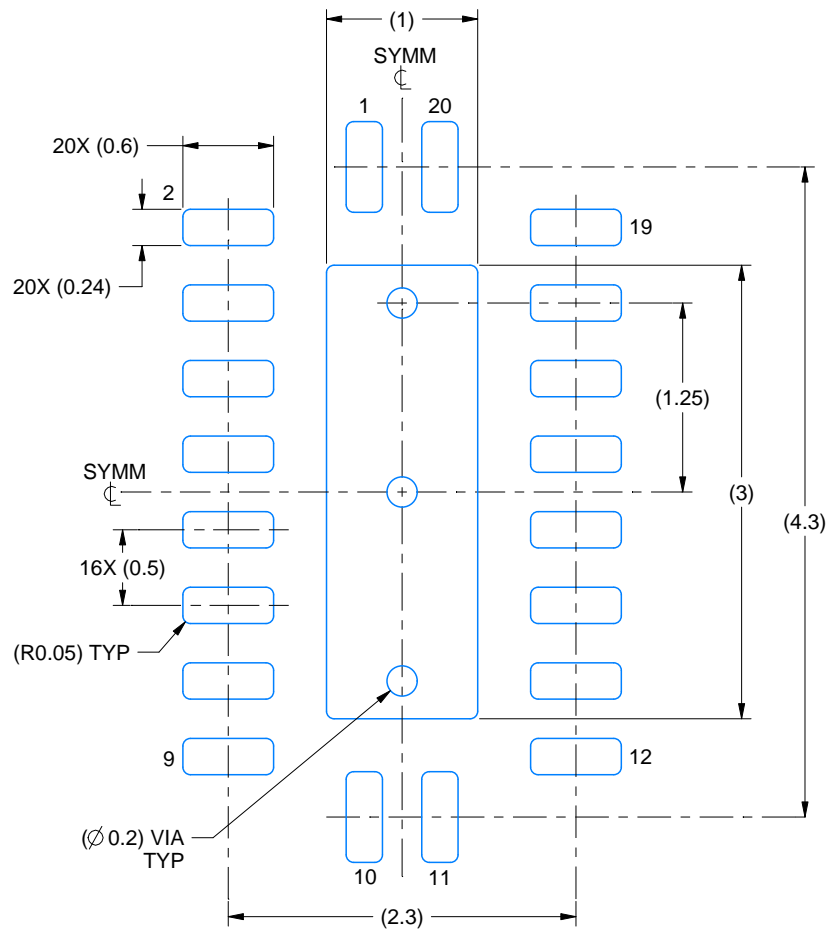
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

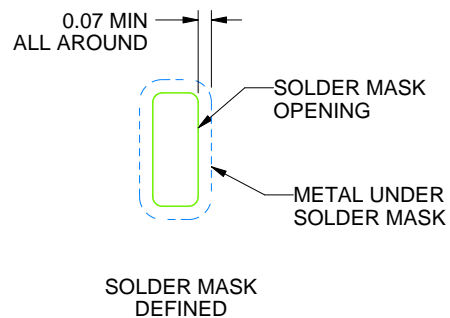
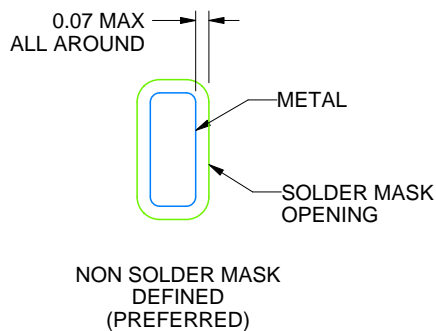
RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

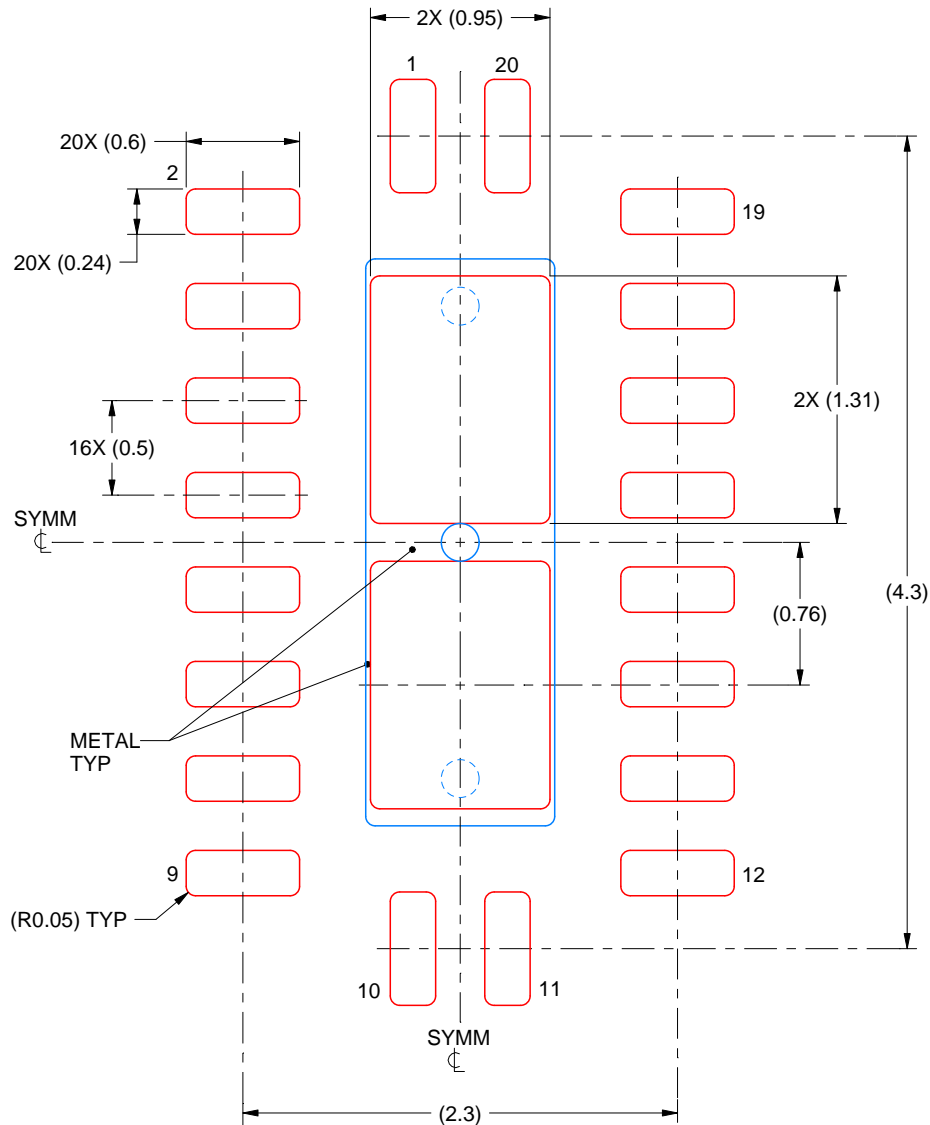
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
83% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

4222490/B 02/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE

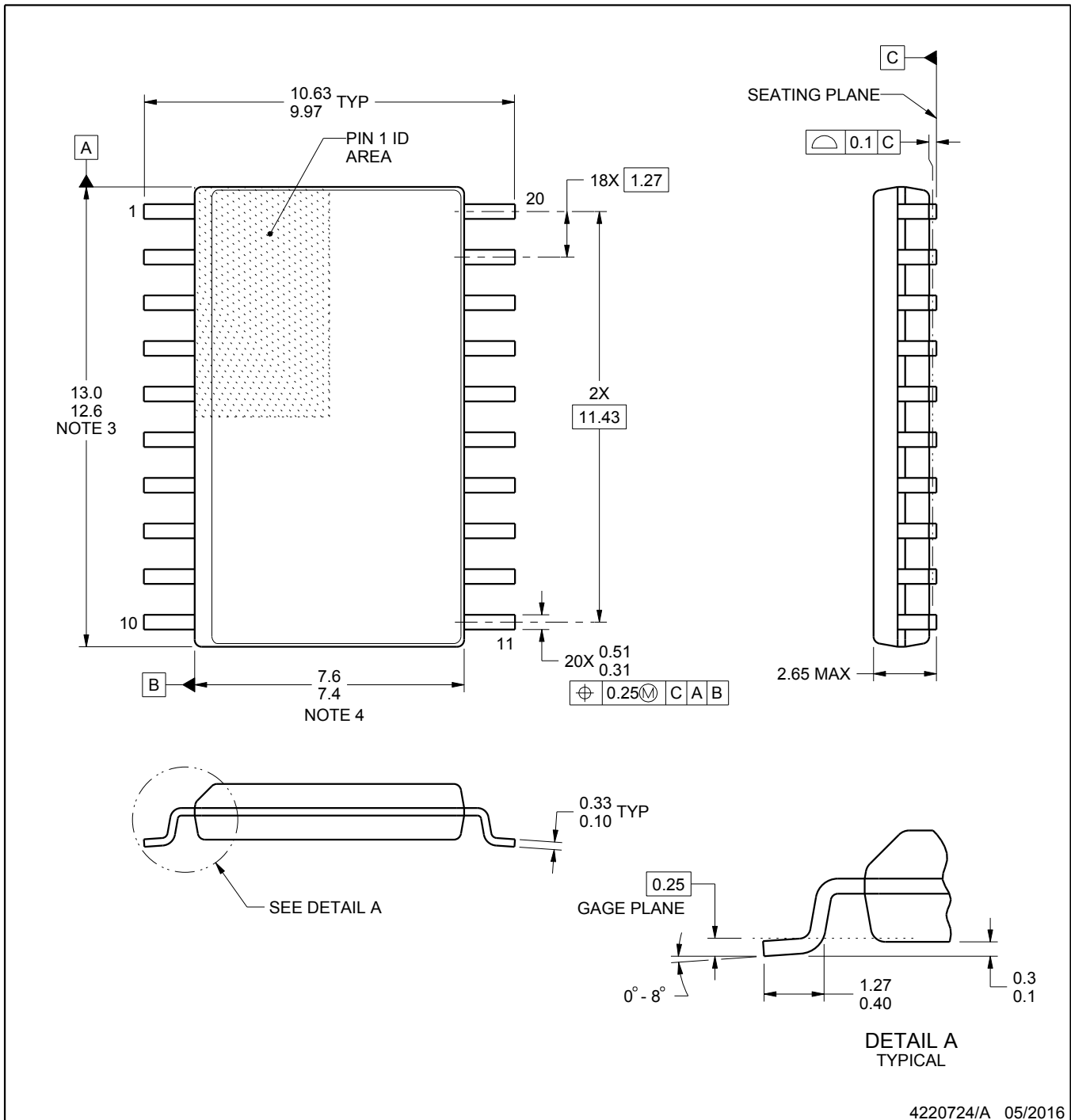


PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

## NOTES:

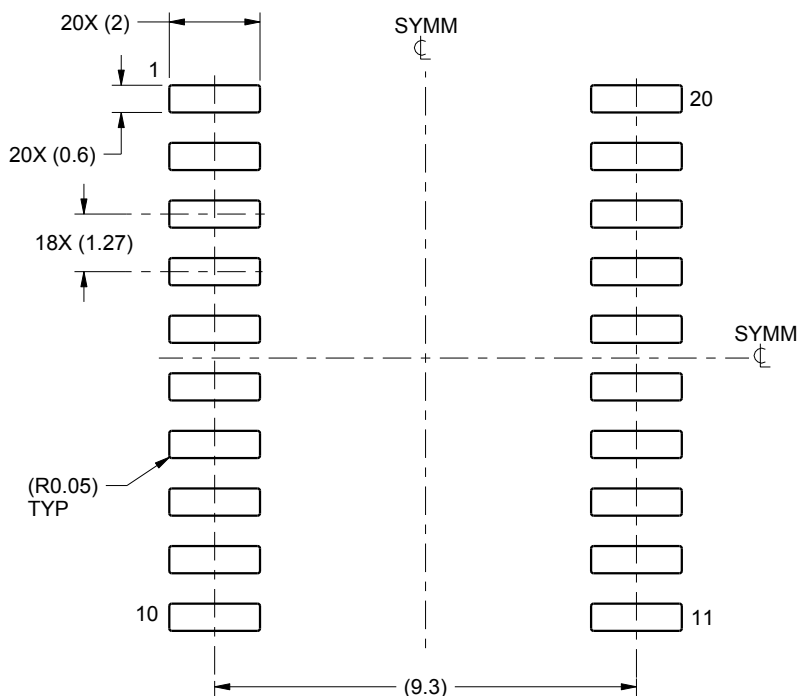
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

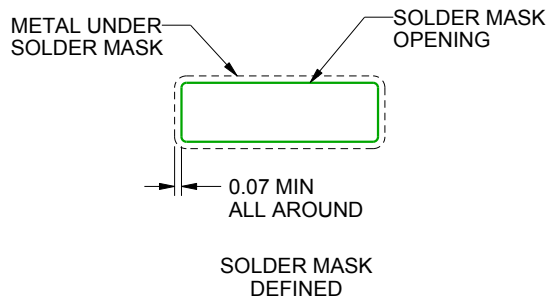
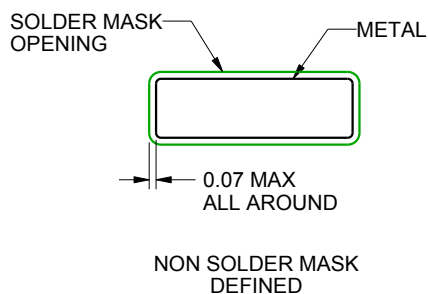
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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