









SN54AHC245, SN74AHC245

SCLS230N - OCTOBER 1995 - REVISED JUNE 2024

SNx4AHC245 Octal Bus Transceivers With 3-State Outputs

1 Features

- Operating range 2V to 5.5V V_{CC}
- Latch-up performance exceeds 250mA per JESD 17
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- Servers
- PCs and notebooks
- **Network switches**
- Wearable health and fitness devices
- Telecom infrastructures
- Electronic points of sale

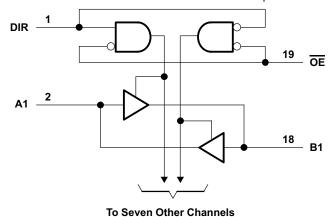
3 Description

The SNx4AHC245 octal bus transceivers are designed for asynchronous two-way communication between data buses. This part operates from 4.5V to 5.5V.

Device Information

	D 01100 .	momation	
PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)	BODY SIZE(3)
	J (CDIP, 20)	24.20mm × 7.62mm	24.20mm × 6.92mm
SN54AHC245	W (CFP, 20)	13.09mm × 8.13mm	13.09mm × 6.92mm
	FK (LCCC, 20)	8.89mm × 8.89mm	8.89mm × 8.89mm
	DB (SSOP, 20)	7.20mm × 7.8mm	7.20mm × 5.30mm
	DGV (TVSOP, 20)	5.00mm × 6.4mm	5.00mm × 4.40mm
	DW (SOIC, 20)	12.80mm × 10.3mm	12.80mm × 7.50mm
SN74AHC245	N (PDIP, 20)	24.33mm × 9.4mm	24.33mm × 6.35mm
	PW (TSSOP, 20)	6.50mm × 6.4mm	6.50mm × 4.40mm
	DGS (VSSOP, 20)	5.10mm × 4.9mm	5.10mm × 3.00mm
	RKS (VQFN, 20)	4.50mm × 2.50mm	4.50mm × 2.50mm

- For more information, see Mechanical, Packaging, and Orderable Information.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



Simplified Schematic

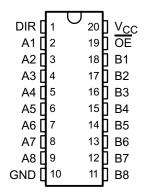


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4 Pin Configuration and Functions



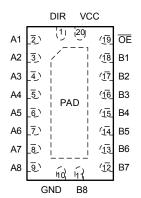


Figure 4-1. SN54AHC245 J or W, SN74AHC245 DB, DGV, DW, N, PW or DGS Package, CDIP, CFP, SSOP, TVSOP, SOIC, PDIP, TSSOP, or VSSOP 20-Pin (Top View)

Figure 4-2. SN74AHC245 RKS Package, VQFN 20-Pin (Top View)

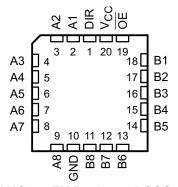


Figure 4-3. SN54AHC245 FK Package, LCCC 20-Pin (Top View)

Table 4-1. Pin Functions

	PIN	TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.	I TPE\''	DESCRIPTION
DIR	1	I/O	Direction Pin
A1	2	I/O	A1 Input/Output
A2	3	I/O	Y4 Input/Output
A3	4	I/O	A2 Input/Output
A4	5	I/O	Y3 Input/Output
A5	6	I/O	A3 Input/Output
A6	7	I/O	Y2 Input/Output
A7	8	I/O	A4 Input/Output
A8	9	I/O	Y1 Input/Output
GND	10	_	Ground Pin
B8	11	I/O	A1 Input/Output
B7	12	I/O	Y4 Input/Output
B6	13	I/O	A2 Input/Output
B5	14	I/O	Y3 Input/Output
B4	15	I/O	A3 Input/Output
B3	16	I/O	Y2 Input/Output
B2	17	I/O	A4 Input/Output



Table 4-1. Pin Functions (continued)

P	PIN		DESCRIPTION
NAME	NO.	TYPE ⁽¹⁾	DESCRIPTION
B1	18	I/O	Y1 Input/Output
ŌĒ	19	I/O	Output Enable
V _{CC}	20	_	Power Pin
Thermal pad		_	Thermal Pad ⁽²⁾

- (1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power
 (2) RKS package only.



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

					MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V			
VI	Input voltage range ⁽¹⁾		Control inputs	-0.5	7	V	
Vo	I/O, Output voltage range				-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		Control inputs		-20	mA
I _{OK}	I/O, Output clamp current	V _O < 0 or \	Vo > Vcc			±20	mA
Io	Continuous output current	V _O = 0 to \	/ _{cc}			±25	mA
	Continuous current through V_{CC} or GND	·				±75	mA

⁽¹⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Handling Ratings

			MIN	MAX	UNIT	
T _{stg}	Storage temperature rang	orage temperature range				
V	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	1500	V	
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	2000	V	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN54AH	C245	SN74AH	C245	UNIT	
			MIN	MAX	MIN	MAX	UNII	
V _{CC}	Supply voltage		2	5.5	2	5.5	V	
		V _{CC} = 2 V	1.5		1.5			
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1		2.1		V	
		V _{CC} = 5.5 V	3.85		3.85			
		V _{CC} = 2 V		0.5		0.5		
V _{IL}	Low-level input voltage	V _{CC} = 3 V		0.9		0.9	V	
		V _{CC} = 5.5 V		1.65		1.65		
VI	Input voltage	OE or DIR	0	5.5	0	5.5	V	
Vo	Output voltage	A or B	0	V _{CC}	0	V _{CC}	V	
		V _{CC} = 2 V		-50		-50	μA	
I _{OH}	High-level output current	V _{CC} = 3.3 V ± 0.3 V		-4		-4	m Λ	
		$V_{CC} = 5 V \pm 0.5 V$		-8		-8	mA	
		V _{CC} = 2 V		50		50	μA	
I _{OL}	Low-level output current	V _{CC} = 3.3 V ± 0.3 V		4		4	mA	
		V _{CC} = 5 V ± 0.5 V		8		8	mA	
A4/Ax	Input transition rise or fall rat-	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		100		100	20/1	
Δt/Δv	input transition rise or fall rate	Input transition rise or fall rate $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		20		20	ns/V	
T _A	Operating free-air temperature		-55	125	-40	125	°C	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, *Implications* of Slow or Floating CMOS Inputs (SCBA004).



5.4 Thermal Information

	THERMAL METRIC ⁽¹⁾	DB	DGV	DW	N	NS	PW	RGY	RKS	DGS	
	THERMAL METRIC	20 PINS									UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113.1	116.1	96.2	51.5	77.1	122.3	35.1	67.7	118.4	
R _{θJC(top)}	Junction-to-case (top) thermal resistance	72.9	31.3	63.6	38.2	43.6	64.8	43.3	72.4	57.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	67.9	57.6	64.7	32.4	44.6	73.3	12.9	40.4	73.1	
ΨЈТ	Junction-to-top characterization parameter	39.3	1.0	40.5	24.6	17.2	19	0.9	10.3	5.7	
ΨЈВ	Junction-to-board characterization parameter	67.5	56.9	64.3	32.3	44.2	73	12.9	40.4	72.7	
R ₀ JC(bot)	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	n/a	7.9	24.1	n/a	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report (SPRA953).

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS			_A = 25°C		SN54AH	C245	SN74AHC245		UNIT
PA	RAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
			2 V	1.9	2		1.9		1.9		
		I _{OH} = -50 μA	3 V	2.9	3		2.9		2.9		
V _{OH}			4.5 V	4.4	4.5		4.4		4.4		V
		I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
		I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
			2 V			0.1		0.1		0.1	
		I _{OL} = 50 μA	3 V			0.1		0.1		0.1	
V _{OL}			4.5 V			0.1		0.1		0.1	V
		I _{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I _{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
	A or B inputs	V ₁ = V _{CC} or GND	5.5 V			±0.1		±1		±1	
l ₁	OE or DIR	A I - ACC OL GIAD	0 V to 5.5 V			±0.1		±1 ⁽¹⁾		±1	μA
I _{OZ} (2)		$V_O = V_{CC}$ or GND, $V_I (\overline{OE}) = V_{IL}$ or V_{IH}	5.5 V			±0.25		±2.5		±2.5	μА
I _{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40		40	μA
C _i	OE or DIR	V _I = V _{CC} or GND	5 V		2.5	10				10	pF
C _{io}	A or B inputs	V _I = V _{CC} or GND	5 V		4						pF

On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V. The parameter I_{OZ} includes the input leakage current.

5.6 Switching Characteristics, V_{CC} = 3.3 V \pm 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM	то	LOAD	Т	A = 25°C	;	SN54Al	HC245	SN74AH	C245	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONII
t _{PLH}	A or B	B or A	C ₁ = 15 pF		5.8 ⁽¹⁾	8.4 ⁽¹⁾	1 ⁽¹⁾	10 ⁽¹⁾	1	10	ns
t _{PHL}	AUID	BULK	CL = 15 pr		5.8 ⁽¹⁾	8.4 ⁽¹⁾	1 ⁽¹⁾	10 ⁽¹⁾	1	10	
t _{PZH}	ŌĒ	A or B	C _L = 15 pF		8.5 ⁽¹⁾	13.2 ⁽¹⁾	1 ⁽¹⁾	15.5 ⁽¹⁾	1	15.5	ns
t _{PZL}	OL	AUD				8.5 ⁽¹⁾	13.2 ⁽¹⁾	1 ⁽¹⁾	15.5 ⁽¹⁾	1	15.5
t _{PHZ}	ŌĒ	A or B	C _L = 15 pF		8.9 ⁽¹⁾	12.5 ⁽¹⁾	1 ⁽¹⁾	15.5 ⁽¹⁾	1	15.5	
t _{PLZ}	OL	AUD	CL = 13 pr		8.9 ⁽¹⁾	12.5 ⁽¹⁾	1 ⁽¹⁾	15.5 ⁽¹⁾	1	15.5	ns

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5.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V (continued)

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM	то	LOAD	Т	_A = 25°C	= 25°C SN54AHC245			SN74AH	C245	UNIT			
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX				
t _{PLH}	A or B	B or A	C = 50 pF		8.3	11.9	1	13.5	1	13.5	ns			
t _{PHL}	AUID	BUIA	$C_L = 50 \text{ pF}$	C[= 30 pr	OL = 30 pi	CL = 30 pi		8.3	11.9	1	13.5	1	13.5	
t _{PZH}	ŌĒ	A or B	C _L = 50 pF		11	16.7	1	19	1	19	ns			
t _{PZL}	OL	AOID	C _L = 50 pr		11	16.7	1	19	1	19				
t _{PHZ}	ŌĒ	A or B	C _L = 50 pF		11.5	15.8	1	18	1	18				
t _{PLZ}	OL	AOID	CL = 30 pr		11.5	15.8	1	18	1	18	ns			
t _{sk(o)}			C _L = 50 pF			1.5 ⁽²⁾				1.5	ns			

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
- (2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.7 Switching Characteristics, $V_{CC} = 5 V \pm 0.5 V$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM	то	LOAD	T _A =	= 25°C		SN54AH	IC245	SN74AH	C245	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONI	
t _{PLH}	A or B	B or A	C _L = 15 pF		4 ⁽¹⁾	5.5 ⁽¹⁾	1 ⁽¹⁾	6.5 ⁽¹⁾	1	6.5	ns	
t _{PHL}	AOID	BULK	CL = 13 pr		4 ⁽¹⁾	5.5 ⁽¹⁾	1 ⁽¹⁾	6.5 ⁽¹⁾	1	6.5	115	
t _{PZH}	ŌĒ	A or B	C _L = 15 pF		5.8 ⁽¹⁾	8.5 ⁽¹⁾	1 ⁽¹⁾	10 ⁽¹⁾	1	10	ns	
t _{PZL}	OL	AOID	CL = 13 pr	į	5.8 ⁽¹⁾	8.5 ⁽¹⁾	1 ⁽¹⁾	10 ⁽¹⁾	1	10	115	
t _{PHZ}	ŌĒ	A or D	C ₁ = 15 pF	į	5.6 ⁽¹⁾	7.8 ⁽¹⁾	1 ⁽¹⁾	9.2 ⁽¹⁾	1	9.2	ns	
t _{PLZ}	OE	A or B	CL = 13 pr	į	5.6 ⁽¹⁾	7.8 ⁽¹⁾	1 ⁽¹⁾	9.2 ⁽¹⁾	1	9.2	115	
t _{PLH}	A or B	B or A	C _L = 50 pF		5.5	7.5	1	8.5	1	8.5	ns	
t _{PHL}	AOID	BULK	CL = 30 pr		5.5	7.5	1	8.5	1	8.5	115	
t _{PZH}	ŌĒ	A or B	C _L = 50 pF		7.3	10.6	1	12	1	12	ns	
t _{PZL}	OE	AUID	CL = 50 pr		7.3	10.6	1	12	1	12	115	
t _{PHZ}	ŌĒ	A or B	C _L = 50 pF		7	9.7	1	11	1	11	ns	
t _{PLZ}	OE	AUID	GL = 30 pr		7	9.7	1	11	1	11	115	
t _{sk(o)}			C _L = 50 pF			1(2)				1	ns	

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
- (2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.8 Noise Characteristics

 $V_{CC} = 5 \text{ V}, C_L = 50 \text{ pF}, T_A = 25^{\circ}\text{C}$ (1)

	PARAMETER	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.9		V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.9		V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		4.3		V
V _{IH(D)}	High-level dynamic input voltage	3.5			V
V _{IL(D)}	Low-level dynamic input voltage			1.5	V

(1) Characteristics are for surface-mount packages only.

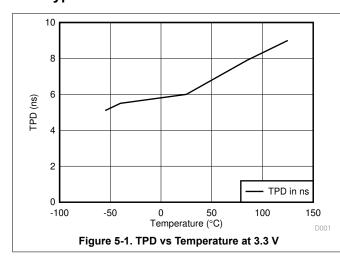


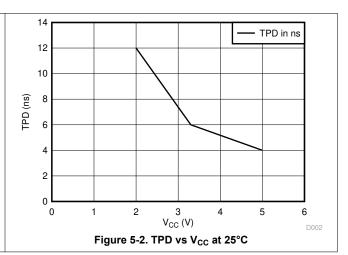
5.9 Operating Characteristics

 V_{CC} = 5 V, T_A = 25°C

	PARAMETER		NDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load	f = 1 MHz	14	pF

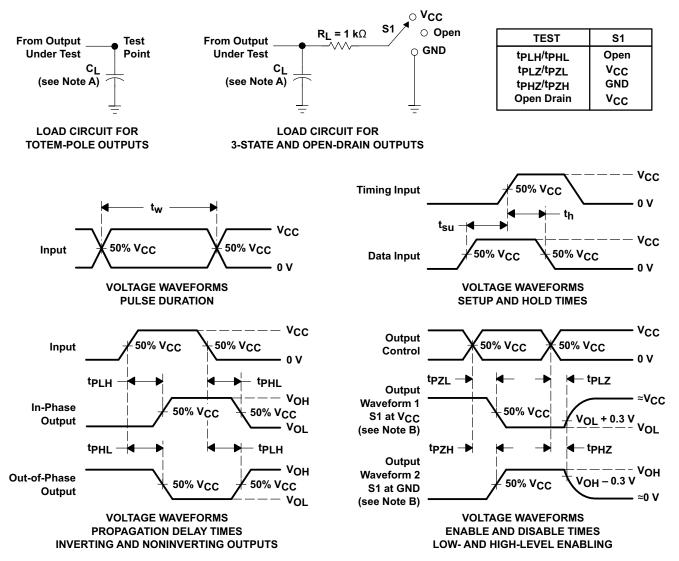
5.10 Typical Characteristics







6 Parameter Measurement Information



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

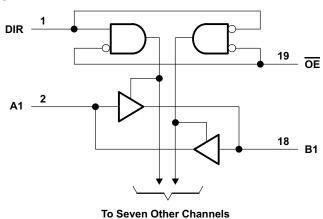
Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements. The SNx4AHC245 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated. For the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram



7.3 Feature Description

- V_{CC} is optimized at 5 V
- Allows down voltage translation from 5 V to 3.3 V
 - Inputs accept voltage levels up to 5.5 V
- Slow edge rates minimize output ringing

7.4 Device Functional Modes

Table 7-1. Function Table (Each Transceiver)

INP	UTS	OPERATION				
ŌĒ	DIR	OPERATION				
L	L	B data to A bus				
L	Н	A data to B bus				
Н	Χ	Isolation				



8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SNx4AHC245A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid V_{CC} making it ideal for down translation.

8.2 Typical Application

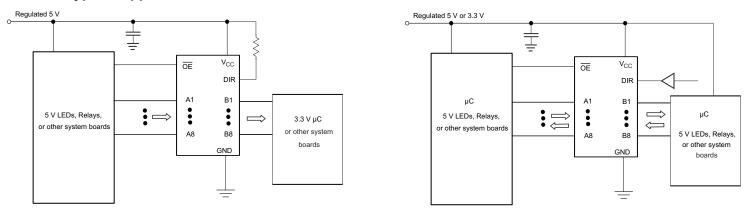


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions
 - Rise time and fall time specs: See ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
 - Specified high and low levels: See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
- 2. Recommend Output Conditions
 - Load currents should not exceed 25 mA per output and 75 mA total for the part.
 - Outputs should not be pulled above V_{CC}.

8.2.3 Application Curves

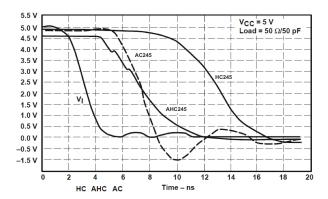


Figure 8-2. Switching Characteristics Comparison

8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended; if there are multiple V_{CC} pins, then 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and a 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 8-3 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.



8.4.2 Layout Example

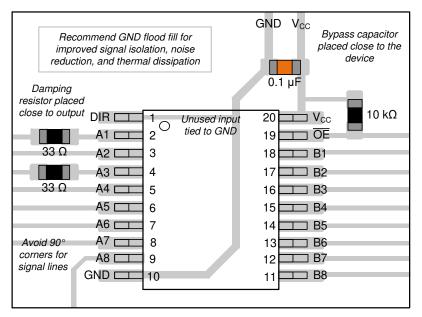


Figure 8-3. Example Layout of the SN74AHC245



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9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

changes nom revision in (same 2020) to revision it (same 2024)	. ugo
Added package size to Device Information table	
Updated names in <i>Pin Functions</i> table	3
Updated Layout Example	
Changes from Revision L (April 2023) to Revision M (June 2023)	Page
 Updated RθJA values: DB = 96.0 to 113.1, DW = 79.8 to 96.2, PW = 102.8 to PW packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in the second second	

11 Mechanical, Packaging, and Orderable Information

Changes from Revision M (June 2023) to Revision N (June 2024)

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN54AHC245 SN74AHC245

www.ti.com

8-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9681801Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9681801Q2A SNJ54AHC 245FK
5962-9681801QRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681801QR A SNJ54AHC245J
5962-9681801QSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681801QS A SNJ54AHC245W
5962-9681801VSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681801VS A SNV54AHC245W
5962-9681801VSA.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681801VS A SNV54AHC245W
SN74AHC245DBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245
SN74AHC245DBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245
SN74AHC245DGVR	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245
SN74AHC245DGVR.A	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245
SN74AHC245DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 125	AHC245
SN74AHC245DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC245
SN74AHC245DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC245
SN74AHC245DWRE4	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC245
SN74AHC245N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC245N
SN74AHC245N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC245N
SN74AHC245NSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC245
SN74AHC245NSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC245
SN74AHC245PW	Obsolete	Production	TSSOP (PW) 20	-		Call TI	Call TI	-40 to 125	HA245
SN74AHC245PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245
SN74AHC245PWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245
SN74AHC245PWRE4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245



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SNJ54AHC245W



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Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	(3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74AHC245PWRG4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245
SN74AHC245PWRG4.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245
SN74AHC245RKSR	Active	Production	VQFN (RKS) 20	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AHC245
SN74AHC245RKSR.A	Active	Production	VQFN (RKS) 20	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AHC245
SNJ54AHC245FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9681801Q2A SNJ54AHC 245FK
SNJ54AHC245FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9681801Q2A SNJ54AHC 245FK
SNJ54AHC245J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681801QF A SNJ54AHC245J
SNJ54AHC245J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681801QF A SNJ54AHC245J
SNJ54AHC245W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681801Q9 A SNJ54AHC245V
SNJ54AHC245W.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681801Q

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OPTION ADDENDUM

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(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54AHC245, SN54AHC245-SP, SN74AHC245:

Catalog: SN74AHC245, SN54AHC245

Automotive: SN74AHC245-Q1, SN74AHC245-Q1

Enhanced Product: SN74AHC245-EP, SN74AHC245-EP

Military: SN54AHC245

Space : SN54AHC245-SP

NOTE: Qualified Version Definitions:

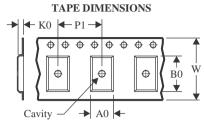
- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application



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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC245DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHC245DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC245DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AHC245NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHC245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHC245PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHC245PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHC245RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC245DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74AHC245DGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74AHC245DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHC245NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74AHC245PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHC245PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHC245PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHC245RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9681801Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9681801QSA	W	CFP	20	25	506.98	26.16	6220	NA
5962-9681801VSA	W	CFP	20	25	506.98	26.16	6220	NA
5962-9681801VSA.A	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHC245N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AHC245N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHC245FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC245FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC245W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54AHC245W.A	W	CFP	20	25	506.98	26.16	6220	NA





- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLATPACK - NO LEAD



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

 D. Index point is provided on cap for terminal identification only.

 E. Falls within Mil—Std 1835 GDFP2—F20







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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