

SNx4AHC244 Octal Buffers/Drivers With 3-State Outputs

1 Features

- V_{CC} operating range of 2V to 5.5V
- Latch-up performance exceeds 250mA per JESD
- On products compliant to MIL-PRF-38535, All parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- **Network Switches**
- Power Infrastructures
- PCs and Notebooks
- Wearable Health and Fitness Devices
- **Tests and Measurements**

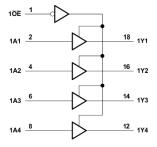
3 Description

These octal buffers and drivers are designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

Device Information

| PART NUMBER | PACKAGE ⁽¹⁾ | PACKAGE SIZE(2) | BODY SIZE(3) |
|----------------|------------------------|-------------------|-------------------|
| | J (CDIP, 20) | 24.2mm x 7.62mm | 24.2mm x 6.92mm |
| SN54AHC244 | W (CFP, 20) | 13.09mm x 8.13mm | 13.09mm x 6.92mm |
| | FK (LCCC, 20) | 8.89 mm x 8.89 mm | 8.89 mm x 8.89 mm |
| | DB (SSOP, 20) | 7.2mm × 7.8mm | 7.50mm x 5.30mm |
| | DW (SOIC, 20) | 12.80mm × 10.3mm | 12.8mm x 7.5mm |
| | N (PDIP, 20) | 24.33mm x 9.4mm | 25.40mm x 6.35mm |
| SN74AHC244 | NS (SOP, 20) | 12.60mm x 7.8mm | 12.6mm x 5.30mm |
| SIN/4AFICZ44 | DGV (TVSOP, 20) | 5.00mm x 6.4mm | 5.00mm x 4.40mm |
| | PW (TSSOP, 20) | 6.50mm × 6.4mm | 6.50mm x 4.40mm |
| | DGS (VSSOP, 20) | 5.10mm × 4.90mm | 5.10mm × 3.00mm |
| | RKS (VQFN, 20) | 4.50mm × 2.50mm | 4.50mm × 2.50mm |

- For more information, see Section 11.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



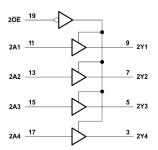




Table of Contents

| 1 Features1 | 7.2 Functional Block Diagram | . 10 |
|---|---|------|
| 2 Applications1 | 7.3 Feature Description | |
| 3 Description1 | 7.4 Device Functional Modes | |
| 4 Pin Configuration and Functions3 | 8 Application and Implementation | . 13 |
| 5 Specifications5 | 8.1 Application Information | . 13 |
| 5.1 Absolute Maximum Ratings5 | 8.2 Typical Application | |
| 5.2 ESD Ratings5 | 8.3 Power Supply Recommendations | |
| 5.3 Recommended Operating Conditions5 | 8.4 Layout | |
| 5.4 Thermal Information6 | 9 Device and Documentation Support | |
| 5.5 Electrical Characteristics6 | 9.1 Documentation Support | . 16 |
| 5.6 Switching Characteristics, V _{CC} = 3.3V ± 0.3V7 | 9.2 Receiving Notification of Documentation Updates | .16 |
| 5.7 Switching Characteristics, V _{CC} = 5V ± 0.5V7 | 9.3 Support Resources | . 16 |
| 5.8 Noise Characteristics8 | 9.4 Trademarks | |
| 5.9 Operating Characteristics8 | 9.5 Electrostatic Discharge Caution | .16 |
| 5.10 Typical Characteristics8 | 9.6 Glossary | .16 |
| 6 Parameter Measurement Information9 | 10 Revision History | |
| 7 Detailed Description10 | 11 Mechanical, Packaging, and Orderable | |
| 7.1 Overview10 | Information | . 17 |
| | | |



4 Pin Configuration and Functions

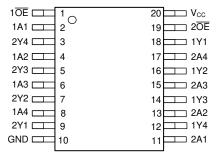


Figure 4-1. SN54AHC244 J or W Package, 20-Pin CDIP or CFP (Top View)

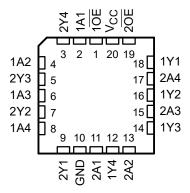


Figure 4-2. SN54AHC244 FK Package, 20-Pin LCCC (Top View)

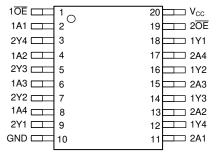


Figure 4-3. SN74AHC244 DB, DGV, DW, N, NS, PW or DGS Package, 20-Pin SSOP, TVSOP, SOIC, PDIP, SOP, TSSOP or VSSOP (Top View)

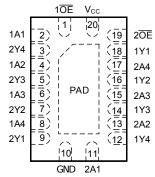


Figure 4-4. SN74AHC244 RKS Package; 20-Pin VQFN (Top View)

Table 4-1. Pin Functions

| P | IN | TYPE(1) | DESCRIPTION |
|-----|------|---------|-----------------|
| NO. | NAME | ITPE\" | DESCRIPTION |
| 1 | 1 OE | ļ | Output Enable 1 |
| 2 | 1A1 | I | 1A1 Input |
| 3 | 2Y4 | 0 | 2Y4 Output |
| 4 | 1A2 | I | 1A2 Input |
| 5 | 2Y3 | 0 | 2Y3 Output |
| 6 | 1A3 | I | 1A3 Input |
| 7 | 2Y2 | 0 | 2Y2 Output |
| 8 | 1A4 | ļ | 1A4 Input |
| 9 | 2Y1 | 0 | 2Y1 Output |
| 10 | GND | _ | Ground pin |
| 11 | 2A1 | I | 2A1 Input |
| 12 | 1Y4 | 0 | 1Y4 Output |
| 13 | 2A2 | ļ | 2A2 Input |
| 14 | 1Y3 | 0 | 1Y3 Output |
| 15 | 2A3 | I | 2A3 Input |
| 16 | 1Y2 | 0 | 1Y2 Output |
| 17 | 2A4 | I | 2A4 Input |
| 18 | 1Y1 | 0 | 1Y1 Output |



Table 4-1. Pin Functions (continued)

| P | IN | TYPE ⁽¹⁾ | DESCRIPTION |
|----------------------------|------|---------------------|--|
| NO. | NAME | ITPE\'' | DESCRIPTION |
| 19 | 2 OE | I | Output Enable 2 |
| 20 | VCC | _ | Power Pin |
| Thermal pad ⁽²⁾ | | | The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply |

- (1) Signal Types: I = Input, O = Output, I/O = Input or Output
- RKS package only



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|------------------|--|-----------------------------|------|-----------------------|------|
| V _{CC} | Supply voltage | | -0.5 | 7 | V |
| VI | Input voltage (2) | | -0.5 | 7 | V |
| Vo | Output voltage range ⁽³⁾ | | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | | -20 | mA |
| I _{OK} | Output clamp current | $V_O < 0$ or $V_O > V_{CC}$ | | ±20 | mA |
| Io | Continuous output current | $V_O = 0$ to V_{CC} | | ±25 | mA |
| | Continuous current through each V _{CC} or GND | · | | ±50 | mA |
| T _{stg} | Storage temperature | | -65 | 150 | °C |

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| | | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | ±2000 | |
| V _(ESD) | Electrostatic discharge | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ±1500 | V |

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | SN54AHC244 | | SN74AHC244 | | UNIT | |
|-----------------|------------------------------------|--|------------|-----------------|------------|-----------------|--------|--|
| | | | MIN | MAX | MIN | MAX | Oldi | |
| V _{CC} | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V | |
| | | V _{CC} = 2 V | 1.5 | | 1.5 | | | |
| V _{IH} | High-level input voltage | V _{CC} = 3 V | 2.1 | | 2.1 | | V | |
| | | V _{CC} = 5.5 V | 3.85 | | 3.85 | | | |
| | | V _{CC} = 2 V | | 0.5 | | 0.5 | | |
| V _{IL} | Low level input voltage | V _{CC} = 3 V | | 0.9 | | 0.9 | V | |
| | | V _{CC} = 5.5 V | | 1.65 | | 1.65 | | |
| VI | Input voltage | · | 0 | 5.5 | 0 | 5.5 | V | |
| Vo | Output voltage | | 0 | V _{CC} | 0 | V _{CC} | V | |
| | | V _{CC} = 2 V | | -50 | | -50 | μA | |
| I _{OH} | High-level output current | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | | -4 | | -4 | mA | |
| | | $V_{CC} = 5 V \pm 0.5 V$ | | -8 | | -8 | ША | |
| | | V _{CC} = 2 V | | 50 | | 50 | μA | |
| I _{OL} | Low level output current | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | | 4 | | 4 | mA | |
| | | $V_{CC} = 5 V \pm 0.5 V$ | | 8 | | 8 | MA | |
| Δt/Δν | Input transition rise or fall rate | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | | 100 | | 100 | ns/V | |
| ΔυΔν | input transition rise of fall fate | $V_{CC} = 5 V \pm 0.5 V$ | | 20 | | 20 | 115/ V | |

⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



over operating free-air temperature range (unless otherwise noted)(1)

| | | SN54AH0 | C244 | SN74AH | SN74AHC244 | | |
|----------------|--------------------------------|---------|------|--------|------------|------|--|
| | | MIN | MAX | MIN | MAX | UNIT | |
| T _A | Operating free-air temperature | -55 | 125 | -40 | 125 | °C | |

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.4 Thermal Information

| PACKAGE | PINS | THERMAL METRIC(1) | | | | | | | |
|-------------|------|-------------------|------------------------|------------------|-----------------|-------------|-----------------------|------|--|
| PACKAGE | PINS | R _{0JA} | R ₀ JC(top) | R _{0JB} | Ψ _{JT} | Ψ_{JB} | R _{0JC(bot)} | UNIT | |
| DB (SSOP) | 20 | 99.9 | 61.7 | 55.2 | 22.6 | 54.8 | N/A | | |
| DGV (TVSOP) | 20 | 119.2 | 34.5 | 60.7 | 1.2 | 60.0 | N/A | | |
| DW (SOIC) | 20 | 81.1 | 48.9 | 53.8 | 19.5 | 53.1 | N/A | | |
| N (PDIP) | 20 | 54.9 | 41.7 | 35.8 | 27.9 | 35.7 | N/A | °C/W | |
| NS (SOP) | 20 | 77.6 | 42.7 | 45.7 | 10.2 | 45.2 | N/A | C/VV | |
| PW (TSSOP) | 20 | 116.8 | 58.5 | 78.7 | 12.6 | 77.9 | N/A | | |
| DGS (VSSOP) | 20 | 131.6 | 69.5 | 86.7 | 10.9 | 85.9 | N/A | | |
| RKS (VQFN) | 20 | 90.4 | 92.2 | 63.4 | 29 | 63.5 | 41.3 | | |

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V | T | (= 25°C | | SN54AI | HC244 | SN74AHC244 | | UNIT |
|-----------------|--|-----------------|------|----------|-------|--------|-------------------|------------|------|------|
| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | MIN | MAX | MIN | MAX | UNII |
| | | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | |
| V _{OH} | I _{OH} = -50 μA | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | I _{OH} = -4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | I _{OH} = -8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| | | 2 V | | | 0.1 | | 0.1 | | 0.1 | |
| | I _{OL} = 50 μA | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| V _{OL} | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | I _{OL} = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | I _{OL} = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| I _I | V _I = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1 ⁽¹⁾ | | ±1 | μΑ |
| I _{OZ} | $V_O = V_{CC}$ or GND, $V_I (\overline{OE}) = V_{IL}$ or V_{IH} | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μΑ |
| I _{CC} | $V_I = V_{CC}$ or GND, $I_O = 0$ | 5.5 V | | | 4 | | 40 | <u> </u> | 40 | μΑ |
| C _i | V _I = V _{CC} or GND | 5 V | | 2 | 10 | | | | 10 | pF |
| Co | V _O = V _{CC} or GND | 5 V | | 3.5 | | | | | | pF |

⁽¹⁾ On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0 \text{ V}$.



5.6 Switching Characteristics, $V_{CC} = 3.3V \pm 0.3V$

over recommended operating free-air temperature range, V_{CC} = 3.3V \pm 0.3V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| DADAMETED | FROM | то | LOAD | • | T _A = 25°C | | SN54AH | IC244 | SN74AHC244 | | LINIT | | | |
|--------------------|---------|----------|-----------------------|-----|-----------------------|---------------------|------------------|---------------------|------------|------|-------|---|----|---|
| PARAMETER | (INPUT) | (OUTPUT) | CAPACITANCE | MIN | TYP | MAX | MIN | MAX | MIN | MAX | UNIT | | | |
| t _{PLH} | А | Y | C _L = 15pF | | 5.8 ⁽¹⁾ | 8.4 ⁽¹⁾ | 1 ⁽¹⁾ | 10 ⁽¹⁾ | 1 | 10 | ns | | | |
| t _{PHL} | | Ţ | CL = 15pr | | 5.8 ⁽¹⁾ | 8.4 ⁽¹⁾ | 1 ⁽¹⁾ | 10 ⁽¹⁾ | 1 | 10 | 115 | | | |
| t _{PZH} | - OE | Y | C _L = 15pF | | 6.6 ⁽¹⁾ | 10.6 ⁽¹⁾ | 1 ⁽¹⁾ | 12.5 ⁽¹⁾ | 1 | 12.5 | ns | | | |
| t _{PZL} | | I | CL = 13pr | | 6.6 ⁽¹⁾ | 10.6 ⁽¹⁾ | 1 ⁽¹⁾ | 12.5 ⁽¹⁾ | 1 | 12.5 | 115 | | | |
| t _{PHZ} | ŌĒ | Y | C _L = 15pF | | 5 ⁽¹⁾ | 9.7 ⁽¹⁾ | 1 ⁽¹⁾ | 11 ⁽¹⁾ | 1 | 11 | ns | | | |
| t_{PLZ} | OE | I | OL - 13pi | | 5 ⁽¹⁾ | 9.7 ⁽¹⁾ | 1 ⁽¹⁾ | 11 ⁽¹⁾ | 1 | 11 | 115 | | | |
| t _{PLH} | А | Y | C _L = 50pF | | 8.3 | 11.9 | 1 | 13.5 | 1 | 13.5 | ns | | | |
| t _{PHL} | Α | Ĭ | C _L = 50pr | | 8.3 | 11.9 | 1 | 13.5 | 1 | 13.5 | 115 | | | |
| t _{PZH} | ŌĒ | Y | C _L = 50pF | | 9.1 | 14.1 | 1 | 16 | 1 | 16 | ns | | | |
| t _{PZL} | OL | I | OL - 30pi | | 9.1 | 14.1 | 1 | 16 | 1 | 16 | 115 | | | |
| t _{PHZ} | ŌĒ | Y | C _L = 50pF | | 10.3 | 14 | 1 | 16 | 1 | 16 | ns | | | |
| t _{PLZ} | UE | UE | OE | OL | OE T | OL - 30PF | | 10.3 | 14 | 1 | 16 | 1 | 16 | i |
| t _{sk(o)} | | | C _L = 50pF | | | 1.5 ⁽²⁾ | | | | 1.5 | ns | | | |

⁽¹⁾ On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.7 Switching Characteristics, $V_{CC} = 5V \pm 0.5V$

over recommended operating free-air temperature range, $V_{CC} = 5V \pm 0.5V$ (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| | FROM | то | LOAD CAPACITANCE | T | _ = 25°C | | SN54AH | IC244 | SN74AHC244 | | |
|--------------------|---------|---------|-----------------------|-----------|--------------------|--------------------|------------------|--------------------|------------|------|------|
| PARAMETER | (INPUT) | (OUTPUT | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | UNIT |
| t _{PLH} | Α | Y | C ₁ = 15pF | | 3.9 ⁽¹⁾ | 5.5 ⁽¹⁾ | 1 ⁽¹⁾ | 6.5 ⁽¹⁾ | 1 | 6.5 | ns |
| t _{PHL} | A A | T T | C _L = 15pr | | 3.9 ⁽¹⁾ | 5.5 ⁽¹⁾ | 1 ⁽¹⁾ | 6.5 ⁽¹⁾ | 1 | 6.5 | 115 |
| t _{PZH} | ŌĒ | Υ | C ₁ = 15pF | | 4.7 ⁽¹⁾ | 7.3 ⁽¹⁾ | 1 ⁽¹⁾ | 8.5 ⁽¹⁾ | 1 | 8.5 | ns |
| t _{PZL} | OE . | ľ | CL = 13pr | | 4.7 ⁽¹⁾ | 7.3 ⁽¹⁾ | 1 ⁽¹⁾ | 8.5 ⁽¹⁾ | 1 | 8.5 | 115 |
| t _{PHZ} | ŌĒ | Y | C _L = 15pF | | 5 ⁽¹⁾ | 7.2 ⁽¹⁾ | 1 ⁽¹⁾ | 8.5 ⁽¹⁾ | 1 | 8.5 | ns |
| t _{PLZ} | OL | ľ | CL = 13pr | | 5 ⁽¹⁾ | 7.2 ⁽¹⁾ | 1 ⁽¹⁾ | 8.5 ⁽¹⁾ | 1 | 8.5 | 115 |
| t _{PLH} | Α | Y | C ₁ = 50pF | | 5.4 | 7.5 | 1 | 8.5 | 1 | 8.5 | ns |
| t _{PHL} | | ľ | C _L = 50pr | | 5.4 | 7.5 | 1 | 8.5 | 1 | 8.5 | 115 |
| t _{PZH} | ŌĒ | Y | C ₁ = 50pF | | 6.2 | 9.3 | 1 | 10.5 | 1 | 10.5 | ns |
| t _{PZL} | OL | ľ | CL = 30pr | | 6.2 | 9.3 | 1 | 10.5 | 1 | 10.5 | 115 |
| t _{PHZ} | ŌĒ | Υ | C ₁ = 50pF | | 6.7 | 9.2 | 1 | 10.5 | 1 | 10.5 | ns |
| t _{PLZ} | | - OE | | OL - 30pr | | 6.7 | 9.2 | 1 | 10.5 | 1 | 10.5 |
| t _{sk(o)} | | | C _L = 50pF | | | 1 ⁽²⁾ | | | | 1 | ns |

¹⁾ On products compliant to MIL-PRF-38535, this parameter is not production tested.

⁽²⁾ On products compliant to MIL-PRF-38535, this parameter does not apply.

⁽²⁾ On products compliant to MIL-PRF-38535, this parameter does not apply.



5.8 Noise Characteristics

 V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C ⁽¹⁾

| | PARAMETER | SN74 | UNIT | | |
|--------------------|---|------|------|-----|------|
| | PARAMETER | MIN | TYP | MAX | UNII |
| V _{OL(P)} | Quiet output, maximum dynamic V _{OL} | | 0.5 | | V |
| V _{OL(V)} | Quiet output, minimum dynamic V _{OL} | | -0.2 | | V |
| V _{OH(V)} | Quiet output, minimum dynamic V _{OH} | | 4.8 | | V |
| V _{IH(D)} | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

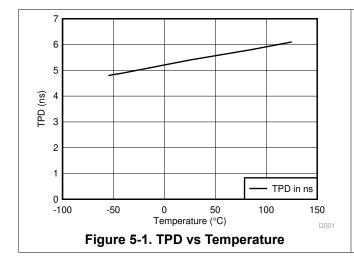
(1) Characteristics are for surface-mount packages only.

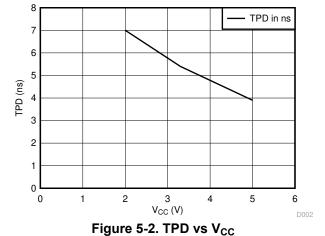
5.9 Operating Characteristics

 $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

| PARAMETER | | TEST CC | ONDITIONS | TYP | UNIT |
|-----------------|-------------------------------|----------|-----------|-----|------|
| C _{pd} | Power dissipation capacitance | No load, | f = 1 MHz | 8.6 | pF |

5.10 Typical Characteristics



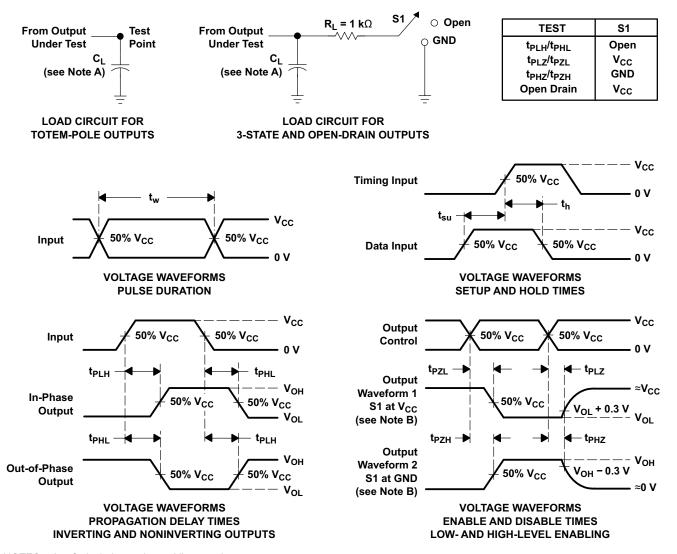


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6 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq 3$ ns. $t_f \leq 3$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SNx4AHC244 contains 8 individual high speed CMOS buffers organized as two 4-bit buffers/line drives with 3-state outputs.

Each buffer performs the boolean logic function xYn = xAn, with x being the bank number and n being the channel number.

Each output enable $(x\overline{OE})$ controls four buffers. When the $x\overline{OE}$ pin is in the low state, the outputs of all buffers in the bank x are enabled. When the $x\overline{OE}$ pin is in the high state, the outputs of all buffers in the bank x are disabled. All disabled output are placed into the high-impedance state.

To put the device in the high-impedance state during power up or power down, tie both \overline{OE} pins to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver and the leakage of the pin as defined in the *Electrical Characteristics* table.

7.2 Functional Block Diagram

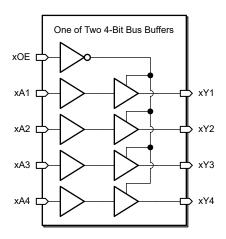


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output



voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a $10k\Omega$ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

7.3.3 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law $(R = V \div I)$.

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a $10k\Omega$ resistor, however, is recommended and will typically meet all requirements.



7.3.4 Clamp Diode Structure

As Figure 7-2 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the Absolute Maximum Ratings table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clampcurrent ratings are observed.

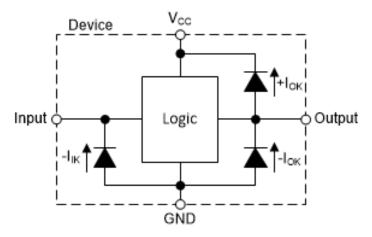


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SNx4AHC244.

| INPU | OUTPUTS | | | | | |
|------|---------|---|--|--|--|--|
| ŌĒ | ŌĒ A | | | | | |
| L | L | L | | | | |
| L | Н | Н | | | | |
| Н | Х | Z | | | | |

Table 7-1. Function Table

H = High Voltage Level, L = Low Voltage Level, X = Do Not (1) Care, Z = High-Impedance State

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

SNx4AHC244 is a high drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern. The inputs can accept voltages to 5.5V at any valid V_{CC} making it ideal for down translation.

8.2 Typical Application

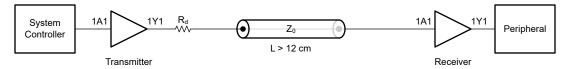


Figure 8-1. Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents in excess of maximum limits. The high drive will also create fast edges into light loads, so consider routing and load conditions to prevent ringing.

8.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions:
 - For rise time and fall time specification, see ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
 - For specified high and low levels, see (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
 - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the Recommended Operating
 Conditions table at any valid V_{CC}.
- 2. Recommended maximum Output Conditions:
 - Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.
 - Outputs should not be pulled above V_{CC}.

8.2.3 Application Curves

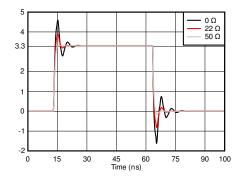


Figure 8-2. Simulated Signal Integrity at the Receiver With Different Damping Resistor (R_d) Values

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A $0.1\mu F$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\mu F$ and $1\mu F$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

- · Bypass capacitor placement
 - Place near the positive supply terminal of the device
 - Provide an electrically short ground return path
 - Use wide traces to minimize impedance
 - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
 - 8mil to 12mil trace width
 - Lengths less than 12cm to minimize transmission line effects
 - Avoid 90° corners for signal traces
 - Use an unbroken ground plane below signal traces
 - Flood fill areas around signal traces with ground
 - Parallel traces must be separated by at least 3x dielectric thickness
 - For traces longer than 12cm
 - · Use impedance controlled traces
 - Source-terminate using a series damping resistor near the output
 - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

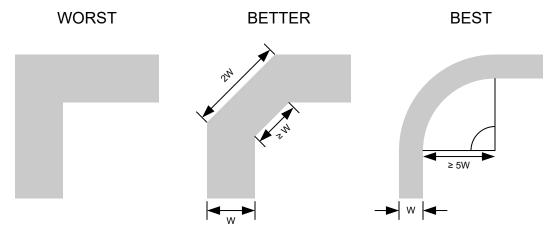


Figure 8-3. Example Trace Corners for Improved Signal Integrity

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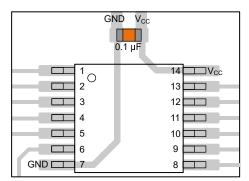


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

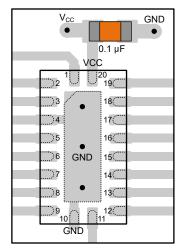


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

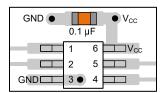


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

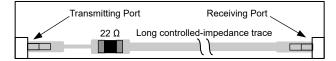


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity



9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and Cpd Calculation application report
- Texas Instruments, Designing With Logic application report
- Texas Instruments, Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision M (January 2025) to Revision N (June 2025) | Page |
|---|------|
| Added VSSOP and VQFN to Device Information table Added Overview section, Feature Description section, Application Information section, and Typical Application section | 1 |
| Added DGS and RKS packages to Pin Configurations and Functions | |
| Changes from Revision L (July 2024) to Revision M (January 2025) | Page |
| Updated HBM and CDM values in ESD Ratings table | 5 |

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material | MSL rating/ Peak reflow | Op temp (°C) | Part marking (6) |
|-----------------------|------------|---------------|------------------|-----------------------|-----------------|-------------------------------|----------------------------|--------------|--|
| 5962-9678201Q2A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9678201Q2A SNJ54AHC 244FK |
| 5962-9678201QRA | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9678201QR A SNJ54AHC244J |
| 5962-9678201QSA | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9678201QS A SNJ54AHC244W |
| 5962-9678201VRA | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9678201VR A SNV54AHC244J |
| 5962-9678201VRA.A | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9678201VR A SNV54AHC244J |
| 5962-9678201VSA | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9678201VS A SNV54AHC244W |
| 5962-9678201VSA.A | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9678201VS A SNV54AHC244W |
| SN74AHC244DBR | Active | Production | SSOP (DB) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA244 |
| SN74AHC244DBR.A | Active | Production | SSOP (DB) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA244 |
| SN74AHC244DBRE4 | Active | Production | SSOP (DB) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA244 |
| SN74AHC244DGSR | Active | Production | VSSOP (DGS) 20 | 5000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC244 |
| SN74AHC244DGVR | Active | Production | TVSOP (DGV) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA244 |
| SN74AHC244DGVR.A | Active | Production | TVSOP (DGV) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA244 |
| SN74AHC244DW | Obsolete | Production | SOIC (DW) 20 | - | = | Call TI | Call TI | -40 to 125 | AHC244 |
| SN74AHC244DWR | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC244 |
| SN74AHC244DWR.A | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC244 |
| SN74AHC244DWRG4 | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC244 |
| SN74AHC244N | Active | Production | PDIP (N) 20 | 20 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74AHC244N |





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| Orderable part number | Status (1) | Material type | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material | MSL rating/ Peak reflow | Op temp (°C) | Part marking (6) |
|-----------------------|------------|---------------|-----------------|-----------------------|-----------------|-------------------------------|----------------------------|--------------|--|
| SN74AHC244N.A | Active | Production | PDIP (N) 20 | 20 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74AHC244N |
| SN74AHC244NSR | Active | Production | SOP (NS) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC244 |
| SN74AHC244NSR.A | Active | Production | SOP (NS) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC244 |
| SN74AHC244PW | Obsolete | Production | TSSOP (PW) 20 | - | - | Call TI | Call TI | -40 to 125 | HA244 |
| SN74AHC244PWR | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | HA244 |
| SN74AHC244PWR.A | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HA244 |
| SN74AHC244PWRE4 | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA244 |
| SN74AHC244PWRG4 | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA244 |
| SN74AHC244PWRG4.A | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA244 |
| SN74AHC244RKSR | Active | Production | VQFN (RKS) 20 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC244 |
| SNJ54AHC244FK | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9678201Q2A SNJ54AHC 244FK |
| SNJ54AHC244FK.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9678201Q2A SNJ54AHC 244FK |
| SNJ54AHC244J | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9678201QR A SNJ54AHC244J |
| SNJ54AHC244J.A | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9678201QR A SNJ54AHC244J |
| SNJ54AHC244W | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9678201QS A SNJ54AHC244W |
| SNJ54AHC244W.A | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9678201QS A SNJ54AHC244W |

⁽¹⁾ Status: For more details on status, see our product life cycle.

PACKAGE OPTION ADDENDUM

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(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC244, SN54AHC244-SP, SN74AHC244:

Catalog: SN74AHC244, SN54AHC244

Automotive: SN74AHC244-Q1, SN74AHC244-Q1

Enhanced Product: SN74AHC244-EP, SN74AHC244-EP

Military: SN54AHC244

Space : SN54AHC244-SP

NOTE: Qualified Version Definitions:



PACKAGE OPTION ADDENDUM

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- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application



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TAPE AND REEL INFORMATION





| A0 | Dimension designed to accommodate the component width |
|----|---|
| В0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|-----------------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| SN74AHC244DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AHC244DGSR | VSSOP | DGS | 20 | 5000 | 330.0 | 16.4 | 5.4 | 5.4 | 1.45 | 8.0 | 16.0 | Q1 |
| SN74AHC244DGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHC244DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AHC244DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AHC244NSR | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74AHC244PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74AHC244PWRG4 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74AHC244PWRG4 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74AHC244RKSR | VQFN | RKS | 20 | 3000 | 180.0 | 12.4 | 2.8 | 4.8 | 1.2 | 4.0 | 12.0 | Q1 |



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*All dimensions are nominal

| 7 til dilitiononono di o momina | | | | | | | |
|---------------------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
| SN74AHC244DBR | SSOP | DB | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHC244DGSR | VSSOP | DGS | 20 | 5000 | 353.0 | 353.0 | 32.0 |
| SN74AHC244DGVR | TVSOP | DGV | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHC244DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74AHC244DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74AHC244NSR | SOP | NS | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74AHC244PWR | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHC244PWRG4 | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHC244PWRG4 | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHC244RKSR | VQFN | RKS | 20 | 3000 | 210.0 | 185.0 | 35.0 |

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|-------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9678201Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9678201QSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| 5962-9678201VSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| 5962-9678201VSA.A | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74AHC244N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74AHC244N.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54AHC244FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AHC244FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AHC244W | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54AHC244W.A | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

 D. Index point is provided on cap for terminal identification only.

 E. Falls within Mil—Std 1835 GDFP2—F20







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







NOTES:

PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. No JEDEC registration as of September 2020.
- 5. Features may differ or may not be present.





NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
- 9. Size of metal pad may vary due to creepage requirement.
- 10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.





NOTES: (continued)

- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com



PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194 8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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