







SN54ACT373, SN74ACT373

SCAS544F - OCTOBER 1995 - REVISED MAY 2024

SNx4ACT373 Octal D-Type Transparent Latches with 3-State Outputs

1 Features

- Operation of 4.5V to 5.5V V_{CC}
- Inputs accept voltages to 5.5V
- Max t_{pd} of 10ns at 5V
- Inputs are TTL-voltage compatible

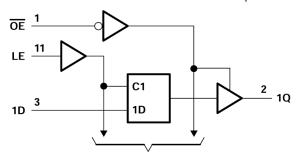
2 Description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)	BODY SIZE(3)
	DB (SSOP, 20)	7.2mm × 7.8mm	7.50mm x 5.30mm
	DW (SOIC, 20)	12.8mm × 10.3mm	12.80mm x 7.50mm
SNx4ACT373	N (PDIP, 20)	24.33mm × 9.4mm	24.33mm x 6.35mm
	NS (SOP, 20)	12.6mm × 7.8mm	12.6mm x 5.3mm
	PW (TSSOP, 20)	6.5mm × 6.4mm	6.50mm x 4.40mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- The package size (length × width) is a nominal value and (2)includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



To Seven Other Channels Logic Diagram (Positive Logic)

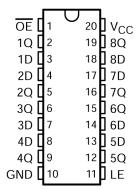


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3 Pin Configuration and Functions



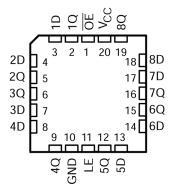


Figure 3-1. SN54ACT373 J or W Package; SN74ACT373 DB, DW, N, NS, or PW Package (Top View)

Figure 3-2. SN54ACT373 FK Package (Top View)

Table 3-1. Pin Functions

	PIN					
NO.	SSOP, TVSOP, SOIC, SO, or TSSOP	VQFN	TYPE	DESCRIPTION		
1	ŌĒ	ŌĒ	I	Output Enable		
2	1Q	1Q	0	1Q Output		
3	1D	1D	I	1D Input		
4	2D	2D	I	2D Input		
5	2Q	2Q	0	2Q Output		
6	3Q	3Q	0	3Q Output		
7	3D	3D	I	3D Input		
8	4D	4D	I	4D Input		
9	4Q	4Q	0	4Q Output		
10	GND	GND	_	Ground Pin		
11	LE	LE	I	Latch Enable		
12	5Q	5Q	0	5Q Output		
13	5D	5D	I	5D Input		
14	6D	6D	I	6D Input		
15	6Q	6Q	0	6Q Output		
16	7Q	7Q	0	7Q Output		
17	7D	7D	I	7D Input		
18	8D	8D	I	8D Input		
19	8Q	8Q	0	8Q Output		
20	V _{CC}	V _{CC}	_	Power Pin		



4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
V _I ²	Input voltage range		-0.5	V _{CC} + 0.5	V
V _O ²	Output voltage range		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	$(V_I < 0 \text{ or } V_I > V_{CC)}$		±20	mA
I _{OK}	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC)}$		±20	mA
Io	Continuous output current	$(V_O = 0 \text{ to } V_{CC})$		±50	mA
	Continuous current through V _{CC} or C		±200	mA	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		SN54ACT3	73	SN74ACT3	73	LINUT
		MIN	MAX	MIN	MAX	UNIT
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
VI	Input voltage	0	V _{CC}	0	V _{CC}	V
Vo	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-24		-24	mA
I _{OL}	Low-level output current		24		24	mA
Δt/Δν	Input transition rise or fall rate		8		8	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

4.3 Thermal Information

THERMAL METRIC(1)			SNx4ACT373						
		THERMAL METRIC ⁽¹⁾ DB (SSOP) DW (SOIC) N (PDIP) NS (SO) PW (TSSOP)							
				20 PINS					
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.2	101.2	69	60	126.2	°C/W		

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	.,	T _A = :	25°C		SN54AC	T373	SN74AC	T373	LINUT
PARAMETER		V _{CC}	MIN T	ΥP	MAX	MIN	MAX	MIN	MAX	UNIT
	L - 50A	4.5 V	4.4 4	1.49		4.4		4.4		
	I _{OH} = -50 μA	5.5 V	5.4 5	.49		5.4		5.4		
.,	1 - 24 mA	4.5 V	3.86			3.7		3.76		V
V _{OH}	$I_{OH} = -24 \text{ mA}$	5.5 V	4.86			4.7		4.76		V
	I _{OH} = -50 mA ⁽¹⁾	5.5 V				3.85				
	I _{OH} = -75 mA ⁽¹⁾	5.5 V						3.85		
	I _{OL} = 50μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
.,	I _{OL} = 24 mA	4.5 V	,		0.36		0.44		0.44	
V _{OL}		5.5 V			0.36		0.44		0.44	
	I _{OL} = 50 mA ⁽¹⁾	5.5 V					1.65			
	I _{OL} = 75 mA ⁽¹⁾	5.5 V							1.65	
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.25		±5		±2.5	μA
I _I	V _I = V _{CC} or GND	5.5 V	,		±0.1		±1		±1	μA
I _{cc}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		80		40	μA
Δl _{CC} ⁽²⁾	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V		0.6			1.5		1.5	mA
Ci	V _I = V _{CC} or GND	5 V		4.5						pF

⁽¹⁾ Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

4.5 Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

		T _A = 25°	С	SN54ACT373 SN74ACT373		UNIT
		MIN	MAX	MIN MAX	MIN MAX	CINIT
t _w	Pulse duration, LE high	7		8.5	8	ns
t _{su}	Setup time, data before LE↓	7		8.5	8	ns
t _h	Hold time, data after LE↓	0		1	1	ns

⁽²⁾ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.



4.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TA	= 25°C		SN54A	CT373	SN74A	CT373	UNIT
PARAMETER	PROW (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
t _{PLH}	D	Q	2.5	8.5	10	1.5	12.5	1.5	11.5	ns
t _{PHL}	Б	Q	2	8	10	1.5	12.5	1.5	11.5	115
t _{PLH}	LE	Q	2.5	8.5	11	1.5	12.5	2	11.5	ns
t _{PHL}	LE	ų ų	2	8	10	1.5	11.5	1.5	11.5	115
t _{PZH}	ŌĒ	Q	2	8	9.5	1.5	11.5	1.5	10.5	ns
t _{PZL}	OL	Q	2	7.5	9	1.5	11	1.5	10.5	115
t _{PHZ}	ŌĒ	Q	2.5	9	11	1.5	14	2.5	12.5	ns
t _{PLZ}	OL	l Q	1.5	7.5	8.5	1.5	11	1	10	115

4.7 Operating Characteristics

 $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

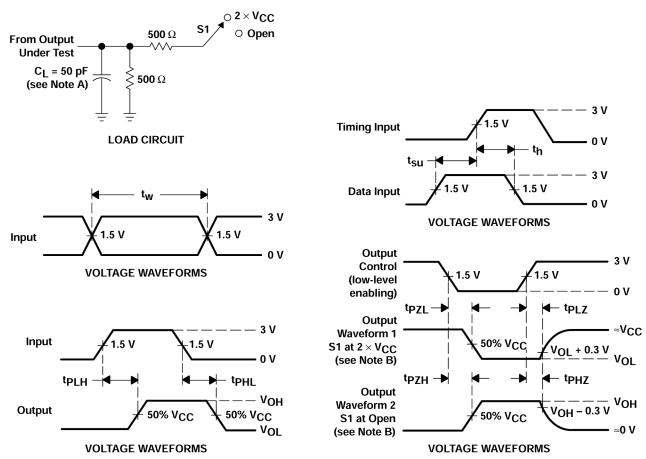
	PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	$C_L = 50 \text{ pF},$	f = 1 MHz	40	pF

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5 Parameter Measurement Information



- A. C₁ includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 5-1. Load Circuit and Voltage Waveforms

TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	2 × V _{CC}
t _{PHZ} /t _{PZH}	Open

6 Detailed Description

6.1 Overview

The eight latches are D-type transparent latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines in bus-organized systems without need for interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

6.2 Functional Block Diagram

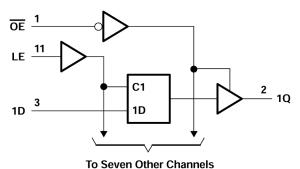


Figure 6-1. Logic Diagram (Positive Logic)

6.3 Device Functional Modes

Table 6-1. Function Table (Each Latch)

INPUTS			OUTPUT Q
OE	LE	D	
L	Н	Н	Н
L	Н	L	L
L	L	Х	Q_0
Н	Х	Х	Z



7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the Section 4.2.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended; if there are multiple V_{CC} pins, then 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and a 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Layout Diagram are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

7.2.2 Layout Example

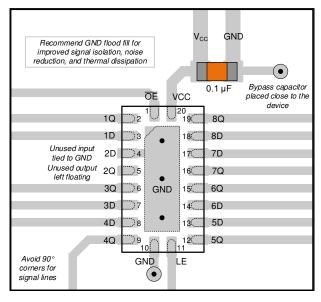


Figure 7-1. Layout example for the SNx4ACT373



8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	
SN54ACT373	Click here	Click here	Click here	Click here	Click here	
SN74ACT373	Click here	Click here	Click here	Click here	Click here	

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

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8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (October 2002) to Revision F (May 2024)

Page

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-87556012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87556012A SNJ54ACT 373FK
5962-8755601RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8755601RA SNJ54ACT373J
5962-8755601SA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8755601SA SNJ54ACT373W
5962-8755601VRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8755601VR A SNV54ACT373J
5962-8755601VRA.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8755601VR A SNV54ACT373J
SN74ACT373DBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD373
SN74ACT373DBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD373
SN74ACT373DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 85	ACT373
SN74ACT373DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT373
SN74ACT373DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT373
SN74ACT373N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT373N
SN74ACT373N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT373N
SN74ACT373NSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT373
SN74ACT373NSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT373
SN74ACT373PW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 85	AD373
SN74ACT373PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD373
SN74ACT373PWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD373
SNJ54ACT373FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87556012A SNJ54ACT 373FK





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Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SNJ54ACT373FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87556012A SNJ54ACT 373FK
SNJ54ACT373J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8755601RA SNJ54ACT373J
SNJ54ACT373J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8755601RA SNJ54ACT373J
SNJ54ACT373W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8755601SA SNJ54ACT373W
SNJ54ACT373W.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8755601SA SNJ54ACT373W

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ACT373, SN54ACT373-SP, SN74ACT373:

Catalog: SN74ACT373, SN54ACT373

● Enhanced Product: SN74ACT373-EP, SN74ACT373-EP

Military: SN54ACT373

Space: SN54ACT373-SP

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

• Military - QML certified for Military and Defense Applications

• Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT373DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ACT373DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74ACT373DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ACT373NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ACT373PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1



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*All dimensions are nominal

7 III GIIII GII GII GII GII GII GII GII							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT373DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74ACT373DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ACT373DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ACT373NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74ACT373PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

www.ti.com 23-Jul-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-87556012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8755601SA	W	CFP	20	25	506.98	26.16	6220	NA
SN74ACT373N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ACT373N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ACT373FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT373FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT373W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54ACT373W.A	W	CFP	20	25	506.98	26.16	6220	NA





- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

 D. Index point is provided on cap for terminal identification only.

 E. Falls within Mil—Std 1835 GDFP2—F20







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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