

SNx4AC32 Quadruple 2-Input Positive-OR Gates

1 Features

- 2V to 6V V_{CC} operation
- Inputs accept voltages to 6V
- Maximum t_{pd} of 7.5ns at 5V

2 Description

The 'AC32 devices are quadruple 2-input positive-OR gates. The devices perform the Boolean function $Y = A + B$ or $Y = \bar{A} \times \bar{B}$ in positive logic.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SNx4AC32	DB (SSOP, 14)	6.2mm × 7.8mm	6.2mm × 5.3mm
	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm
	N (PDIP, 14)	19.3mm × 9.4mm	19.3mm × 6.35mm
	NS (SO, 14)	10.2mm × 7.8mm	10.3mm × 5.3mm
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm
	BQA (WQFN)	3mm × 2.5mm	3mm × 2.5mm

- (1) For more information, see [Section 10](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram, Each Gate (Positive Logic)



Table of Contents

1 Features	1	6.2 Device Functional Modes.....	9
2 Description	1	7 Application and Implementation	10
3 Pin Configuration and Functions	3	7.1 Power Supply Recommendations.....	10
4 Specifications	5	7.2 Layout.....	10
4.1 Absolute Maximum Ratings.....	5	8 Device and Documentation Support	11
4.2 Recommended Operating Conditions.....	5	8.1 Documentation Support.....	11
4.3 Thermal Information.....	6	8.2 Receiving Notification of Documentation Updates....	11
4.4 Electrical Characteristics.....	6	8.3 Support Resources.....	11
4.5 Switching Characteristics, $V_{CC} = 3.3V \pm 0.3V$	7	8.4 Trademarks.....	11
4.6 Switching Characteristics, $V_{CC} = 5V \pm 0.5V$	7	8.5 Electrostatic Discharge Caution.....	11
4.7 Operating Characteristics.....	7	8.6 Glossary.....	11
5 Parameter Measurement Information	8	9 Revision History	11
6 Detailed Description	9	10 Mechanical, Packaging, and Orderable Information	12
6.1 Functional Block Diagram.....	9		

3 Pin Configuration and Functions

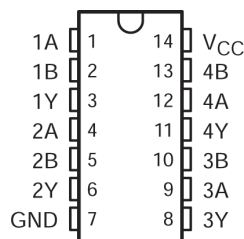
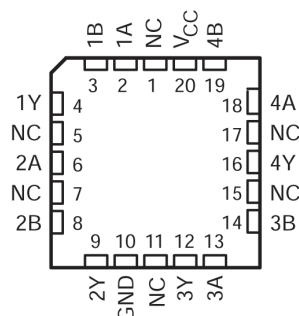


Figure 3-1. SN54AC32 J or W Package, 14-Pin CDIP or CFP; SN74AC32 D, DB, N, NS, or PW Package, 14-Pin SOIC, SSOP, PDIP, SOP, or TSSOP (Top View)



NC – No internal connection
Figure 3-2. SN54AC32 FK Package, 14-Pin LCCC (Top View)

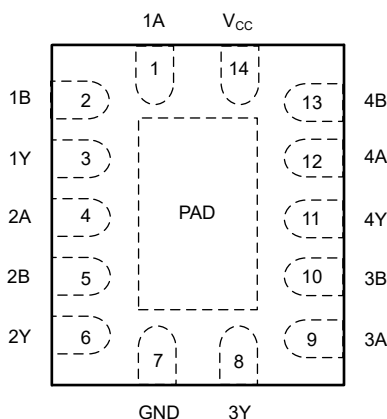


Figure 3-3. SN74AC32 BQA Package, 14-Pin WQFN (Top View)

Table 3-1. Pin Functions

PIN				TYPE ⁽¹⁾	DESCRIPTION
NAME	SN74AC32	SN54AC32			
	D, DB, DGV, N, NS, PW, RGY, BQA	J, W	FK		
1A	1	1	2	I	1A Input
1B	2	2	3	I	1B Input
1Y	3	3	4	O	1Y Output
2A	4	4	6	I	2A Input
2B	5	5	8	I	2B Input
2Y	6	6	9	O	2Y Output
3A	9	9	13	I	3A Input
3B	10	10	14	I	3B Input
3Y	8	8	12	O	3Y Output
4A	12	12	18	I	4A Input
4B	13	13	19	I	4B Input
4Y	11	11	16	O	4Y Output

Table 3-1. Pin Functions (continued)

PIN				TYPE ⁽¹⁾	DESCRIPTION
NAME	SN74AC32	SN54AC32			
	D, DB, DGV, N, NS, PW, RGY, BQA	J, W	FK		
GND	7	7	10	—	Ground Pin
NC	—	—	1, 5, 7, 11, 15, 17	—	No Connection
V _{CC}	14	14	20	—	Power Pin
Thermal Pad ⁽²⁾				—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

(2) BQA Package Only

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	7	V
V_I ⁽²⁾	Input voltage range	-0.5	$V_{CC} + 0.5$	V
V_O ⁽²⁾	Output voltage range	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$(V_I < 0 \text{ or } V_I > V_{CC})$		±20 mA
I_{OK}	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC})$		±20 mA
I_O	Continuous output current	$(V_O = 0 \text{ to } V_{CC})$		±50 mA
I_O	Continuous current through V_{CC} or GND			±200 mA
T_{stg}	Storage temperature range	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN54AC32		SN74AC32		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	6	2	6	V
V_{IH}	High-level input voltage	$V_{CC} = 3 \text{ V}$	2.1		2.1		V
		$V_{CC} = 4.5 \text{ V}$	3.15		3.15		
		$V_{CC} = 5.5 \text{ V}$	3.85		3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 3 \text{ V}$		0.9		0.9	V
		$V_{CC} = 4.5 \text{ V}$		1.35		1.35	
		$V_{CC} = 5.5 \text{ V}$		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 3 \text{ V}$		-12		-12	mA
		$V_{CC} = 4.5 \text{ V}$		-24		-24	
		$V_{CC} = 5.5 \text{ V}$		-24		-24	
I_{OL}	Low-level output current	$V_{CC} = 3 \text{ V}$		12		12	mA
		$V_{CC} = 4.5 \text{ V}$		24		24	
		$V_{CC} = 5.5 \text{ V}$		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			8		8	ns/V
T_A	Operating free-air temperature		-55	125	-55	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the [Implications of Slow or Floating CMOS Inputs](#) application note.

4.3 Thermal Information

THERMAL METRIC ⁽¹⁾		SNx4AC32						UNIT
		BQA (WQFN)	D (SOIC)	DB (SSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	91.3	119.9	96	80	76	145.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99.4	—	—	—	—	—	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.0	—	—	—	—	—	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.5	—	—	—	—	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.8	—	—	—	—	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	37.0	—	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application note.

4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54AC32		SN74AC32		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50\mu\text{A}$		3V	2.9			2.9		2.9		V
			4.5V	4.4			4.4		4.4		
			5.5V	5.4			5.4		5.4		
	$I_{OH} = -12\text{mA}$		3V	2.56			2.4		2.4		
			4.5V	3.86			3.7		3.7		
	$I_{OH} = -24\text{mA}$		5.5V	4.86			4.7		4.7		
			5.5V				3.85		3.85		
V_{OL}	$I_{OL} = 50\mu\text{A}$		3V		0.002	0.1		0.1		0.1	V
			4.5V		0.001	0.1		0.1		0.1	
			5.5V		0.001	0.1		0.1		0.1	
	$I_{OL} = 12\text{mA}$		3V			0.36		0.5		0.5	
			4.5V			0.36		0.5		0.5	
	$I_{OL} = 24\text{mA}$		5.5V			0.36		0.5		0.5	
			5.5V				1.65		1.65		
I_L	A or B ports	$V_I = V_{CC}$ or GND	5.5V			± 0.1		± 1		± 1	μA
			5.5V			2		40		40	μA
C_i		$V_I = V_{CC}$ or GND	5V		2.6						pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2ms.

4.5 Switching Characteristics, $V_{CC} = 3.3V \pm 0.3V$

over recommended operating free-air temperature range, $V_{CC} = 3.3V \pm 0.3V$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ C$			SN54AC32		SN74AC32		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	7	9	1	12	1	12	ns
t_{PHL}			1.5	7	8.5	1	11.5	1	11.5	

4.6 Switching Characteristics, $V_{CC} = 5V \pm 0.5V$

over recommended operating free-air temperature range, $V_{CC} = 5V \pm 0.5V$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

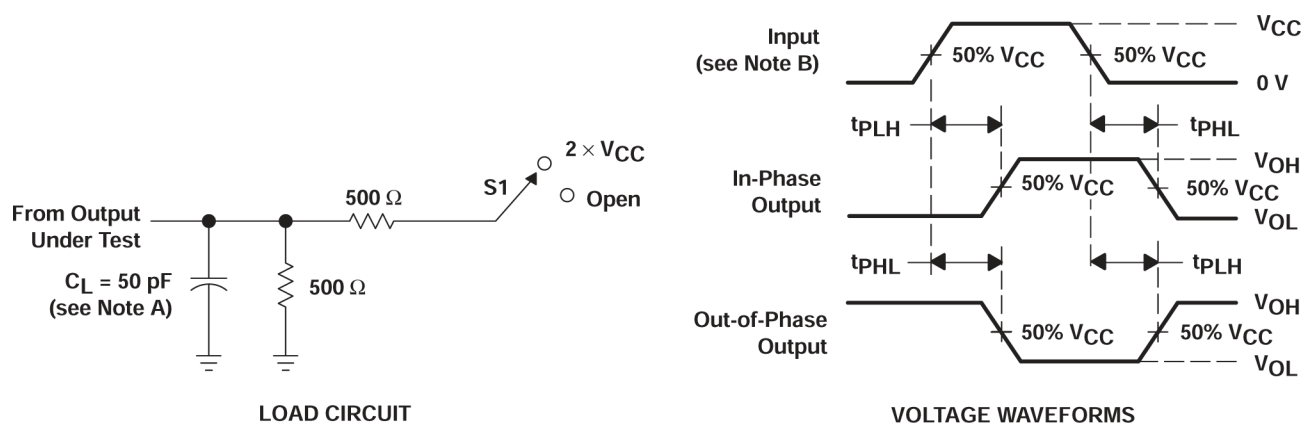
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ C$			SN54AC32		SN74AC32		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	5.5	7.5	1	9	1	9	ns
t_{PHL}			1.5	5	7	1	8.5	1	8.5	

4.7 Operating Characteristics

$V_{CC} = 5V$, $T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50pF$,	$f = 1MHz$	40	pF

5 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 5-1. Load Circuit and Voltage Waveforms

TEST	S1
t_{PLH}/t_{PHL}	Open

6 Detailed Description

6.1 Functional Block Diagram



Figure 6-1. Logic Diagram, Each Gate (Positive Logic)

6.2 Device Functional Modes

Table 6-1. Function Table (Each Gate)

INPUTS		OUTPUT Y
A	B	
H	X	H
X	H	H
L	L	L

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#). Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1 μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1 μF and 1 μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in [Figure 7-1](#).

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

7.2.2 Layout Example

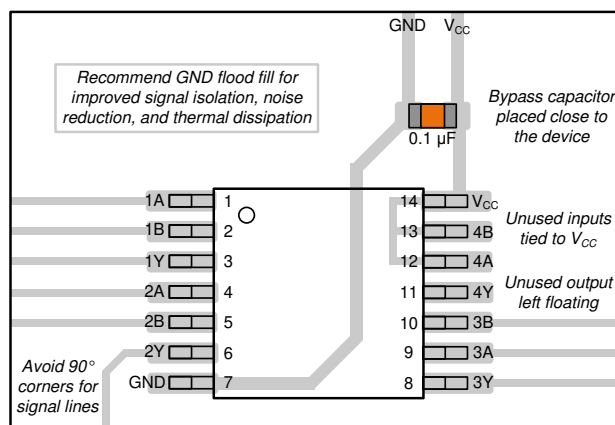


Figure 7-1. Layout Example for the SNx4AC32

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AC32	Click here	Click here	Click here	Click here	Click here
SN74AC32	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (February 2025) to Revision H (April 2025)	Page
• Added BQA Package.....	3
• Added BQA thermal information.....	6

Changes from Revision F (December 2024) to Revision G (February 2025)	Page
• Updated SN74AC32 operating temperature to 125°C and respective values in <i>Recommended Operating Conditions</i> table.....	5

- Updated SN74AC32 operating temperature to 125°C and respective values in *Electrical Characteristics* table.6
- Updated SN74AC32 operating temperature to 125°C and respective values in *Switching Characteristics* tables..... 7

Changes from Revision E (July 2024) to Revision F (December 2024)	Page
• Corrected V_{IH} values in <i>Recommended Operating Conditions</i> table.....	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-87614012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87614012A SNJ54AC 32FK
5962-8761401CA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8761401CA SNJ54AC32J
5962-8761401DA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8761401DA SNJ54AC32W
SN74AC32BQAR	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC32
SN74AC32BQAR.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC32
SN74AC32D	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 85	AC32
SN74AC32DBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC32
SN74AC32DBR.A	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC32
SN74AC32DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC32
SN74AC32DR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC32
SN74AC32N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AC32N
SN74AC32N.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AC32N
SN74AC32NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC32
SN74AC32NSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC32
SN74AC32PW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 85	AC32
SN74AC32PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	AC32
SN74AC32PWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC32
SN74AC32PWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC32
SN74AC32PWRG4.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC32
SNJ54AC32FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87614012A SNJ54AC 32FK
SNJ54AC32FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87614012A SNJ54AC 32FK

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54AC32J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8761401CA SNJ54AC32J
SNJ54AC32J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8761401CA SNJ54AC32J
SNJ54AC32W	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8761401DA SNJ54AC32W
SNJ54AC32W.A	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8761401DA SNJ54AC32W

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AC32, SN74AC32 :

- Catalog : [SN74AC32](#)
- Automotive : [SN74AC32-Q1](#), [SN74AC32-Q1](#)
- Enhanced Product : [SN74AC32-EP](#), [SN74AC32-EP](#)
- Military : [SN54AC32](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC32BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AC32DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AC32DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AC32DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AC32NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AC32PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AC32PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC32BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AC32DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74AC32DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AC32DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AC32NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AC32PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AC32PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-87614012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8761401DA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AC32N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AC32N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AC32N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AC32N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AC32FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AC32FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AC32W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54AC32W.A	W	CFP	14	25	506.98	26.16	6220	NA

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

BQA 14

WQFN - 0.8 mm max height

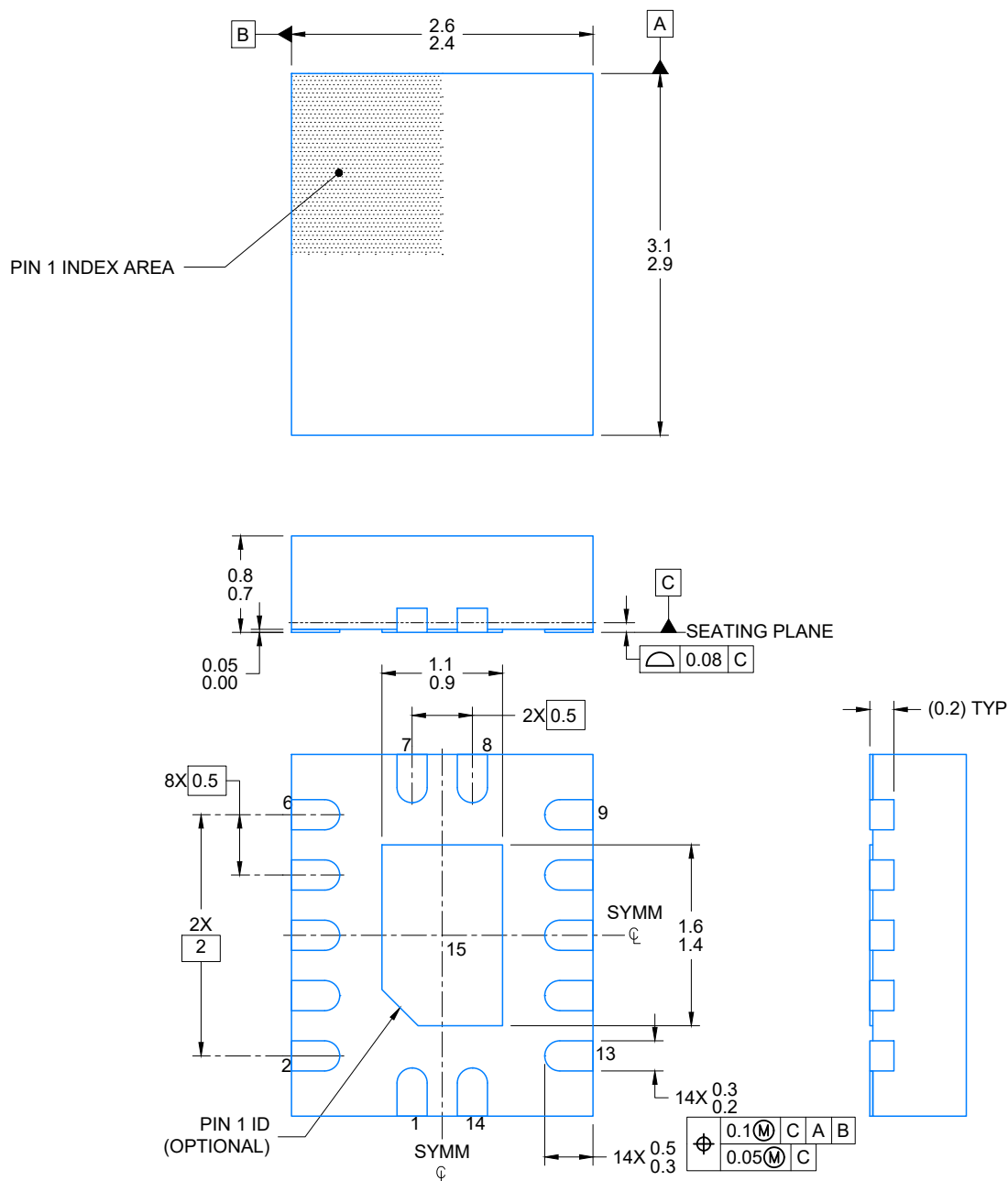
2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A



4224636/A 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

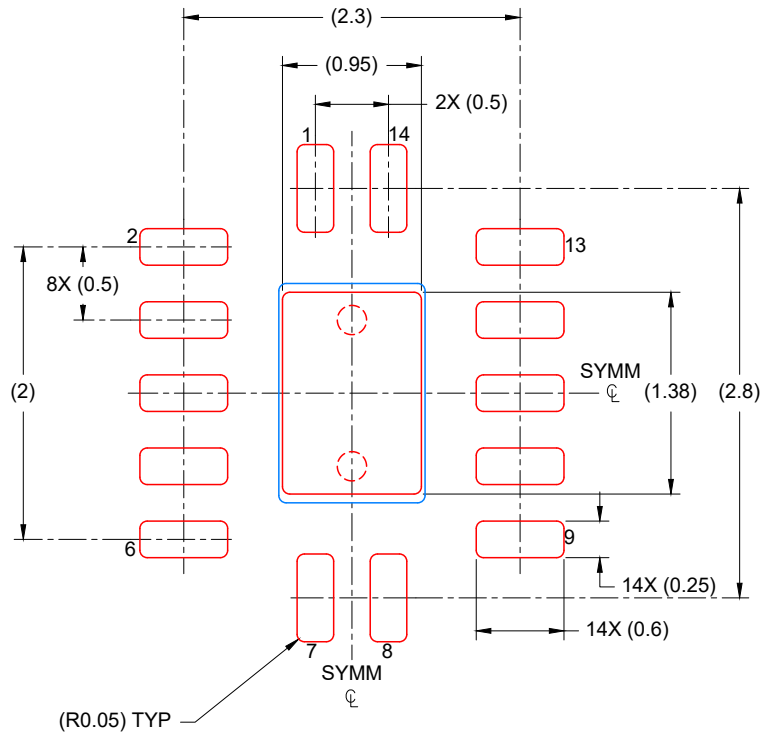
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



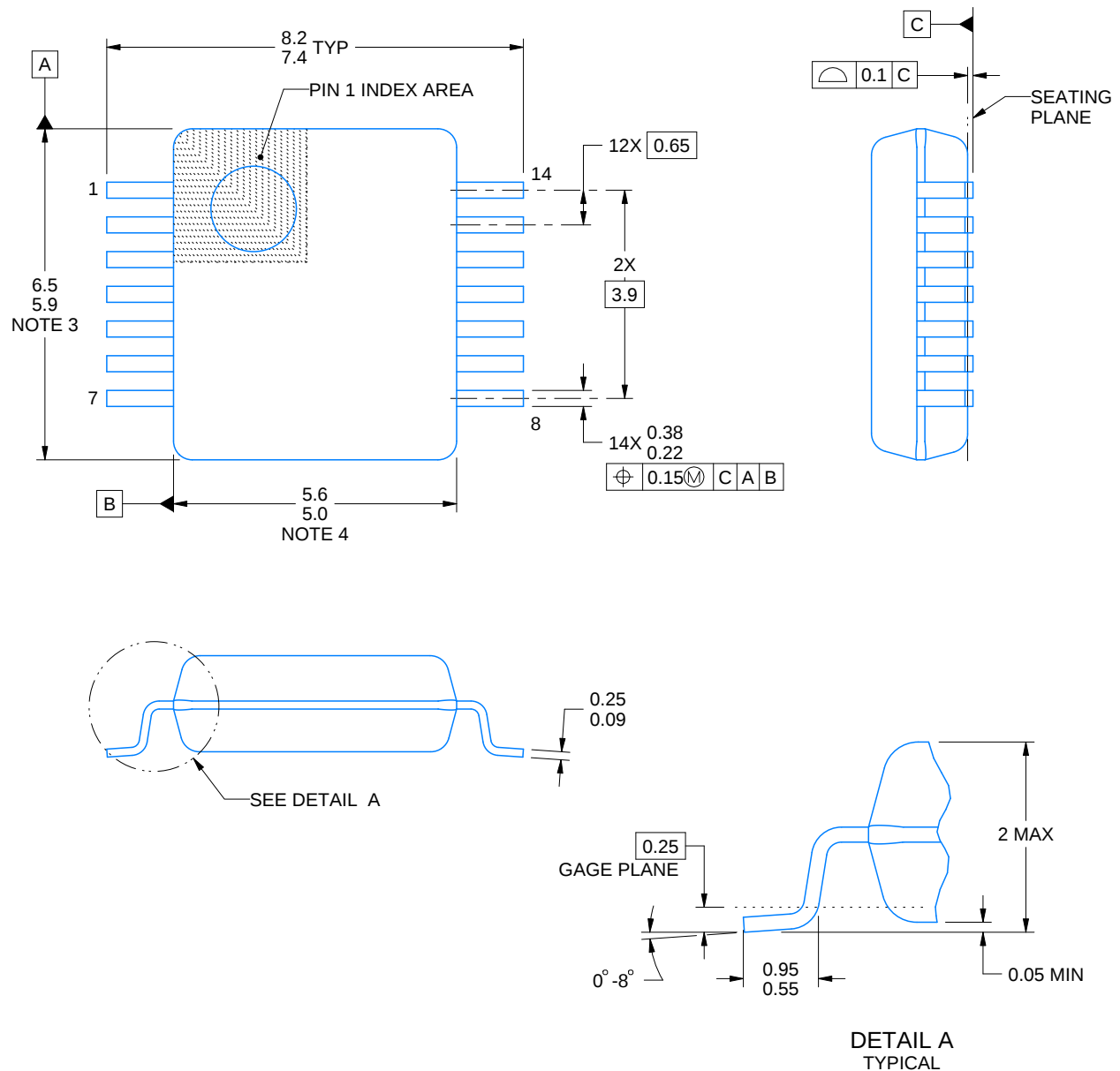
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F14



4220762/A 05/2024

NOTES:

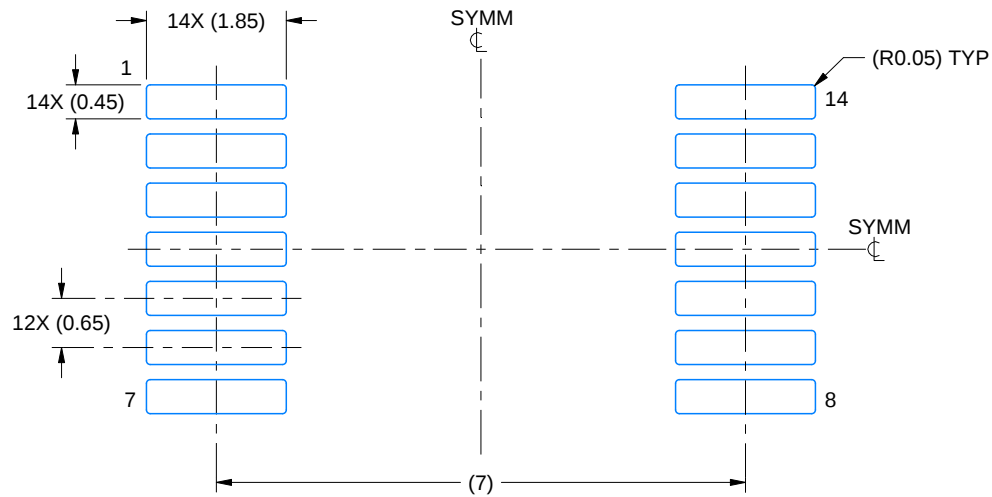
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

- Publication IPC-7351 may have alternate designs.
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW

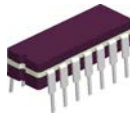
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

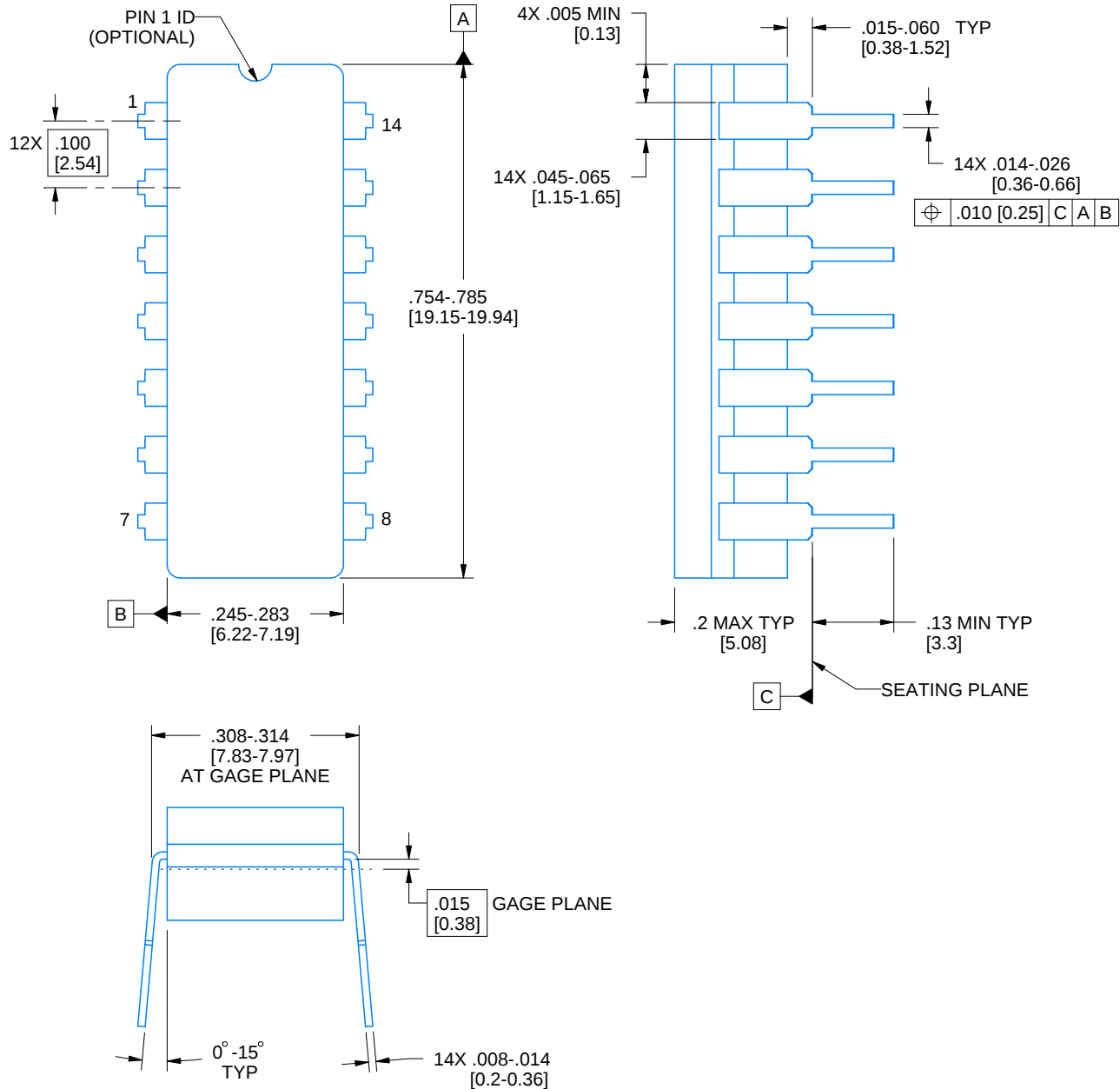


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

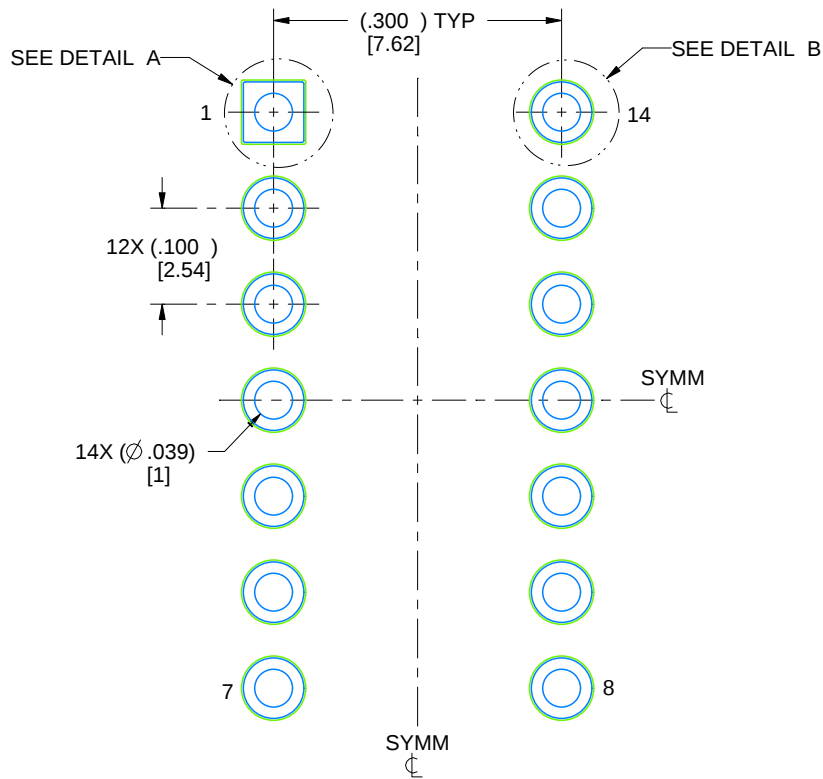
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

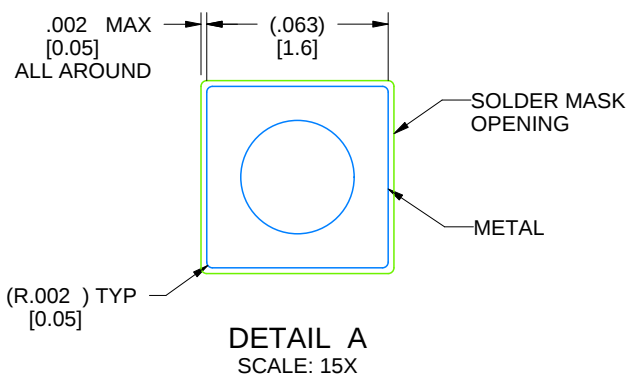
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

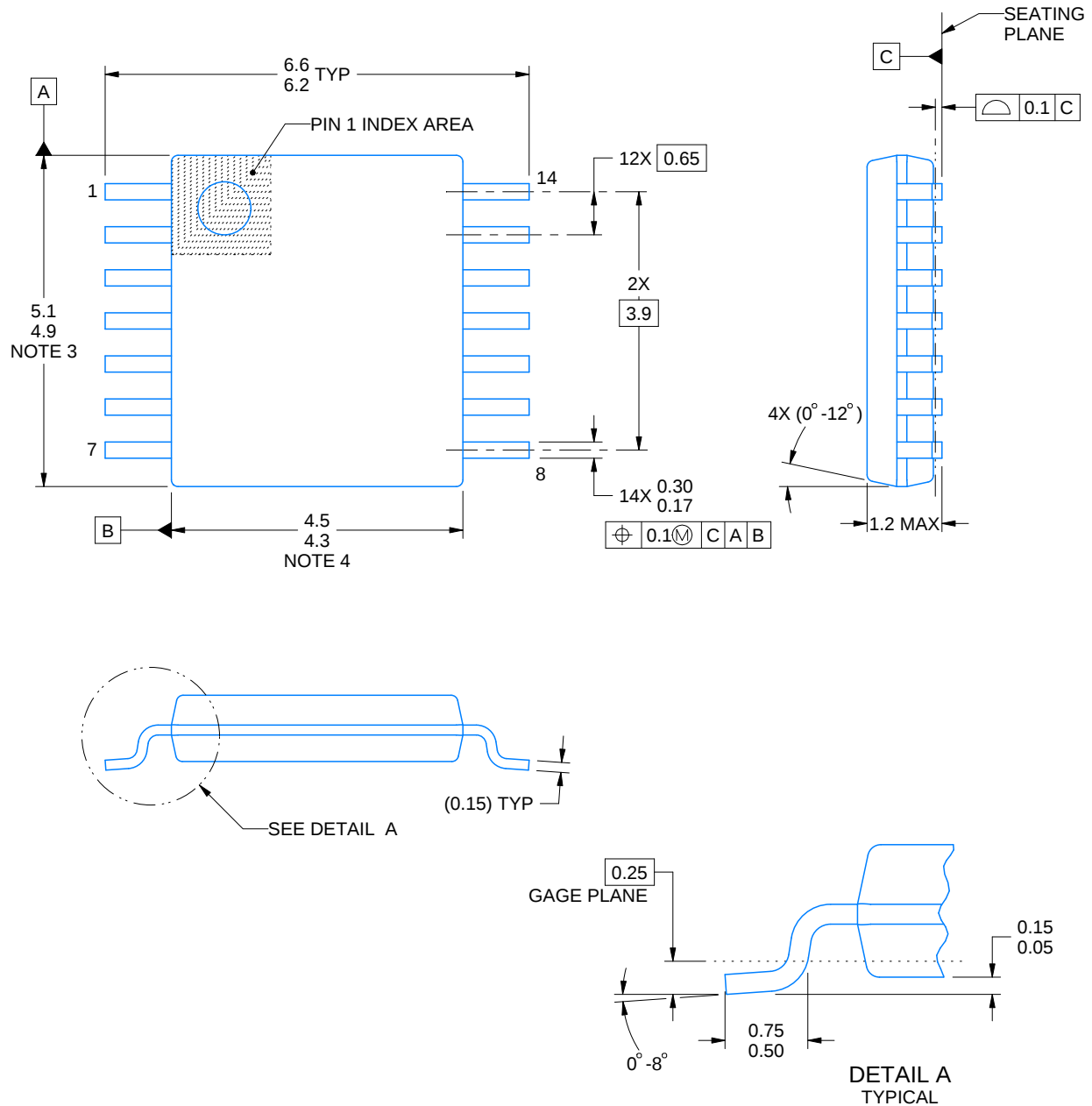
- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated