- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs (-32-mA I_{OH}, 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs

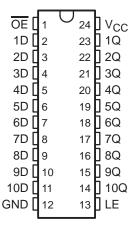
description

The SN54ABT841 and SN74ABT841A 10-bit latches are designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

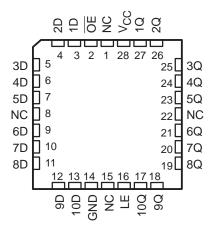
The ten transparent D-type latches provide true data at their outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

SN54ABT841 . . . JT OR W PACKAGE SN74ABT841A . . . DB, DW, NT, OR PW PACKAGE (TOP VIEW)



SN54ABT841 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

OE does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT841 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT841A is characterized for operation from –40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

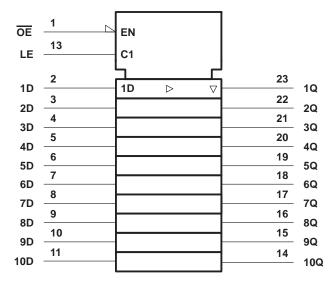
EPIC-IIB is a trademark of Texas Instruments Incorporated.



FUNCTION TABLE

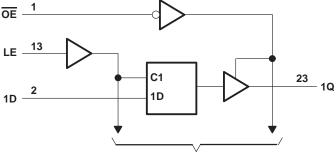
	INPUTS		OUTPUT
OE	LE	Q	
L	Н	Н	Н
L	Н	L	L
L	L	Χ	Q_0
Н	Χ	Χ	Z

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

logic diagram (positive logic)



To Seven Other Channels

Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.



SN54ABT841, SN74ABT841A 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS196D - FEBRUARY 1991 - REVISED MAY 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high or power-off state, VO	–0.5 V to 5.5 V
Current into any output in the low state, IO: SN54ABT841	96 mA
SN74ABT841A	128 mA
Input clamp current, I _{IK} (V _I < 0)	–18 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Package thermal impedance, θ _{JA} (see Note 2): DB package	104°C/W
DW package	81°C/W
NT package	67°C/W
PW package	120°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		SN54A	BT841	SN74AB	T841A	UNIT
		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
VI	Input voltage	0	VCC	0	VCC	V
IOH	High-level output current		-24		-32	mA
lOL	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		5		5	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



SN54ABT841, SN74ABT841A 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS196D - FEBRUARY 1991 - REVISED MAY 1997

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST COMPLE	TIONIC	Т	A = 25°C	;	SN54A	BT841	SN74AB	T841A	UNIT
PARAMETER	TEST CONDIT	IONS	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNII
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			-1.2		-1.2		-1.2	V
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.5			2.5		2.5		
V	$V_{CC} = 5 V$,	$I_{OH} = -3 \text{ mA}$	3			3		3		V
VOH	V _{CC} = 4.5 V	$I_{OH} = -24 \text{ mA}$	2			2				V
	VCC = 4.5 V	$I_{OH} = -32 \text{ mA}$	2*					2		
VOL	V _{CC} = 4.5 V	$I_{OL} = 48 \text{ mA}$			0.55		0.55			V
VOL	VCC = 4.5 V	$I_{OL} = 64 \text{ mA}$			0.55*				0.55	V
V _{hys}				100						mV
lį	$V_{CC} = 0 \text{ to } 5.5 \text{ V},$	$V_I = V_{CC}$ or GND			±1		±1		±1	μΑ
lozpu‡	$V_{CC} = 0$ to 2.1 V, $V_{O} = 0.5$ V t	to 2.7 V, $\overline{\sf OE}$ = X			±50		±50		±50	μΑ
lozpd [‡]	$V_{CC} = 2.1 \text{ V to } 0, V_{O} = 0.5 \text{ V}$	to 2.7 V, OE = X			±50		±50		±50	μΑ
lozh	$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V}, V_{O} = 2.7 \text{ V}$	7 V, OE ≥ 2 V			10		10		10	μΑ
lozL	$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V}, V_{O} = 0.9$	5 V, OE ≥ 2 V			-10		-10		-10	μΑ
l _{off}	$V_{CC} = 0$,	V_I or $V_O \le 4.5 \text{ V}$			±100				±100	μΑ
ICEX	$V_{CC} = 5.5 \text{ V}, V_{O} = 5.5 \text{ V}$	Outputs high			50		50		50	μΑ
IO§	V _{CC} = 5.5 V,	V _O = 2.5 V	-50	-140	-180	-50	-180	-50	-180	mA
		Outputs high		1**	250**		280		250	μΑ
Icc	$V_{CC} = 5.5 \text{ V}, I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low		24**	38¶**		45¶		38¶	mA
	1 - 1 CC 01 011B	Outputs disabled		0.5**	250**		280		250	μΑ
	V _{CC} = 5.5 V,	Outputs enabled			1.5		1.5		1.5	mA
∆lcc#	One input at 3.4 V,	Outputs disabled			250**		280		250	μΑ
	Other inputs at V _{CC} or GND	Control inputs			1.5		1.5		1.5	mA
C _i	V _I = 2.5 V or 0.5 V			4						pF
Co	V _O = 2.5 V or 0.5 V			7						pF

^{*} On products compliant to MIL-PRF-38535, this parameter does not apply.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

					SN54ABT841		SN74ABT841A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE high or low		3.3		3.3		3.3		ns
	Setup time, data before LE↓	High	2.5		2.5		2.5		no
t _{su}	Setup time, data before LEV	Low	1.5		1.5		1.5		ns
Ţ.	Hold time, data after LE↓	High	1.5		1.5		1.5		ns
t _h	Floid time, data after LLV	Low	1.5		2		1.5		115



^{**} These limits apply only to the SN74ABT841A.

[†] All typical values are at $V_{CC} = 5 \text{ V}$.

[‡] This parameter is characterized, but not production tested.

[§] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[¶] This limit may vary among suppliers.

[#]This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

				SN	54ABT8	41		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _C	C = 5 V \ = 25°C	<u>'</u> ,	MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	D	Q	1†	4.1	5.5	1†	6.8	ns
^t PHL	Б	ų ,	1.5†	4	5.5	1.5†	6.8	115
t _{PLH}	LE	Q	1.6†	4.1	6.6†	1.6†	7.4	nc
t _{PHL}	LE	L Q	2†	4.6	6.2	2†	6.8	ns
^t PZH	ŌĒ	Q	1	3	4.9†	1	5.8	no
tPZL	OE	<u> </u>	2.2	4.1	5.7	2.2	6.5	ns
^t PHZ	ŌĒ	Q	2†	4.7	6.2	2†	7.2	ns
t _{PLZ}	OE .		1.5†	4.6	6.1	1.5†	6.6	115

[†] This data sheet limit may vary among suppliers.

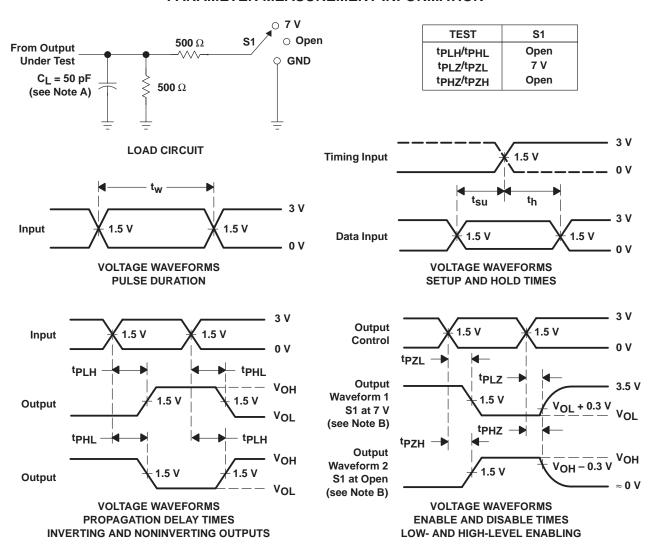
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V ₍	CC = 5 V 4 = 25°C	/, ;	MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	D	Q	1.4†	4.1	5.5	1.4†	6.2†	ns
t _{PHL}	U	Q	1.5†	4	5.5	1.5†	6.2	113
t _{PLH}	LE	Q	2.1†	4.1	5.9†	2.1†	6.5†	ns
^t PHL	LL	Q .	2.4†	4.6	6.2	2.4†	6.7	115
^t PZH	ŌĒ	Q	1	3	4.7	1	5.3†	20
tPZL	OE	Q	2.2	4.1	5.7	2.2	6.3†	ns
^t PHZ	ŌĒ	Q	2.6†	4.7	6.2	2.6†	7.1	ns
^t PLZ	OE	Q	1.9†	4.6	6.1	1.9†	6.5	115

[†]This data sheet limit may vary among suppliers.



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{Q} = 50 Ω , t_{f} \leq 2.5 ns, t_{f} \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9676901QLA	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9676901QL A SNJ54ABT841JT
SN74ABT841ADBR	Active	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB841A
SN74ABT841ADBR.B	Active	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB841A
SN74ABT841ADBRE4	Active	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB841A
SN74ABT841ADW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT841A
SN74ABT841ADW.B	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT841A
SN74ABT841ADWG4	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT841A
SN74ABT841ADWR	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT841A
SN74ABT841ADWR.B	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT841A
SN74ABT841APW	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB841A
SN74ABT841APW.B	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB841A
SN74ABT841APWR	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB841A
SN74ABT841APWR.B	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB841A
SNJ54ABT841JT	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9676901QL A SNJ54ABT841JT

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.



PACKAGE OPTION ADDENDUM

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT841ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74ABT841ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74ABT841APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

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*All dimensions are nominal

Device	Package Type Package Drawing		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT841ADBR	SSOP	DB	24	2000	353.0	353.0	32.0
SN74ABT841ADWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74ABT841APWR	TSSOP	PW	24	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ABT841ADW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ABT841ADW.B	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ABT841ADWG4	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ABT841APW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74ABT841APW.B	PW	TSSOP	24	60	530	10.2	3600	3.5

JT (R-GDIP-T**)

24 LEADS SHOWN

CERAMIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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