# SN54121, SN74121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

MAY 1983 - REVISED MARCH 1988

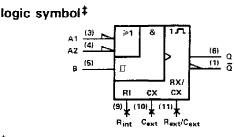
- Programmable Output Pulse Width
  With R<sub>int</sub>...35 ns Typ
  With R<sub>ext</sub>/C<sub>ext</sub>...40 ns to 28 Seconds
- Internal Compensation for Virtual Temperature Independence
- Jitter-Free Operation up to 90% Duty Cycle
- Inhibit Capability

	N PACKAGE OP VIEW)
Q   1 NC   2 A1   3 A2   4 B   5 Q   6 GND   7	14 VCC 13 NC 12 NC 11 Rext/Cext 10 Cext 9 Rint 8 NC

SN54121 . . . J OR W PACKAGE

NC - No internal connection.

### **FUNCTION TABLE** INPUTS OUTPUTS Q ō A1 Δ2 В I L × н L Lt нt Х L H Lt нt х х L LŤ x Ηt н н Ш н ч i н L 1 1 х $\Box$ ٦



<sup>‡</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

For explanation of function table symbols, see page

† These lines of the function table assume that the indicated steady-state conditions at the A and B inputs have been setup long enough to complete any pulse started before the setup.

### description

These multivibrators feature dual negative-transition-triggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to VCC noise of typically 1.5 volts is also provided by internal latching circuitry.

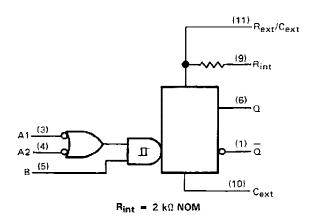
Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R<sub>int</sub> connected to V<sub>CC</sub>, C<sub>ext</sub> and R<sub>ext</sub>/C<sub>ext</sub> open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of  $V_{CC}$  and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and VCC ranges for more than six decades of timing capacitance (10 pF to 10  $\mu$ F) and more than one decade of timing resistance (2 k $\Omega$  to 30 k $\Omega$  for the SN54121 and 2 k $\Omega$  to 40 k $\Omega$  for the SN74121). Throughout these ranges, pulse width is defined by the relationship  $t_{W(out)} = C_{ext}RT_{10} \approx 0.7 C_{ext}R_{10}$ . In circuits where pulse cutoff is not critical, timing capacitance up to 1000  $\mu$ F and timing resistance as low as 1.4 k $\Omega$  may be used. Also, the range of jitter-free output pulse widths is extended if VCC is held to 5 volts and free-air temperature is 25 °C. Duty cycles as high as 90% are achieved when using maximum recommended RT'. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.



# logic diagram (positive logic)

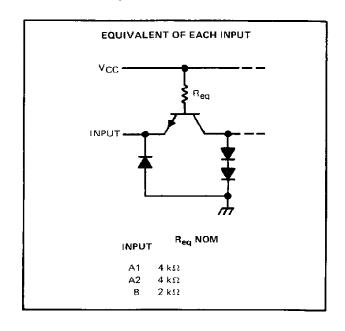


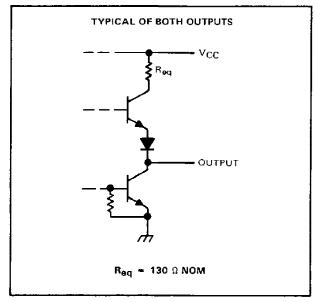
Pin numbers shown on logic notation are for J or N packages.

NOTES: 1. An external capacitor may be connected between  $C_{ext}$  (positive) and  $R_{ext}/C_{ext}$ .

2. To use the internal timing resistor, connect  $R_{int}$  to  $V_{CC}$ . For improved pulse width accuracy and repeatability, connect an external resistor between  $R_{ext}/C_{ext}$  and  $V_{CC}$ with Rint open-circuited.

# schematics of inputs and outputs





# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 3)	/
Input voltage	/
Operating free-air temperature range: SN5412155°C to 125°C	2
SN74121	2
Storage temperature range65°C to 150°C	3

NOTE 3: Voltage values are with respect to network ground terminal.

# recommended operating conditions

				MIN	NOM	MAX	UNIT	
Vcc	Supply voltage		54 Family	4.5	5	5.5	v	
*	Supply voltage		74 Family	4.75	5	5.25	\ \ \	
ЮН	High-level output current	High-level output current				-0.4	mA	
JOL	Low-level output current					16	mA	
dv/dt Rate of rise or fall of input pulse		Schmitt input, B		1			V/s	
uv/ut	Rate of rise or fall of input pulse	Logic inputs, A1, A2		1			V/μs	
tw(in)	input pulse width		<del></del>	50			ns	
R <sub>ext</sub>	External timing capacitance	54 Family		1.4		30		
''ext	External timing capacitance		74 Family	1.4		40	kΩ	
C <sub>ext</sub>	External timing capacitance			0		1000	μF	
	Duty cycle	$R_T = 2 k\Omega$				67		
	Daty Cycle	R <sub>T</sub> = MAX R <sub>ext</sub>				90	%	
T. Operati	Operating free-air temperature			- 55		125		
TA	Operating mee-air temperature		74 Family	0		70	оC	

# SN54121, SN74121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

# electrical characteristics over recommended operating free-air temperature range (unless otherwise

	PARAMETER	TEST CO	NDITONS <sup>†</sup>	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage at B input	V <sub>CC</sub> = MIN		2			V
VIL	Low-level input voltage at A input	V <sub>CC</sub> - MIN				0.8	ν
V <sub>T+</sub>	Positive-going threshold voltage at B input	VCC = MIN		1	1.55	2	V
VT_	Negative-going threshold voltage at B input	VCC = MIN		0.8	1.35		٧
Vik	Input clamp voltage	V <sub>CC</sub> = MIN,	I <sub>f</sub> = -12 mA			- 1.5	٧
ЮН	High-level output voltage	VCC = MIN,	IOH = MAX	2.4	3.4		٧
Vol	Low-level output voltage	VCC = MIN,	IOL = MAX		0.2	0.4	V
ΙĮ	Input current at maximum input voltage	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 5.5 V			1	mÅ
1	High land in the surrent	V <sub>CC</sub> = MAX,	A1 or A2			40	
۱Н	High-level input current	V <sub>1</sub> - 2.4 V	В			80	μА
		VCC = MAX,	A1 or A2			- 1.6	4
IIL	Low-level input current	V <sub>I</sub> = 0.4 V	В			- 3.2	mA
	ξ	14 444.94	54 Family	- 20		- 55	
os	Short-circuit output current <sup>§</sup>	V <sub>CC</sub> = MAX	74 Family	- 18		- 55	mA
1	C In accordant	U MAY	Quiescent		13	25	^
ICC	Supply current	V <sub>CC</sub> = MAX	Triggered		23	40	mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25 \,^{\circ}\text{C}$

	PARAMETER	TEST CON	IDITIONS	MIN	TYP	MAX	UNIT
<sup>t</sup> PLH	Propagation delay time, low-to-high- level Q output from either A input				45	70	ns
tpLH	Propagation delay time, low-to-high- level Ω output from B input	C <sub>ext</sub> = 80 pF,			35	55	ns
tPHL	Propagation delay time, high-to-low level Q output from either A input	C <sub>I</sub> = 15 pF,	R <sub>int</sub> to V <sub>CC</sub>		50	80	пŝ
<sup>†</sup> PHL	Propagation delay time, high-to-low level $\overline{\Omega}$ output from 8 input	$R_L = 400 \Omega$ , See Note 4			40	65	ns
tw(out)	Pulse width obtained using internal timing resistor		C <sub>ext</sub> = 80 pF, R <sub>int</sub> to V <sub>CC</sub>	70	110	150	ns
tw(out)	Pulse width obtained with zero timing capacitance		C <sub>ext</sub> = 0, R <sub>int</sub> to V <sub>CC</sub>		30	50	ns
	Pulse width obtained using		$C_{\text{ext}} = 100 \text{ pF},$ $R_{\text{T}} = 10 \text{ k}\Omega$	600	700	800	ns
<sup>t</sup> w(out)	external timing resistor		$C_{\text{ext}} = 1 \mu\text{F},$ $R_{\text{T}} = 10 \text{k}\Omega$	6	7	8	ms

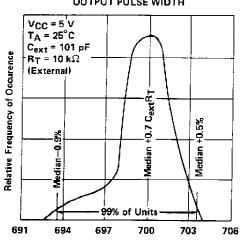
NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

 $<sup>^{\</sup>ddagger}$ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25 °C.  $^{\dagger}$ Not more than one output should be shorted at a time.

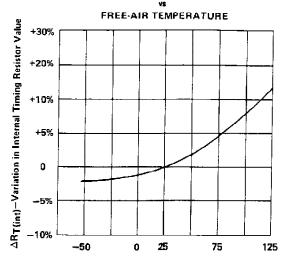
### TYPICAL CHARACTERISTICS<sup>†</sup>

# DISTRIBUTION OF UNITS

OUTPUT PULSE WIDTH



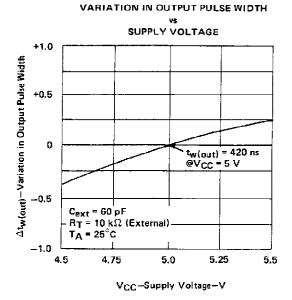
# VARIATION IN INTERNAL TIMING RESISTOR VALUE



TA-Free-Air Temperature-°C

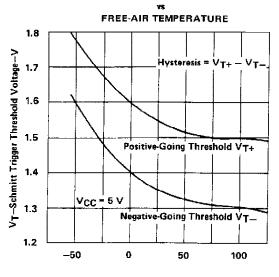
### FIGURE 1

tw(out)-Output Pulse Width-ns



### FIGURE 2

SCHMITT TRIGGER THRESHOLD VOLTAGE



TA-Free-Air Temperature-°C

FIGURE 3

FIGURE 4

<sup>†</sup>Data for temperatures below 0°C and above 70°C are applicable for SN54121.



# TYPICAL CHARACTERISTICS<sup>†</sup> (continued)

10 ns

# VARIATION IN OUTPUT PULSE WIDTH vs FREE-AIR TEMPERATURE 1.0% VCC = 5 V VCC = 5 V CT = 60 pF RT = 10 kΩ Tw/out) = 420 ns © TA = 25°C

TIMING RESISTOR VALUE

10 ms

1 ms

1 ms

Coxt 1 ms

Coxt 1 ms

100 ms

Coxt 1 000 pr

100 ns

VCC = 6 V Coxt 10 pr

**OUTPUT PULSE WIDTH** 

R<sub>T</sub>-Timing Resistor Value- $k\Omega$ 

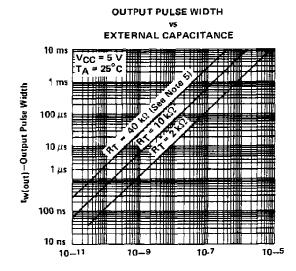
TA-Free-Air Temperature-°C

FIGURE 5

FIGURE 6

10

100



Cext —Timing Capacitance—F

### FIGURE 7

NOTE 5: These values of resistance exceed the maximum recommended use over the full temperature range of the SN54121. †Data for temperatures below 0 °C and above 70 °C are applicable for SN54121.

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# PACKAGE OPTION ADDENDUM



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# **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9755301QCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
5962-9755301QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
5962-9755301QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SN54121J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SN54121J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SN74121D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74121D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74121DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74121DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74121N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74121N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74121N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74121N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74121NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74121NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SNJ54121J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54121J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54121W	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54121W	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54121WA	ACTIVE	CFP	WA	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54121WA	ACTIVE	CFP	WA	14	1	TBD	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



# PACKAGE OPTION ADDENDUM

23-Apr-2005

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# 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# W (R-GDFP-F14)

# CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

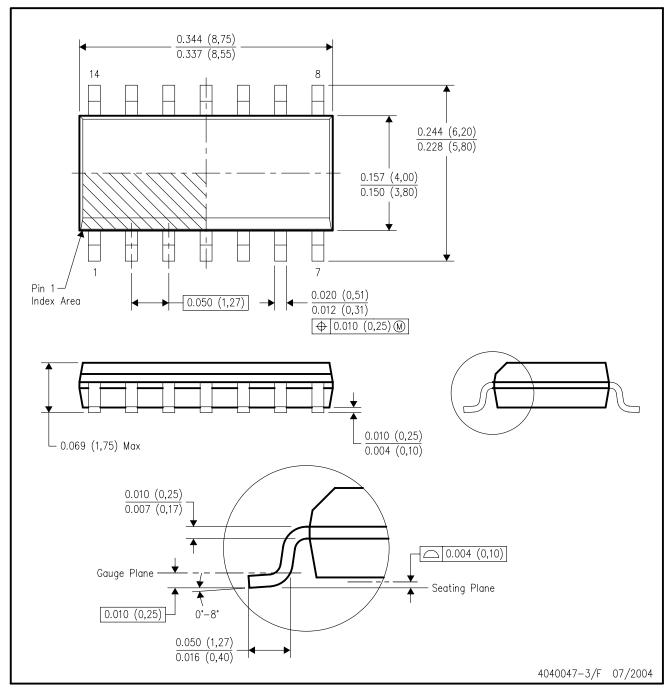


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



# D (R-PDSO-G14)

# PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012 variation AB.



# **MECHANICAL DATA**

# NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

# PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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11-Nov-2025

# **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9755301QCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9755301QC A SNJ54121J
5962-9755301QDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9755301QD A SNJ54121W
SN54121J	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54121J
SN54121J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54121J
SN74121D	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74121
SN74121D.A	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74121
SN74121DE4	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74121
SN74121N	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74121N
SN74121N.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74121N
SNJ54121J	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9755301QC A SNJ54121J
SNJ54121J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9755301QC A SNJ54121J
SNJ54121W	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9755301QD A SNJ54121W
SNJ54121W.A	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9755301QD A SNJ54121W

<sup>(1)</sup> **Status:** For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

# PACKAGE OPTION ADDENDUM

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(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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### OTHER QUALIFIED VERSIONS OF SN54121, SN74121:

Catalog: SN74121

Military: SN54121

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

Military - QML certified for Military and Defense Applications

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 23-May-2025

# **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9755301QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74121D	D	SOIC	14	50	506.6	8	3940	4.32
SN74121D.A	D	SOIC	14	50	506.6	8	3940	4.32
SN74121DE4	D	SOIC	14	50	506.6	8	3940	4.32
SN74121N	N	PDIP	14	25	506	13.97	11230	4.32
SN74121N	N	PDIP	14	25	506	13.97	11230	4.32
SN74121N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74121N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54121W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54121W.A	W	CFP	14	25	506.98	26.16	6220	NA



SMALL OUTLINE INTEGRATED CIRCUIT



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



# W (R-GDFP-F14)

# CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14



CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4040083-5/G





CERAMIC DUAL IN LINE PACKAGE



- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
   Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
   Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE



# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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