

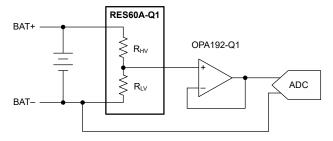
RES60A-Q1 Automotive, 1400V_{DC}, Precision Resistive Divider

1 Features

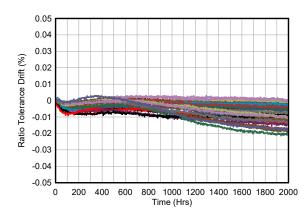
- AEC-Q200 qualified for automotive applications:
 - Temperature grade 1: –40°C to +125°C
- High voltage rating:
 - Survives 3+ HiPOT tests at 4000V_{DC} (60s)
 - 1700V_{DC} creepage and clearance support between HVIN and LVIN (IEC-61010 PD 2)
- High dc precision with low shift and drift:
 - Initial ratio matching precision: ±0.1% (max)
 - Low drift: ±1ppm/°C (typ)
 - Accurate ±0.2% across aging and temperature
- · Low thermal noise thin-film resistors

2 Applications

- High-voltage bus and battery voltage monitoring
 - HEV/EV battery management system (BMS)
 - HEV/EV DC/DC converter
 - HEV/EV onboard charger (OBC)
 - HEV/EV inverter and motor control
- · Nonisolated, same-ground, always-on dividers
- High common-mode range amplifiers



Typical Schematic



Long-term Drift Data (RES60A100, n=37 units)

3 Description

The RES60A-Q1 is a matched resistive divider, implemented in thin-film SiCr with Texas Instruments' modern, high-performance, analog wafer process. A high quality SiO_2 insulative layer encapsulates the resistors and enables usage at extremely high voltages, up to 1400V_{DC} for sustained operation or 4000V_{DC} for HiPOT testing (60s). The device has a nominal input resistance of R_{HV} = $12.5\text{M}\Omega$, and is available in several nominal ratios to meet a wide array of system needs.

The RES60A-Q1 series features high ratio matching precision, with the measured ratio of each divider within $\pm 0.1\%$ (max) of the nominal. This precision is maintained over the specified temperature range and aging, with a cumulative drift of only $\pm 0.2\%$ (max). Therefore, the lifetime tolerance of an uncalibrated RES60A-Q1 remains within a $\pm 0.3\%$ (max) envelope.

The RES60A-Q1 is automotive qualified under AEC-Q200 temperature grade 1, with a specified temperature range from –40°C to +125°C. The device is offered in an 8-pin SOIC package, with nominal body size 7.5mm × 5.85mm, and features creepage and clearance distances of at least 8.5mm between the high-voltage and low-voltage pins.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
RES60A-Q1	DWV (SOIC, 8)	5.85mm × 11.5mm

- (1) For more information, see Section 10.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

PART NUMBER	NOMINAL RATIO (R _{HV} :R _{LV})
RES60A145-Q1	145:1
RES60A210-Q1	210:1
RES60A315-Q1	315:1
RES60A410-Q1	410:1
RES60A500-Q1	500:1
RES60A610-Q1	610:1
RES60A100-Q1	1000:1



Table of Contents

1 Features1	7 Application and Implementation	. 10
2 Applications1	7.1 Application Information	. 10
3 Description1	7.2 Typical Application	. 13
4 Pin Configuration and Functions2	7.3 Power Supply Recommendations	
5 Specifications3	7.4 Layout	. 15
5.1 Absolute Maximum Ratings3	8 Device and Documentation Support	
5.2 ESD Ratings3	8.1 Device Support	. 17
5.3 Recommended Operating Conditions4	8.2 Documentation Support	. 18
5.4 Thermal Information4	8.3 Receiving Notification of Documentation Updates	18
5.5 Electrical Characteristics5	8.4 Support Resources	
5.6 Typical Characteristics7	8.5 Trademarks	
6 Detailed Description8	8.6 Electrostatic Discharge Caution	18
6.1 Overview8	8.7 Glossary	
6.2 Functional Block Diagram8	9 Revision History	
6.3 Feature Description8	10 Mechanical, Packaging, and Orderable	
6.4 Device Functional Modes9	Information	. 19

4 Pin Configuration and Functions

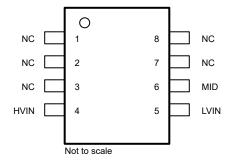


Figure 4-1. DWV Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions

	PIN	TYPE	DESCRIPTION
NAME	NO.	ITPE	DESCRIPTION
HVIN	4	Input	High-voltage input of divider
LVIN	5	Input	Low-voltage input of divider
MID	6	Output	Center tap of divider
NC	1, 2, 3	_	Noninternally-connected pins on high-voltage side. Solder to the PCB for best board-level reliability. The exposed metal area of these pins must be considered as part of any creepage and clearance calculations.
NC	7, 8	_	Noninternally-connected pins on low-voltage side. Solder to the PCB for best board-level reliability. The exposed metal area of these pins must be considered as part of any creepage and clearance calculations.

Submit Document Feedback



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
		RES60A145	-2700	2700	
	Maximum short-term overload voltage per divider, V _D = V _{HVIN} – V _{A, m. (100ms, T_A = 25°C)(2) (3)}	RES60A210	-2700	2700	
		RES60A315	-2700	2700	V
		RES60A410	-2700	2700	
		RES60A500	-2700	2700	
		RES60A610	-2700	2700	
		RES60A100	-2700	2700	
		RES60A145	-3000	3000	
		RES60A210	-3000	3000	
	Transient high-potential voltage, ac (50Hz, T _A = 25°C) ^{(4) (5)}	RES60A315	-3000	3000	V_{RMS}
		RES60A410	-3000	3000	
		RES60A500	-3000	3000	
		RES60A610	-3000	3000	
		RES60A100	-3000	3000	
		RES60A145	-4000	4000	
		RES60A210	-4000	4000	
		RES60A315	-4000	4000	
	Transient high-potential voltage, dc $(T_A = 25^{\circ}C)^{(4)}$ (5)	RES60A410	-4000	4000	V_{DC}
	(14 25 5)	RES60A500	-4000	4000	
		RES60A610	-4000	4000	
		RES60A100	-4000	4000	
T _A	Ambient temperature		-55	150	°C
TJ	Junction temperature		-55	150	°C
T _{stg}	Storage temperature		-55	175	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Maximum short-term voltage permitted under transient conditions without performance degradation. Avoid sustained operation at or beyond these voltage levels, especially if the resulting self-heating causes T_J to exceed 150°C.
- (3) Tested in production, with ±2.7kV stress for 100ms, on each device.
- (4) Differential voltage from high-voltage domain (pins 1-4) to low-voltage domain (pins 5-8) of the package.
- (5) Total stress duration of 180s, accumulated over lifetime in increments of no longer than 60s periods, with duty cycle ≤ 20%. For example, after 60s of continuous stress, wait 240s for device temperature to settle before repeating the stress. Repeated transient high-potential voltage testing can lead to performance degradation or device damage.

5.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per AEC Q200-002, all pins except 5 and 6	±4000	
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q200-002, pins 5 and 6	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1500	



5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM MAX	UNIT
		RES60A145	-1400	1400	
	F	RES60A210	-1400	1400	
		RES60A315	-1400	1400	
	Maximum sustained dc voltage per divider (HVIN pin to LVIN pin, 10 years at $T_A = 25^{\circ}\text{C})^{(1)}$	RES60A410	-1400	1400	V_{DC}
	ZVIIV piii, 10 youro ut 1 _A 20 0)	RES60A500	-1400	1400	
		RES60A610	-1400	1400	
		RES60A100	-1400	1400	
		RES60A145	-550	550	
		RES60A210	-550	550	
		RES60A315	-550	550	
	Maximum sustained 50Hz ac voltage per divider (HVIN pin to LVIN pin, 10 years at $T_A = 25^{\circ}\text{C}$) ⁽¹⁾	RES60A410	-550	550	V _{RMS}
	to Evily pill, To years at TA = 23 G/V	RES60A500	-550	550	
		RES60A610	-550	550	
		RES60A100	-550	550	
T _A	Ambient temperature	1	-40	125	°C

⁽¹⁾ Assumes $R_{\theta JA} = 110.4$ °C/W.

5.4 Thermal Information

		RES60A-Q1	
	THERMAL METRIC(1)	DWV (SOIC)	UNIT
		8 PINS	
R _{0JA}	Junction-to-ambient thermal resistance	110.4	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	55.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	53.0	°C/W
ΨЈТ	Junction-to-top characterization parameter	41.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	51.6	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Submit Document Feedback



5.5 Electrical Characteristics

at V_D = 1000V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN TYP	MAX	UNIT
INITIAL I	RESISTANCE					
R _{HV}	Input resistance			12.5		ΜΩ
		RES60A145		86.2		
		RES60A210		59.5		
		RES60A315		39.7		
R_{LV}	Ratio-dependent resistance ⁽¹⁾	RES60A410		30.5		kΩ
		RES60A500		25.0		
		RES60A610		20.5		
		RES60A100		12.5		
			RES60A145	145		
			RES60A210	210		
			RES60A315	315		
G_{nom}	Nominal ratio	R _{HV} / R _{LV}	RES60A410	410		
			RES60A500	500		
			RES60A610	610		
			RES60A100	1000		
			RES60A145	±0.02	±0.1	
			RES60A210	±0.02	±0.1	
			RES60A315	±0.02	±0.1	
t_D	Initial ratio tolerance ⁽²⁾	$V_D = 250V \text{ to } V_D = 1000V,$ $(R_{HV} / R_{LV}) / G_{nom} - 1^{(3)}$	RES60A410	±0.02	±0.1	%
		(THV / TLV / Onom	RES60A500	±0.02	±0.1	
			RES60A610	±0.02	±0.1	
			RES60A100	±0.02	±0.1	
t _{abs}	Absolute tolerance (per resistor) ⁽⁵⁾	$(R_x / R_{xnom}) - 1^{(3)}$			±15	%
RESISTA	ANCE DRIFT					
	Ratio tolerance drift across operating lifetime ⁽⁴⁾	10 years continuous, T _A = - V _D = 1000V, (G _{INITIAL} – G _{FI}	–40°C to +85°C, _{INAL}) / G _{INITIAL} ⁽³⁾		±0.2	%
TCR _{abs}	Absolute temperature coefficient of resistance (per resistor) ⁽⁵⁾ (6)	$(\Delta R_x / R_{x(25^{\circ}C)}) / \Delta T_A$, $T_A = -40^{\circ}C$ to +125°C		±23		ppm/°C
TCD	Divider temperature coefficient of	ivider temperature coefficient of $\Delta t_D / \Delta T_A$, $T_A = -40$ °C to		±1	±5	nnm/°C
TCR _{ratio}	resistance (per divider) ^{(2) (6)}	$\Delta t_D / \Delta T_A$, $T_A = -40^{\circ}$ C to +	125°C	±1	±5	ppm/°C
VCP	Absolute voltage coefficient of	$\Delta R_x / \Delta V_{Rx}$, $V_D = 100V$ to	R _{HV}	±3.7		Ω/V
VCR _{abs}	resistance (per resistor) ⁽⁵⁾ (6)	$V_D = 1000V$	R _{LV}	±2.9		12/ V
VCR _{ratio}	Divider voltage coefficient of resistance (per divider) ⁽²⁾ (6)	$\Delta t_D / \Delta V_D$, $V_D = 100 V$ to V_D) = 1000V	±0.3		ppm/V



5.5 Electrical Characteristics (continued)

at V_D = 1000V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST COND	TEST CONDITIONS		MAX	UNIT
IMPED	ANCE					
		HVIN, V _{LVIN} = V _{MID} = 0V	$HVIN$, $V_{LVIN} = V_{MID} = 0V$			
C _{IN}	Pin capacitance ⁽⁶⁾ (7)	MID, V _{LVIN} = V _{HIN} = 0V		1.12		pF
		LVIN, V _{MID} = V _{HIN} = 0V		2.66		
			RES60A145	68.5		
			RES60A210	72.9		
			RES60A315	77.3		
	–3dB bandwidth ⁽⁶⁾ (8)	Normalized to attenuation at f = 100Hz, no C _{FILTER}	RES60A410	71.7		kHz
		att 1001.12, 110 OFILIER	RES60A500	74.9		
			RES60A610	73.8		
			RES60A100	73.7		
			RES60A145	TBD		
			RES60A210	TBD		μs
			RES60A315	TBD		
		To 1%, 10V step	RES60A410	TBD		
			RES60A500	TBD		
			RES60A610	TBD		
	Settling time ⁽⁶⁾		RES60A100	TBD		
t _s	Settling time(*)		RES60A145	TBD		
			RES60A210	TBD		
			RES60A315	TBD		
		To 0.1%, 10V step	RES60A410	TBD		μs
			RES60A500	TBD		
			RES60A610	TBD		
			RES60A100	TBD		
			RES60A145	36		
			RES60A210	30		
			RES60A315	25		
e _N	Thermal noise density ⁽⁷⁾	f = 1kHz	RES60A410	22		nV/√Hz
			RES60A500	20		
			RES60A610	18		
			RES60A100	14		

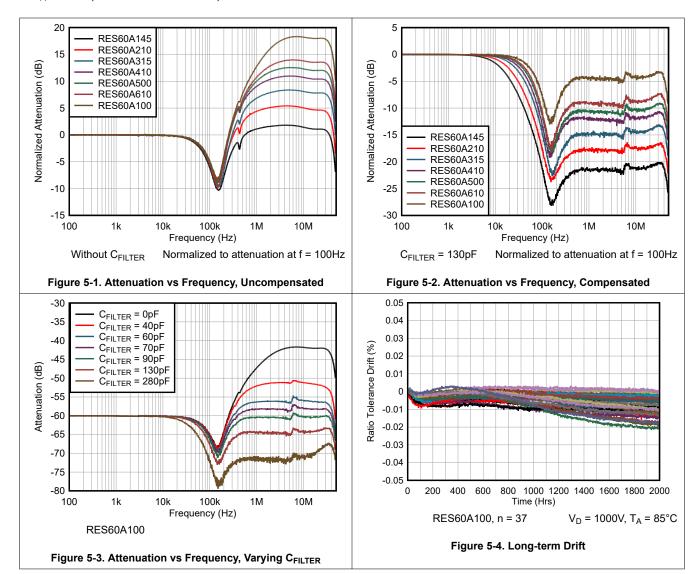
- (1) Input resistance (R_{HV}) and nominal ratio (G_{nom}) are the controlling specifications that dictate the values of R_{LV}. Nominal values of R_{LV} are reported with three significant figures for convenience.
- (2) R_{HV} / R_{LV} vs nominal ratio.
- (3) The specification is the result of this expression, given as a percentage (multiplied by 100%)
- (4) Specified by design and accelerated qualification testing.
- (5) R_{HV} and R_{LV} vs nominal values.
- (6) Specified by characterization.
- (7) Specified by design.
- The –3dB bandwidth for a given device and application is heavily influenced by parasitic device-level and board-level capacitances. Feed-forward capacitances cause attentuation at high frequencies to fall below nominal values, resulting in gain peaking. Use a filtering capacitor in parallel with R_{LV} for gain shaping and confirm attentuation across frequency meets circuit and design goals. The value of this capacitor is best determined and verified experimentally. Refer to Typical Characteristics and Layout Guidelines for additional information.

Submit Document Feedback



5.6 Typical Characteristics

at T_A = 25°C (unless otherwise noted)



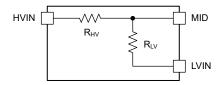


6 Detailed Description

6.1 Overview

The RES60A-Q1 consists of two, precision, thin-film SiCr resistors, arranged to form a matched divider and encapsulated by an insulative SiO_2 layer. The device contains an *input* resistor, R_{HV} , that is nominally 12.5M Ω . The device also incorporates a *gain* resistor, R_{LV} , with a value that depends on the nominal ratio (R_{HV} / R_{LV}) of the RES60A-Q1.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Absolute and Ratiometric Tolerances

The resistors of the RES60A-Q1 are described by the following equations:

$$R_{HV} = R_{HVnom} \times (1 \pm t_{absRHV}) = R_{HVnom} \times (1 \pm t_{RHV}) \times (1 \pm t_{SiCr})$$
(1)

$$R_{LV} = R_{LVnom} \times (1 \pm t_{absRLV}) = R_{LVnom} \times (1 \pm t_{RLV}) \times (1 \pm t_{SiCr})$$
(2)

 R_{HVnom} and R_{LVnom} are the nominal values of each resistor. The parameter t_{abs} is an error term that describes the absolute tolerance of the RES60A-Q1 resistor in question, such that $|t_{abs}| \le 15\%$. For example, a nominally $12.5M\Omega$ resistor with $t_{abs} = 5\%$ actually measures $13.125M\Omega$. This error is analogous to the specified *absolute tolerance* of most single-element resistors, or the end-to-end tolerance of more specialized resistor dividers.

Note

The RES60A-Q1 is not a laser-trimmed device. Each ratio of the RES60A-Q1 features a unique die specifically optimized for that ratio, providing the precise matching and consistent thermal characteristics necessary to achieve extremely low drift.

The absolute tolerance is dominated by the variation in the SiCr resistivity, t_{SiCr} . The two resistors of a given RES60A-Q1 are interdigitated and come from the same area of the wafer; therefore, t_{SiCr} is effectively the same for both of the two resistors, although t_{SiCr} varies on a part-to-part basis.

The following examples show that when the divider is considered in ratiometric terms, the t_{SiCr} error terms drop out. Parameter t_{Rx} is a residual error term that describes the remaining effective tolerance of each resistor of the given RES60A-Q1 device, after accounting for the universal t_{SiCr} .

$$\frac{R_{HV}}{R_{LV}} = \frac{R_{HVnom} \times (1 \pm t_{RHV}) \times (1 \pm t_{SiCr})}{R_{LVnom} \times (1 \pm t_{RLV}) \times (1 \pm t_{SiCr})} = \frac{R_{HVnom} \times (1 \pm t_{RHV})}{R_{LVnom} \times (1 \pm t_{RLV})} = G_{nom} \times \frac{(1 \pm t_{RHV})}{(1 \pm t_{RLV})} = G$$
(3)

$$\frac{R_{HV}}{R_{LV} + R_{HV}} = \frac{R_{HVnom} \times (1 \pm t_{RHV}) \times (1 \pm t_{SiCr})}{R_{LVnom} \times (1 \pm t_{RLV}) \times (1 \pm t_{SiCr}) + R_{HVnom} \times (1 \pm t_{RHV}) \times (1 \pm t_{SiCr})}$$

$$= \frac{R_{HVnom} \times (1 \pm t_{RHV})}{R_{LVnom} \times (1 \pm t_{RLV}) + R_{HVnom} \times (1 \pm t_{RHV})}$$
(4)

The individual values of t_{RHV} and t_{RLV} describe the tolerance of each individual resistor, but are not independent variables in a Gaussian sense. Rather, the matching of these values to each other (by design) is used to achieve highly stable ratiometric relationships between the resistors, giving an effective *ratio* with an extremely low error.

The RES60A-Q1 is specified with a maximum initial divider ratio tolerance of 0.1%, meaning that the relationship between the actual divider ratio, G, and the nominal ratio, G_{nom} , of a given divider is described by the following:

Submit Document Feedback



$$G = \frac{R_{HV}}{R_{IV}} = G_{nom} \times (1 \pm t_D)$$
 (5)

such that $t_D \le 0.1\%$. The limits of t_D for the RES60A-Q1 are enforced by precise parametric testing in production, with the divider voltage swept from $V_D = 250V$ to $V_D = 1000V$. Single-element resistors do not have an equivalent to t_D , because no part-to-part matching is considered other than the gradeout limit. In other divider data sheets, the equivalent of t_D is often called *ratio tolerance*.

Because any devices that do not meet these criteria are screened out at final test, this equation can be used with the previous equations to prove the effective bounds of t_{RHV} and t_{RLV} for a given ratio. Therefore, despite the wide absolute tolerance bounds of $\pm 15\%$, the worst-case initial absolute error tolerances of t_{RHV} and t_{RLV} are within approximately $\pm 0.115\%$ of each other.

6.3.2 Ultra-Low Noise

Noise in resistors can be evaluated in two separate regions: low-frequency flicker noise and wideband thermal noise. Flicker, or 1/f noise, is extremely important for systems that require signal gain at frequencies less that 100Hz. The flicker noise for thin-film resistors, including the RES60A-Q1, is lower than that of thick-film resistor processes. Thermal noise typically dominates in the region greater than 1kHz, and increases as resistor magnitude increases. Noise is modeled as a voltage source in series with the resistor.

For a resistive divider such as the RES60A-Q1, the thermal noise as measured at the center tap of two resistors R_{HV} and R_{LV} is equivalent to the thermal noise of a resistor with value $R_{HV} \parallel R_{LV}$:

$$e_{\rm N} = \sqrt{(4k_{\rm B}TR)} \tag{6}$$

where:

- e_N is the thermal noise density in nV/√Hz
- T is the absolute temperature in kelvins (K)
- k_B is the Boltzmann constant, 1.381 × 10-23 J/K
- R = R_{HV} || R_{LV}

R_{HV} >> R_{LV}; therefore, R ≈ R_{LV}. As an example, for the RES60A610-Q1:

$$e_{N} = \sqrt{(4k_{B}TR)} = \sqrt{4 \times 1.38E^{-23} \frac{J}{K} \times 278K \times (12.5M\Omega \parallel 20.49k\Omega)} = 18nV/\sqrt{Hz}$$
 (7)

6.4 Device Functional Modes

The RES60A-Q1 features a single pad for the HVIN pin and two pads for the MID and LVIN pins, with all other pads and pins electrically floating. Connect both the MID and LVIN pins to the *low-voltage domain* of the system, such as a microcontroller ADC input and chassis ground, respectively. Bias the HVIN pin to the high potential of the measured system, such as the high side of the battery stack.

HVIN and LVIN can be used to measure directly between the high side and low side of the battery. However, to avoid an overvoltage condition, verify that the downstream circuitry driven by MID is properly referenced to the low side (LVIN).



7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Battery Stack Measurement

The RES60A-Q1 can be used in conjunction with an automotive precision amplifier, such as the OPA192-Q1, for single-ended measurement of the high side (BAT+) of an EV battery relative to a fixed potential. For those systems where BAT- and GND are equivalent, as in Figure 7-1 (a), the configuration shown in Figure 7-2 applies. An alternative approach is to measure directly across the battery from BAT+ to BAT-, as shown in Figure 7-3. This approach is useful for systems referenced to the low side of the battery, BAT-, as in Figure 7-1 (b).

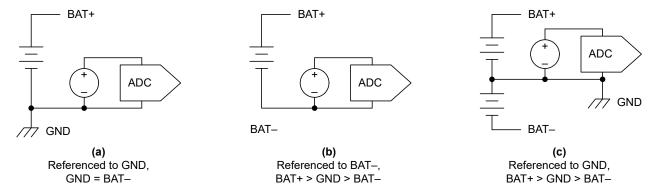


Figure 7-1. Common Battery and System Configurations

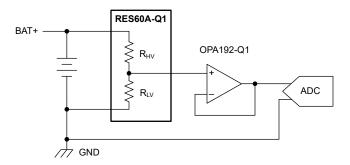


Figure 7-2. Single-Ended Measurement, BAT+ to GND

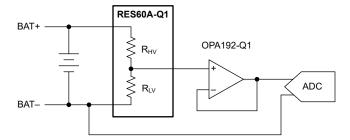


Figure 7-3. Single-Ended Measurement, BAT+ to BAT-

Product Folder Links: RES60A-Q1



For some system architectures, BAT– floats relative to the chassis GND; see also Figure 7-1 (c). If for example a microcontroller referenced to chassis ground needs to measure the voltage across the entire battery stack, a difference amplifier can be constructed using two RES60A-Q1 devices and an OPA192-Q1. Figure 7-4 shows this approach. If two ADC channels are available, two single-ended measurements can be done using two RES60A-Q1 devices and an OPA2192-Q1.

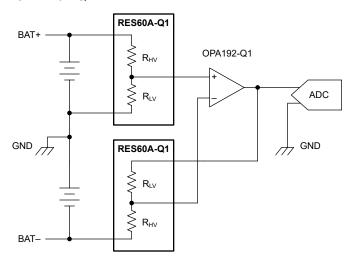


Figure 7-4. Differential Measurement, BAT+ to BAT-

Leakage in the system and quiescent current from the amplifier input reduce the precision of the measurement. In some cases, a guard buffer can be used to reduce leakage currents. Follow best practices to reduce board contamination and leakage.

For an 800V single-ended battery measurement (see also Figure 7-2), the static current through the divider is:

$$I_{\text{STATIC}} = \frac{V_{\text{BATT}}}{(R_{\text{HV}} + R_{\text{LV}})} = \frac{800V}{(12.5M\Omega + 20.49k\Omega)} = 63.9\mu\text{A}$$
 (8)

Therefore, the buffer amplifier used must have a low bias current, such that $I_B << I_{STATIC}$. The low bias current of the OPA192-Q1 (5pA typical at 25°C, 5nA maximum from -40°C to +125°C) makes the device an excellent choice for this role.

7.1.2 Gain Scaling the RES60A-Q1 With the RES11A-Q1

While multiple RES60A-Q1 ratios are available, additional effective ratios are achieved by finely scaling the divider output using a low-offset buffer amplifier and low-voltage matched divider network such as the RES11A-Q1. The low ratiometric errors of the RES11A-Q1 minimize additional gain error contributions to the signal chain, while maximizing the input full-scale range (FSR) of downstream ADCs.

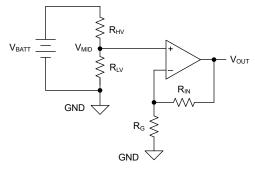


Figure 7-5. Battery Pack Measurement with RES60A-Q1 and RES11A-Q1



$$V_{\text{MID}} = V_{\text{BATT}} \times \frac{R_{\text{LV}}}{R_{\text{HV}} + R_{\text{LV}}} = \frac{V_{\text{BATT}}}{G_{\text{R60}} + 1} \tag{9}$$

$$V_{OUT} = V_{MID} \left(\frac{R_{IN}}{R_G} + 1 \right) = V_{MID} \left(\frac{1}{G_{R11}} + 1 \right) = V_{BATT} \left(\frac{1 + G_{R11}}{G_{R11} \times (G_{R60} + 1)} \right)$$
 (10)

For brevity, the effective transfer function of the RES60A-Q1, RES11A-Q1, and amplifier circuit is summarized as G_{SF} .

$$G_{SF} = \frac{G_{R11} \times (G_{R60} + 1)}{1 + G_{R11}} \tag{11}$$

$$V_{OUT} = V_{BATT} \times \left(\frac{1}{G_{SF}}\right) \tag{12}$$

Table 7-1 shows the effective voltage divider scaling factor G_{SF} associated with various RES60A-Q1 and RES11A-Q1 combinations.

Table 7-1. Effective Scaling Factor G_{SF} for the RES60A-Q1 and RES11A-Q1 Combinations

G _{R60}	145	210	315	410	500	610	1000	
G _{R11}		EFFECTIVE SCALING FACTOR G _{SF}						
None	146.00	211.00	316.00	411.00	501.00	611.00	1001.00	
1	73.00	105.50	158.00	205.50	250.50	305.50	500.50	
1.5	87.60	126.60	189.60	246.60	300.60	366.60	600.60	
1.6667	91.26	131.88	197.51	256.89	313.15	381.90	625.67	
2	97.33	140.67	210.67	274.00	334.00	407.33	667.33	
2.5	104.29	150.71	225.71	293.57	357.86	436.43	715.00	
3	109.50	158.25	237.00	308.25	375.75	458.25	750.75	
4	116.80	168.80	252.80	328.80	400.80	488.80	800.80	
5	121.67	175.83	263.33	342.50	417.50	509.17	834.17	
9	131.40	189.90	284.40	369.90	450.90	549.90	900.90	
10	132.73	191.82	287.27	373.64	455.45	555.45	910.00	

Submit Document Feedback



7.2 Typical Application

The RES60A-Q1 can be configured with an isolated amplifier such as the AMC1311B-Q1 for measurements requiring reinforced isolation. Figure 7-6 shows an example circuit configuration for such an application, where the RES60A-Q1 attenuates the input voltage and the AMC1311B-Q1 crosses the isolation barrier. A discrete difference amplifier with RES11A-Q1 and OPA388-Q1 is used to adapt the differential output voltage of the AMC1311B-Q1 for use with a single-ended 5V ADC.

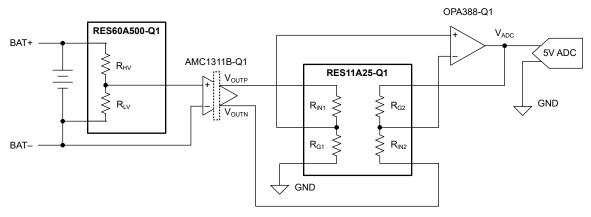


Figure 7-6. DC Bus Measurement With the RES60A-Q1 and AMC1311B-Q1

7.2.1 Design Requirements

PARAMETER	DESIGN GOAL
DC bus voltage range	0V to 1000V
Output (V _{ADC}) full-scale range	0V to 5V
Attenuation (nominal ratio)	500:1
Uncalibrated initial measurement error	±0.5% FSR

7.2.2 Detailed Design Procedure

This design attenuates the high common-mode voltage of the bus to a level that falls within the linear input range of the AMC1311B-Q1. Some key possible circuit error sources can be considered as follows:

- The AMC1311B-Q1 has a typical input bias current of 3.5nA. With $R_{LV} = 25k\Omega$, this input bias current manifests appears as an 88µV offset error at MID. When this offset is calculated in a root-sum-of-squares with the 400µV typical input offset voltage of the AMC1311B-Q1, a 410µV offset results. This offset represents 0.0205% of the 2V full-scale range, and is typically not the dominating error factor.
- The gain error and integrated nonlinearity error of the AMC1311B-Q1 can be approximated using the Isolated Amplifier Voltage Sensing Excel Calculator. For this example, the typical FSR error is calculated as 0.06%.
- The typical initial ratiometric gain tolerance of the RES60A500-Q1 is 0.02%, which sums with the previously
 mentioned errors of the AMC1311B-Q1 in a root-sum-of-squares manner to give a total typical FSR error of
 0.066%.
- The level-shifting circuit introduces additional errors, and applies a gain factor to the previously discussed errors. However, due to the low offset of the OPA388-Q1 and high precision of the RES11A-Q1, these errors (0.012% FSR) are low enough to not significantly impact the final typical error.

The final calculated result of 0.068% typical FSR error represents a 1σ value, so a $\pm 6\sigma$ estimate gives $\pm 0.41\%$ FSR error. The results suggest the circuit meets the $\pm 0.5\%$ FSR application requirement, with margin.



7.2.3 Application Curves

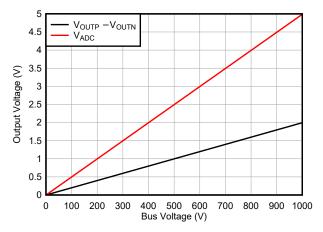


Figure 7-7. Transfer Function

7.3 Power Supply Recommendations

The RES60A-Q1 is a high-voltage resistor divider, with no active circuitry or protective diodes. There are no specific power-supply connection requirements other than respecting the limits expressed in *Absolute Maximum Ratings* and *Recommended Operating Conditions*. To provide additional protection against high-edge-rate transient events, use a high-voltage capacitor at the device input. Be aware that additional input capacitance extends step-response settling times. A TVS diode at the MID pin provides additional protection against fast transients for downstream low-voltage circuitry, if necessary.

Submit Document Feedback



7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Reduce parasitic coupling by running sensitive traces, such as the MID connection, as far away from supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Make sure supply voltages are adequately filtered.
- Power dissipated in the RES60A-Q1 causes the junction temperature to rise. For reliable operation, junction temperature must be limited to 150°C, maximum. Maintaining a lower junction temperature results in higher reliability.
 - Package thermal resistance, R_{θJA}, is affected by mounting techniques and environments. Poor air circulation can significantly increase thermal resistance to the ambient environment. Best thermal performance is achieved by soldering the RES60A-Q1 onto a circuit board with wide printed circuit traces, especially for the LVIN connection, to allow greater conduction through the device leads.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the
 plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture
 introduced into the device packaging during the cleaning process.
 - A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.
- Use conformal coating or potting, the deposition of an insulating polymer or other material layer over an assembled PCB, to reduce the pollution degree around the RES60A-Q1. This process reduces the requirements for creepage and clearance distances by eliminating or reducing the influence of pollutants.
- Use groove cutting to attain a lower PCB creepage distance. For grooves wider than 1mm, the effective
 creepage distance is the existing creepage distance plus the width of the groove and twice the depth of the
 groove. This sum must equal or exceed the required creepage distance. The groove must not weaken the
 substrate to the point of failure to meet mechanical test requirements. All layers under the groove must be
 free from traces, vias, and pads to maintain the maximum creepage distance.
- Place a filtering capacitor, C_{FILTER}, in parallel with R_{LV} by connecting the capacitor between the LVIN and MID pins. The value of this capacitor is experimentally determined, and depends on application requirements such as intended bandwidth and attentuation flatness characteristics. Circuit parasitics can cause attenuation at high frequencies to be less than the expected attenuation at dc, as the circuit parasitics interact with device parasitic capacitances to form an impedance divider. Use a capacitor with a sufficiently high voltage rating to withstand any anticipated high-frequency transients, such as those caused by switching events.



7.4.2 Layout Example

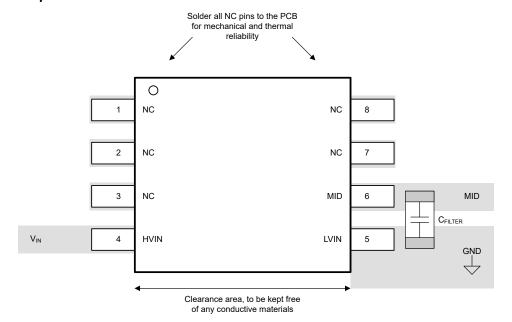


Figure 7-8. Layout Example

Submit Document Feedback



8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype designs before committing to layout and fabrication, reducing development cost and time to market.

8.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design and simulation tools web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

8.1.1.3 TI Reference Designs

TI reference designs are analog designs created by TI's precision analog applications experts. TI reference designs offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI reference designs are available online at https://www.ti.com/reference-designs.

8.1.1.4 Analog Filter Designer

Available as a web-based tool from the Design and simulation tool web page, the Analog Filter Designer allows the user to design, optimize, and simulate complete multistage active filter designs within minutes.



8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, What Are Creepage And Clearance? TI Precision Labs video
- Texas Instruments, RES11A-Q1 Automotive, Low-Noise, Precision, Matched, Thin-Film Resistor Pairs data sheet
- Texas Instruments, RES60EVM evaluation module

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TINA-TI™ and TI E2E™ are trademarks of Texas Instruments.

TINA™ is a trademark of DesignSoft, Inc.

PSpice® is a registered trademark of Cadence Design Systems, Inc.

All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2024) to Revision A (October 2025)

•	Removed RES60A310 (310:1 ratio) and replaced with RES60A315 (315:1 ratio), and added RES60A145
	(145:1 ratio), throughout document
•	Updated formatting of min and max voltage specifications in Absolute Maximum Ratings and Recommended
	Operating Conditions
•	Updated footnotes describing short-term overload voltage and transient high-potential voltages in <i>Absolute</i>
	Maximum Ratings3

- Updated typical values in *Electrical Characteristics* Changed initial ratio tolerance spec to apply from V_D = 250V to V_D = 1000V

Product Folder Links: RES60A-Q1

Page



•	Added absolute voltage coefficient of resistance (per resistor) specification
	Updated descriptions of pin capacitance and –3dB bandwidth, and typical values
	Updated test conditions for settling time
	Added Typical Characteristics
	Updated Ratiometric Matching and renamed to Absolute and Ratiometric Tolerances
	Added Gain Scaling the RES60A-Q1 With the RES11A-Q1 to Application Information
	Added discussion of low-voltage filtering capacitance, C _{FILTER} , to Layout Guidelines

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 21-May-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
XRES60A100QDWVRQ1	Active	Drangaduation	COIC (DWAA) I o	4000 LL ADOF TOD		(4) Call TI	(5) Call TI	-40 to 125	
ARESOUATUUQDWVRQT	Active	Preproduction	SOIC (DWV) 8	1000 LARGE T&R	-	Call 11	Call 11	-40 to 125	
XRES60A100QDWVRQ1.B	Active	Preproduction	null (null)	1000 LARGE T&R	-	Call TI	Call TI	See XRES60A100QDWVRQ	
XRES60A410QDWVRQ1	Active	Preproduction	SOIC (DWV) 8	1000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
XRES60A410QDWVRQ1.B	Active	Preproduction	null (null)	1000 LARGE T&R	-	Call TI	Call TI	See XRES60A410QDWVRQ	
XRES60A500QDWVRQ1	Active	Preproduction	SOIC (DWV) 8	1000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
XRES60A500QDWVRQ1.B	Active	Preproduction	null (null)	1000 LARGE T&R	-	Call TI	Call TI	See XRES60A500QDWVRQ	

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

www.ti.com 21-May-2025

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



SOIC



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOIC



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025