REF80 Temperature-Controlled Buried Zener Reference with 0.05ppm/°C Drift and < 1ppm Stability

1 Features

- 7.6V ultra-precision reference with minimal number of external components
- Ultra-low temperature drift: 0.05ppm/°C
- Excellent long term stability: 0.3ppm (1k hour to 5k hour)
- Integrated heater with temperature stable indicator
- 1/f noise (0.1Hz to 10Hz) : $0.12\text{ppm}_{\text{pk-pk}}$
- Input Voltage range: 10V to 16.5V
- Heater supply range: 10V to 42V
- Hermetically sealed ceramic package (20 pin LCCC)

2 Applications

- Parametric measurement unit
- Lab and field instrumentation
- Precision weight scales
- Battery test equipment
- Digital multimeter
- Source measurement unit
- Data acquisition

3 Description

The REF80 is a highly integrated ultra-low drift buried zener precision voltage reference. The REF80 combines a precision 7.6V reference with an internal heater to achieve extremely low temperature drift of 0.05ppm/°C. The integrated heater maintains the internal temperature of the die at a constant set point. This helps the reference voltage stay constant irrespective of ambient temperature variations. The device internal temperature is pre-programmed to eliminate design complexities. This allows for fast design cycles, easy bring up and no dependence on high-cost external precision components.

The REF80 family is available in a 20-pin LCCC package. The LCCC package is a hermetically sealed ceramic package that enables ultra-low long-term stability specification of 0ppm (after settling), critical for applications that demand a long time period without calibration. The package also offers excellent immunity against humidity variation.
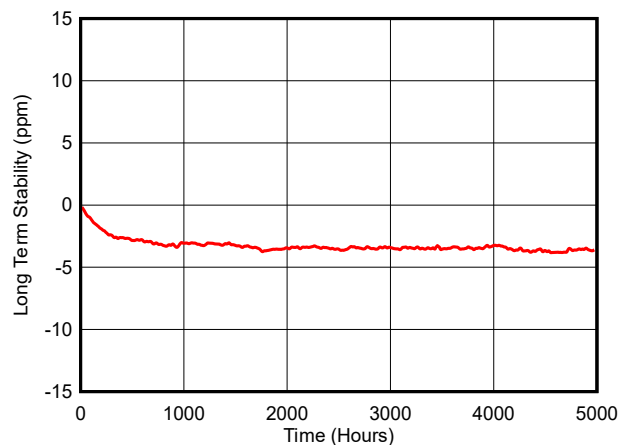
Device Information

PART NAME	PACKAGE [1]	BODY SIZE (NOM) [2]
REF80	LCCC (20)	8.89mm × 8.89mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
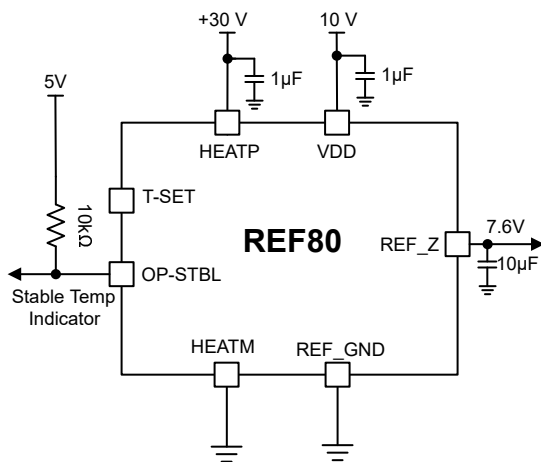
REF80 Circuit Diagram
(With Supply and Passive Requirement)
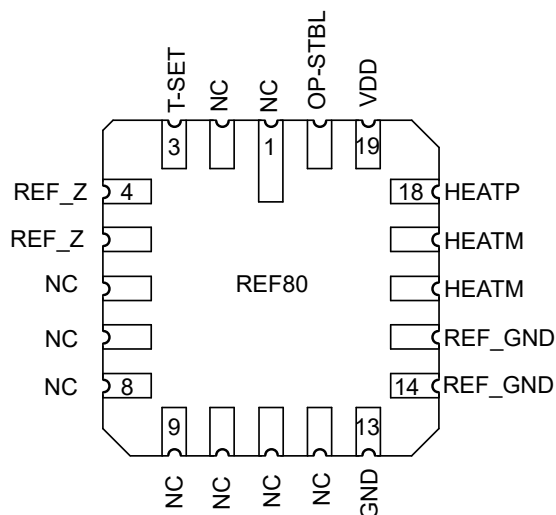

Reference Voltage Drift Vs Time

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Product Folder Links: *REF80*

4 Device Comparison Table

PRODUCT	V_{REF_Z}	Temperature Range
REF80000B1NAJT	7.6V	0ºC to 70ºC

5 Pin Configuration and Functions

Figure 5-1. NAJ Package
20-Pin LCCC
Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	**Number**		
NC	1, 2, 6-12	No Connect	No connect pin. Leave this pin floating or connected to GND.
T-SET	3	Input	Connect resistor to adjust the heater temperature. Leave the pin floating to use factory programmed heater set point. Refer Section 7.3.1 for more details.
REF_Z	4,5	Output	Reference voltage output. Connect a 10µF to 100µF output capacitor to REF_GND for the best performance.
GND	13	Ground	This pin must be shorted to REF_GND pin.
REF_GND	14, 15	Ground	Reference ground pin.
HEATM	16, 17	Power	Heater power supply negative connection.
HEATP	18	Power	Heater power supply positive connection.
VDD	19	Power	Power supply for buried zener core and buffer.
OP_STBL	20	Output	Active high open drain output. Indicates the internal heater is stabilized at factory programmed temperature.

Product Folder Links: *REF80*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, all the voltages ratings are specified with respect to REF_GND pin voltage (unless otherwise noted) [1]

		MIN	MAX	UNIT
Voltage	VDD, OP_STBL,	−0.3	18	V
	T-set, NC	−0.3	6	V
	REF_Z	−0.3	10	V
	HEATP	−0.3	48	V
	HEATM	−42	0.3	V
	HEATP - HEATM	0	42	
Output short circuit current	I_{SC}		30	mA
Operating temperature range	T_A	−55	125	°C
Storage temperature range	T_{stg}	−65	170	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified in the Electrical Characteristics Table is not implied.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins [2]	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC[1]		REF80		UNIT
		NAJ (LCCC)		
		20 PINS		
		1s0p JEDEC	REF8EVM	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	103.6	141.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.1	55.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	38.3	39.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	45.1	55.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range, all the voltages ratings are specified with respect to REF_GND pin voltage (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	VDD	10		16.5	V
	REF_Z	0		8	
	VHET Heater voltage, $V_{(HEATP - HEATM)}$	10		42	
	HEATP	0		42	
	HEATM	-42		0	
	OP_STBL	0		VDD	
Current	OP_STBL (I_{OL})	0		5	mA
T_A	Operating temperature	-40		70	°C

6.5 Electrical Characteristics

At VDD = 10V, VHET= 30V, T_{SET} = 115°C, C_{REF_Z} = 10μF, C_{VDD} = 1μF, I_L = 0mA, T-SET = Open, OP_STBL is pulled up to 5V through 10kΩ resistor, minimum and maximum specifications across supported temperature range, typical specifications T_A = 25°C; unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT						
REF_Z	Output voltage			7.6		V
	Output voltage accuracy		−50		50	mV
	Output voltage temperature coefficient[1]	T_A = 0°C to 70°C		0.05	0.2	ppm/°C
HYSTERESIS AND LONG-TERM STABILITY						
	Long-term stability	1000 hours, T_A = 25°C, T_{SET} = 115°C		3		ppm
		1000 hours to 5000 hours , T_A = 25°C, T_{SET} = 115°C		0.3		
	Output voltage hysteresis	Cycle 1		1		ppm
		Cycle 2		0.3		ppm
NOISE						
e_{np-p}	Low frequency noise	f = 0.1Hz to 10Hz		0.12		ppm_{p-p}
e_n	Output voltage noise	f = 10Hz to 100Hz,		0.6		uV_{rms}
LINE REGULATION						
$\Delta V_{REF\_z}/\Delta VDD$	Line regulation	VDD = 10V to 16.5V		4	10	ppm/V
POWER SUPPLY						
VDD	Input voltage		10		16.5	V
VHET	Input voltage	(HEATP - HEATM)	10		42	V
IHET	Start up current			335		mA
	Quiescent current	T_A = 25°C, T_{SET} = 115°C, VHET = 10V		75		
		T_A = 25°C, T_{SET} = 115°C, V_{HEATER} = 42V		18		
I_{VDD}	Quiescent current			15		mA
TURNON TIME						
Start-up	V_{REF_Z}	REF_Z settled within ±3ppm from VDD and VHET power up time		100		sec
	Heater regulation time	OP_STBL goes to logic high level form VHET power-up time		250		ms

6.5 Electrical Characteristics (continued)

At VDD = 10V, VHET= 30V, T_{SET} = 115℃, C_{REF_Z} = 10µF, C_{VDD} = 1µF, I_L = 0mA, T-SET = Open, OP_STBL is pulled up to 5V through 10kΩ resistor, minimum and maximum specifications across supported temperature range, typical specifications T_A = 25℃; unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
OP_STBL						
V_{OL}	Low level output voltage	OP_STBL Pin Current I_{OL} = 5mA		0.65		V
I_{LKG}	Leakage Current when output is high	Pullup Voltage at OP_STBL V_{PULLUP} = 18V		100		nA
STABLE CAPACITANCE RANGE						
	Input capacitor range			0.1		µF
	Output capacitor range [2]		10		100	µF

(1) Temperature drift is calculated using box method
(2) ESR for the capacitor can range from 10mΩ to 400mΩ

6.6 Typical Characteristics

At T_A = 25°C, V_{IN} = 10V, VHET = 30V, C_{REF_Z} = 10µF, C_{VDD} = 1µF, (unless otherwise noted)
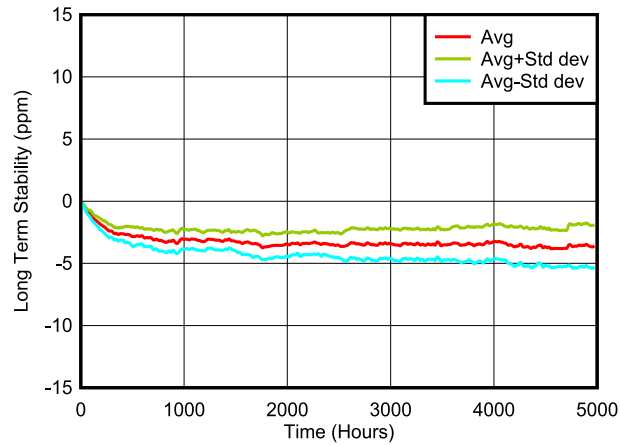
Figure 6-1. Long-Term Stability
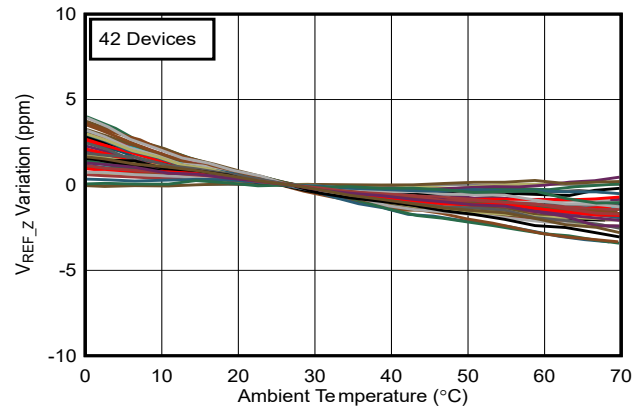
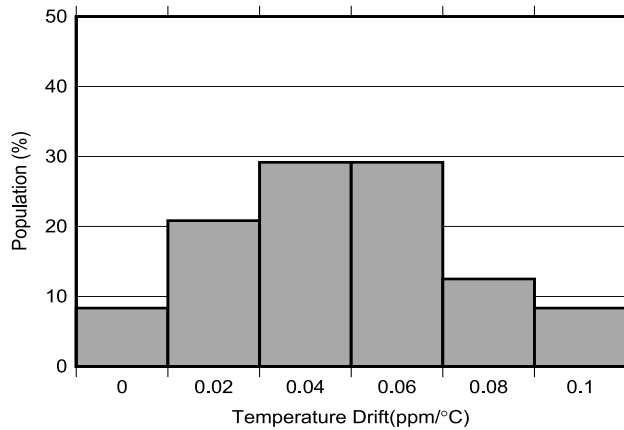**Figure 6-2. V_{REF_Z} Vs Free-Air Temperature**
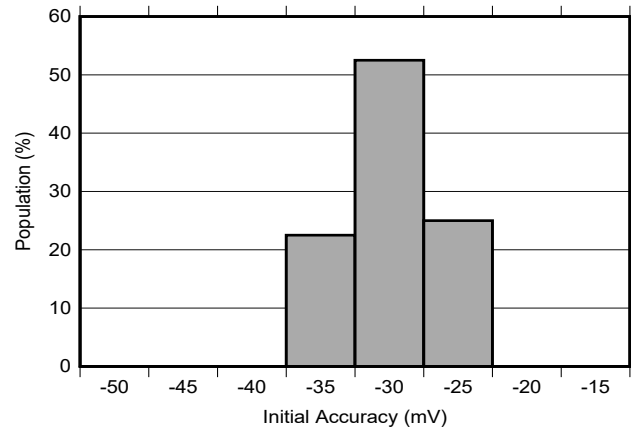

Figure 6-3. Temperature Drift Distribution
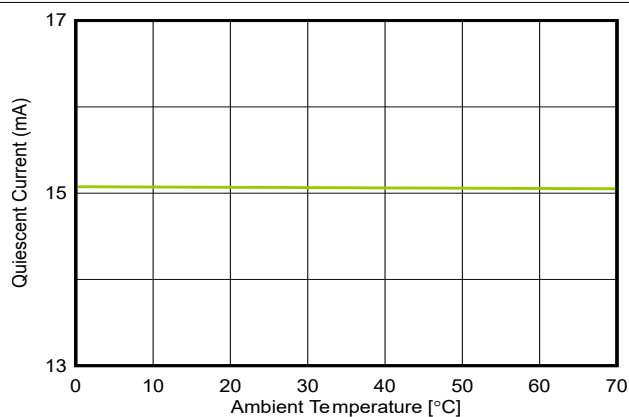

Figure 6-4. Accuracy Distribution
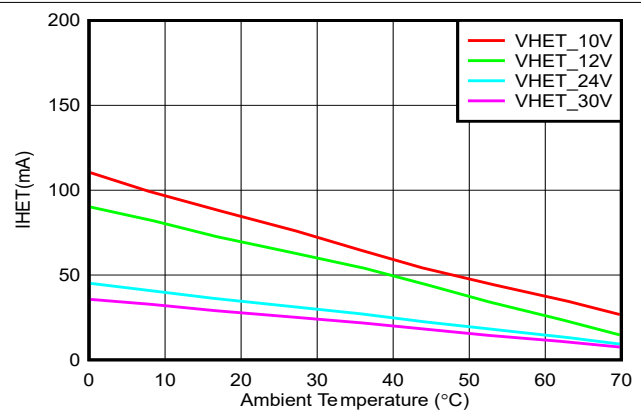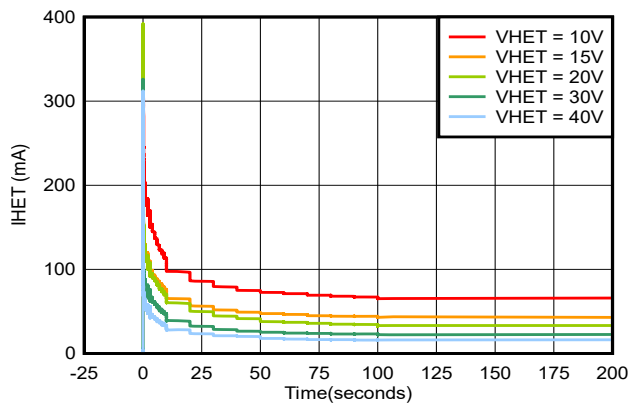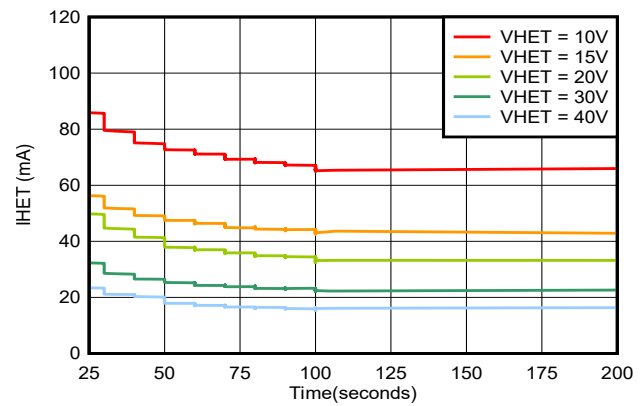

Figure 6-5. Supply Current (I_{VDD}) vs Temperature

**Figure 6-6. Steady State Heater Current
IHET vs Temperature**

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Product Folder Links: *REF80*

6.6 Typical Characteristics (continued)

At T_A = 25°C, V_{IN} = 10V, VHET = 30V, C_{REF_Z} = 10µF, C_{VDD} = 1µF, (unless otherwise noted)

Figure 6-7. Startup Heater Current
IHET vs Time

Figure 6-8. Startup Heater Current (Zoomed View)
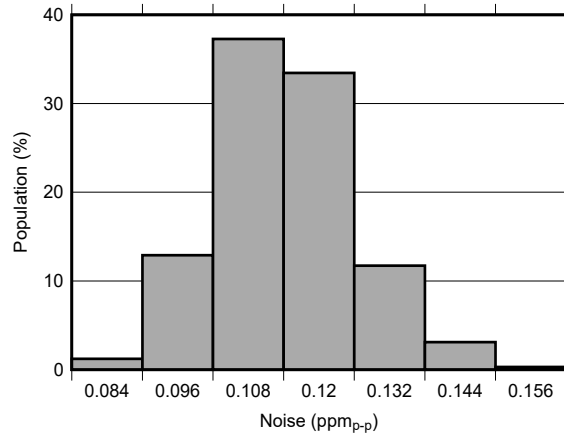**IHET vs Time**

Figure 6-9. 0.1Hz to 10Hz Voltage Noise Distribution
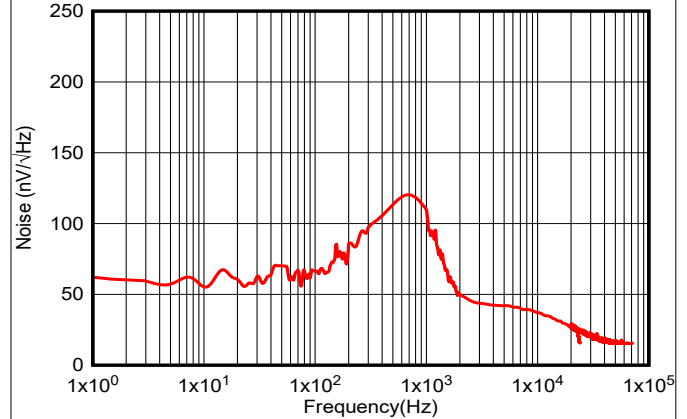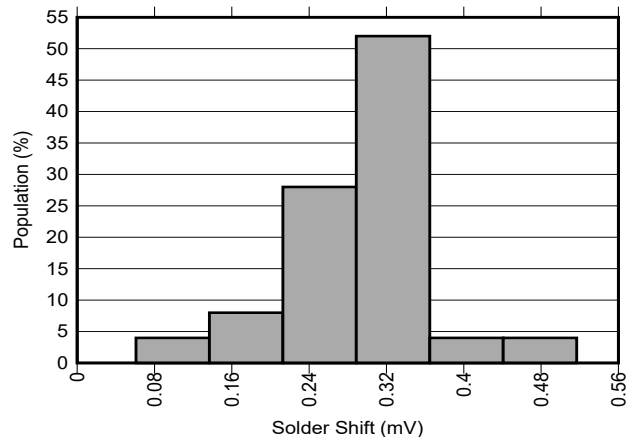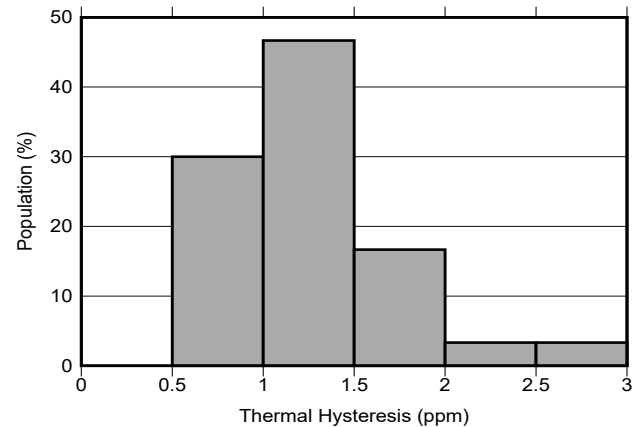

Figure 6-10. Noise Density vs Frequency

Figure 6-11. Solder Shift Distribution

Figure 6-12. Thermal Hysteresis (Cycle 1) Distribution
T_A = 0°C to 70°C

6.6 Typical Characteristics (continued)

At T_A = 25°C, V_{IN} = 10V, VHET = 30V, C_{REF_Z} = 10µF, C_{VDD} = 1µF, (unless otherwise noted)
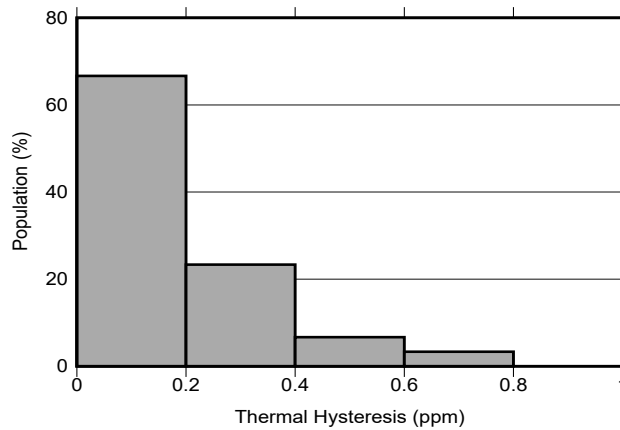

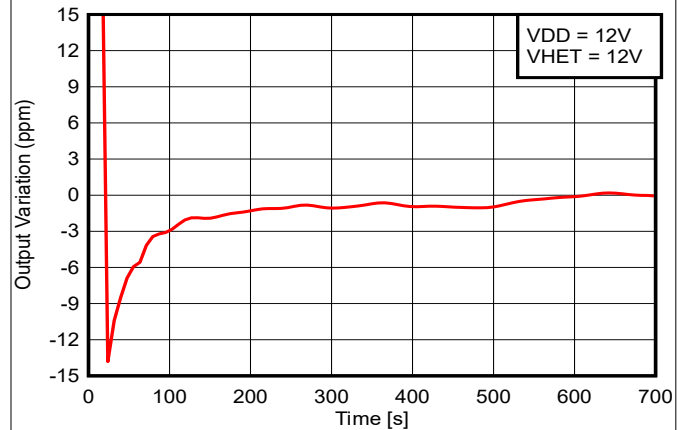**Figure 6-13. Thermal Hysteresis (Cycle 2) Distribution T_A = 0°C to 70°C**

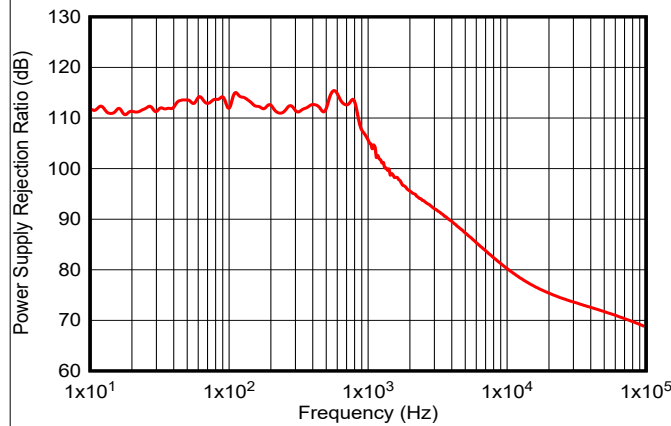**Figure 6-14. Startup Behavior**

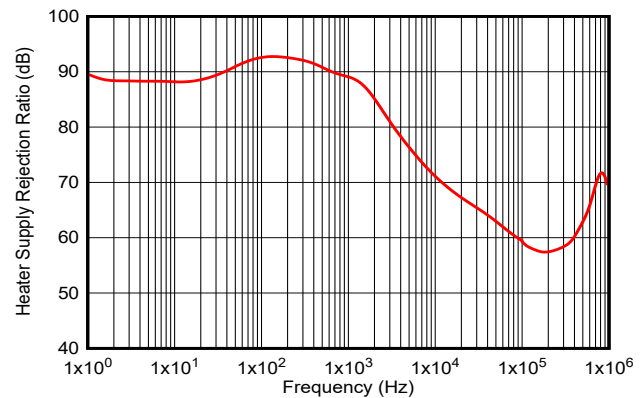**Figure 6-15. Power-Supply Rejection Ratio vs Frequency**

Figure 6-16. Heater Supply Rejection Ratio vs Frequency

7 Detailed Description

7.1 Overview

The REF80 is temperature controlled, buried zener voltage reference specifically designed for excellent voltage stability over time and temperature. The Figure 7-1 is the simplified block diagram of the REF80 showing the generation of voltage reference with buried zener and on chip heater control.
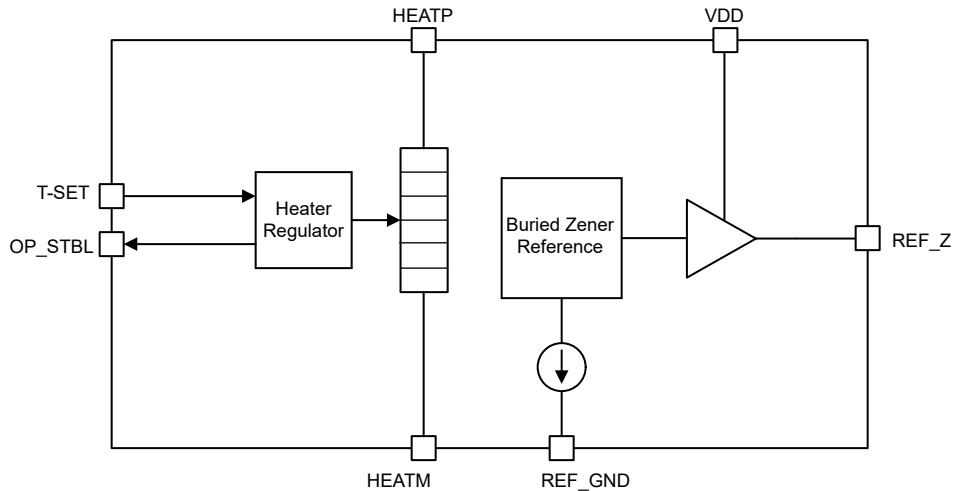
7.2 Functional Block Diagram

Figure 7-1. Functional Block Diagram for REF80

7.3 Feature Description

7.3.1 Heater

REF80 has on chip heater which is factory programmed to T_{SET} temperature as per Table 7-1 to regulate the temperature of the die within ±1ºC, for the entire operating ambient temperature range. This allows REF80 to achieve ultra low temperature drift of 0.05ppm/ºC. Heater has dedicated supply pins HEATP and HEATM which run independent of VDD supply pin. The steady state power dissipation of the heater is directly proportional to the difference between ambient temperature T_A and T_{SET} as per Equation 1. Heater current depends on (HEATP - HEATM) voltage. Heater takes high transient current at the time of start-up to heat up the device from ambient. REF80 has heater indicator pin OP_STBL, which de-asserts when the heater reaches within ±0.1% of T_{SET}.

Table 7-1. T_{SET} of Heater

Operating Temperature Range (T_A)	T_{SET}
0ºC to 70ºC	115ºC

$$P_{HEATER}(W) = \left(\frac{T_{SET} - T_A}{R_{\theta JA}}\right) - V_{DD} \times I_{VDD} \tag{1}$$

V_{DD} is supply voltage for the chip and I_{VDD} is the supply current.

$R_{\theta JA}$ depends on board thickness and layout. The data sheet value of $R_{\theta JA}$ is based on JEDEC standard board.

REF80 offers flexibility to decrease the heater temperature by putting a resistor with less than 2% tolerance on the T-SET pin as per Table 7-2 to save power and reduce the thermal noise for restricted ambient temperature applications. T_{SET} must be programmed to 45ºC above the max ambient temperature to make sure that the heater is regulating the temperature properly. REF80 samples the value of the resistor at the time of startup and the value of T_{SET} is modified accordingly. Small drift in resistor value does not impact the T_{SET} temperature as T-SET pin samples discreet value.

Table 7-2. T-SET Pin Resistor VS Change in T_{SET}

Resistor on T-SET pin	Heater Temperature
0	T_{SET}
130kΩ	T_{SET} - 10ºC
360kΩ	T_{SET} - 20ºC
800kΩ	T_{SET} - 30ºC
OPEN	T_{SET}

For the applications that require the device to be turned off, make sure to power off for at least 15 seconds before turning the device back on.

7.3.2 Buried Zener Reference

The 7.6V reference output is generated with an ultra low noise buried zener diode which is biased at 15mA current. This buried zener exhibits extremely stable long term stability characteristics, which helps REF80 to achieve an accuracy of calibration grade instruments.

Product Folder Links: *REF80*

8 Parameter Measurement Information

8.1 Long-Term Stability

Buried zener references typically exhibit very stable long term stability and are used as an ultra stable reference for internal calibration of the system. The long-term stability value is tested in a typical setup that reflects standard PCB board manufacturing practices for references with a strain modulation structure around the device. The boards are made of standard FR4 material with 35µm of Copper. The devices have been soldered through standard reflow.

Long term stability setup is designed with utmost care to minimize impact of thermocouple error, strain impact and mechanical vibration in long term stability measurement. The boards are maintained at 25°C in an air drift oven with heater temperature set to 115°C in powered on condition for long term stability measurement.

Typical long-term stability characteristic is expressed as a deviation over time. Figure 8-1 shows the typical drift value for the V_{REF_Z} is 3ppm from 0 to 1000 hours. Drift of REF80 gets flat after 1000 hours. Powered-up burn-in at room temperature helps REF80 to achieve best long term stability performance.

Power cycle has minimal impact on the stability of the V_{REF_Z} and doesn't change the settled profile. Figure 8-2 shows the behavior of the output when the devices are powered off for 24 hours.
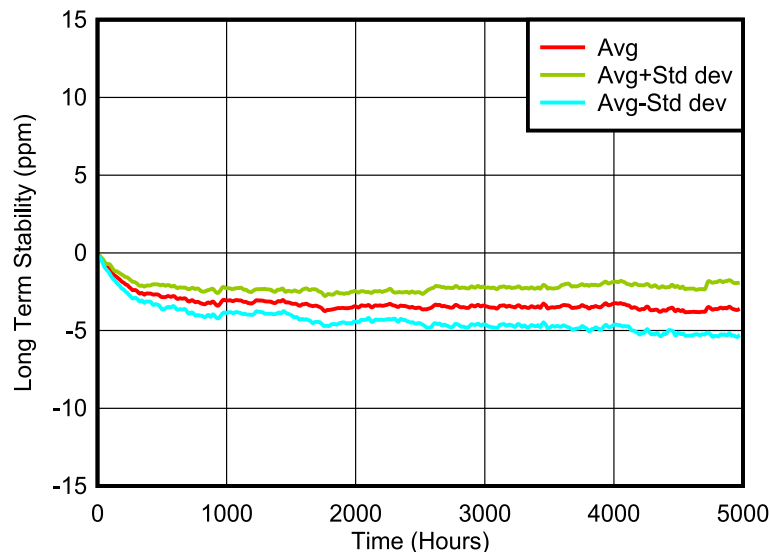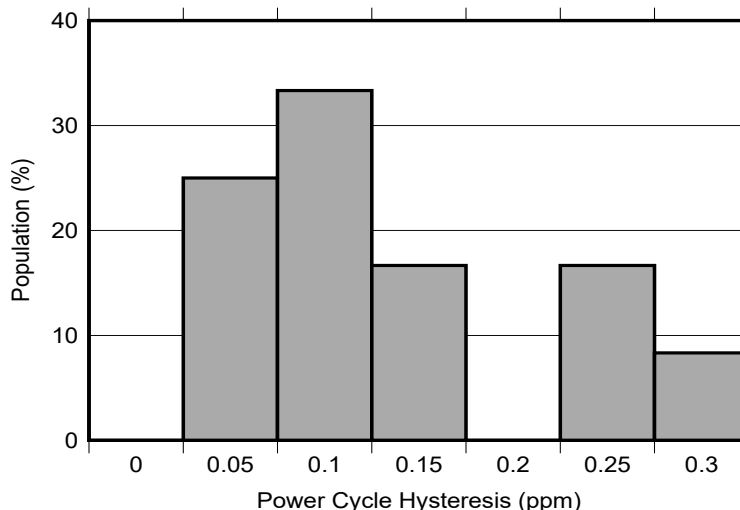

Figure 8-1. Long Term Stability (V_{REF_Z})

Figure 8-2. Power Cycle Hysteresis

8.2 Temperature Drift

The REF80 has integrated on chip heater, which is factory programmed to T_{SET} = 115°C temperature. Heater regulates the T_{SET} temperature to ±1°C for entire operating temperature range. This results in 0.05ppm/°C temperature drift coefficient for REF80. Figure 6-2 shows temperature drift profile of 42 devices.

The temperature coefficient is calculated using the box method in which a box is formed by the min/max variation for the nominal output voltage over the operating temperature range. REF80 has a maximum temperature coefficient of 0.2ppm/°C for 0°C to70°C temperature range. The box method specifies limits for the temperature error but does not specify the exact shape and slope of the device under test. See *SLYT183* for more information on the box method. The box method equation is shown in Equation 2:

$$\text{Drift}\left(\text{ppm/°C}\right) = \left(\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF(25°C)} \times \text{Temperature Range}}\right) \times 10^6 \tag{2}$$
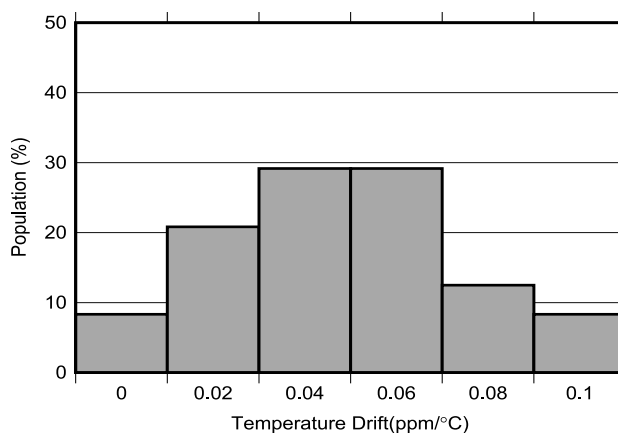

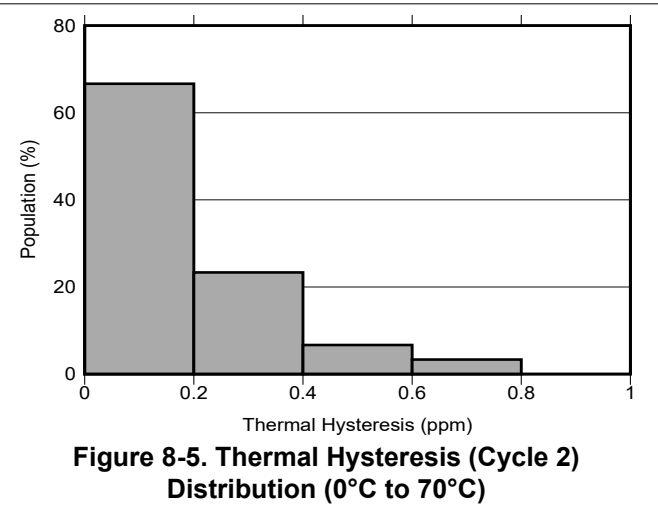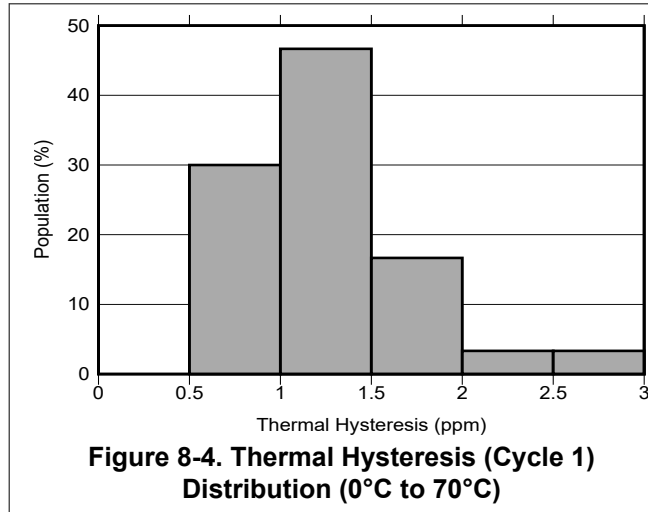**Figure 8-3. Temperature Drift Distribution**

8.3 Thermal Hysteresis

Thermal hysteresis is measured with the REF80 soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the 0°C to 70°C temperature range, and returning to 25°C. Thermal hysteresis for REF80 reduces significantly from second cycle ownwards as shown in Figure 8-4 and Figure 8-5. Hysteresis can be expressed by Equation 3

Product Folder Links: *REF80*

$$V_{HYST}\left(ppm\right) = \left(\frac{|V_{PRE} - V_{POST}|}{V_{PRE}}\right) \times 10^6 \tag{3}$$

where-

- V_{HYST} = thermal hysteresis (in units of ppm)
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of 0°C to75°C and returns to 25°C.

Figure 8-4. Thermal Hysteresis (Cycle 1) Distribution (0°C to 70°C)

Figure 8-5. Thermal Hysteresis (Cycle 2) Distribution (0°C to 70°C)

8.4 Noise Performance

8.4.1 1/f Noise

1/f noise, also known as flicker noise, is dominant mostly in the lower frequency bands. Flicker noise affects the device output voltage which can affect the ENOB of the signal chain. REF80 data sheet specifies flicker noise for 0.1Hz to 10Hz frequency band where 1/f noise has maximum power. Flicker noise is measured by filtering the output from 0.1Hz to 10Hz. Since the 1/f noise is an extremely low value, the frequency of interest needs to be amplified and band-pass filtered as shown in Figure 8-6. 1/f noise must be tested in a Faraday cage enclosure to block environmental noise. Refer to application note Techniques for Noise Measurements in Precision Series References for more detail on noise measurement for precision series references.
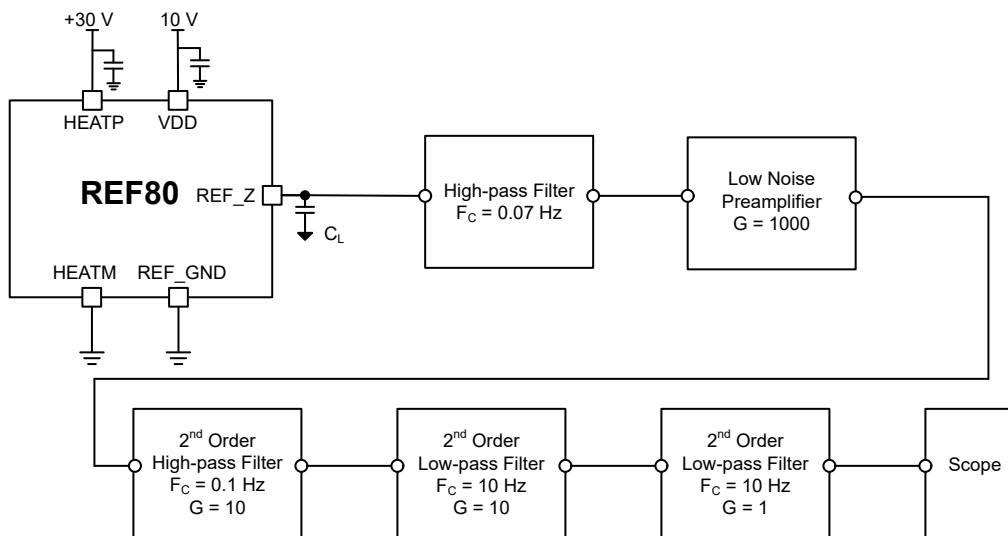
Figure 8-6. 1/f Noise Test Setup

Typical 1/f noise (0.1Hz to 10Hz) distribution can be seen in Figure 8-7.
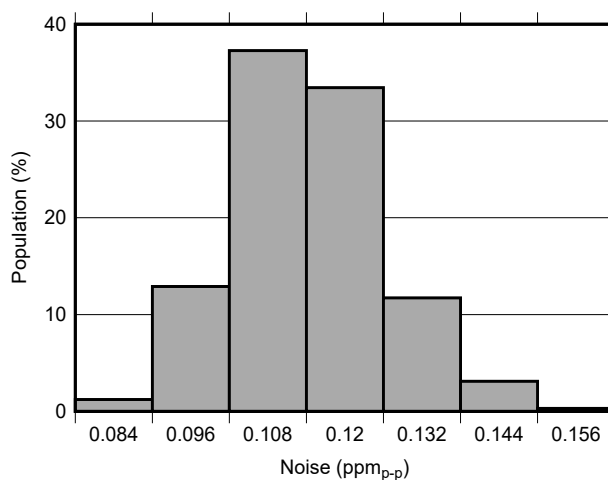

Figure 8-7. 0.1Hz to 10Hz Voltage Noise Distribution

The 1/f noise is in such a low frequency range that it is not practical to filter out which makes it a key parameter for ultra-low noise measurements. Noise sensitive designs must use the lowest 1/f noise for the highest precision measurements. Figure 8-8 shows the effect of 1/f noise over 10s.
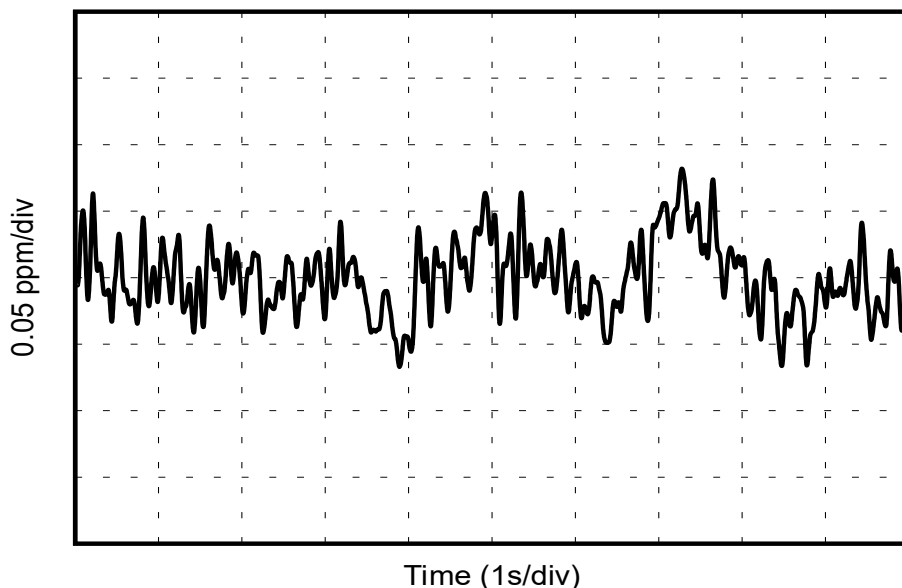
Product Folder Links: *REF80*

Figure 8-8. 0.1Hz to 10Hz REF_Z Noise

8.4.2 Broadband Noise

Broadband noise is a noise that appears at higher frequency compared to 1/f noise. The broadband noise is dominated by white noise as shown in Figure 6-10. The broadband noise is measured by high-pass filtering the output of the REF80 and measuring the result on a spectrum analyzer as shown in Figure 8-9. The DC component of the REF80 is removed by using a high-pass filter and then amplified. When measuring broadband noise, you do not need high gain to achieve maximum bandwidth.
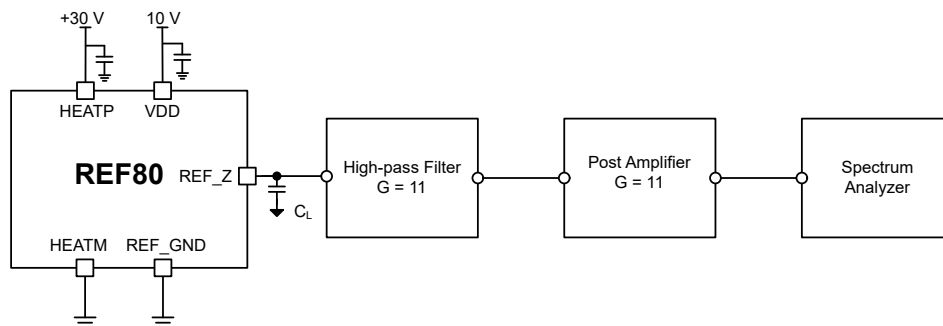

Figure 8-9. Broadband Noise Test Setup

For noise sensitive designs, a low-pass filter can be used to reduce broadband noise output noise levels by removing the high frequency components. When designing a low-pass filter special care must be taken to make sure the output impedance of the filter does not degrade ac performance. This can occur in RC low-pass filters where a large series resistance can impact the load transients due to output current fluctuations.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Basic applications convert the REFZ output to calibration signal or connect to <= 5V signal for precision data converter. The table below shows the typical applications of REF80 and the companion data converter.

APPLICATION	DATA CONVERTER
Test & Measurement	DAC11001B

9.2 Typical Applications

9.2.1 Typical Application: Basic Voltage Reference Connection

The circuit shown in Figure 9-1 shows the basic configuration for the REF80 references. Connect bypass capacitors according to the guidelines in Section 9.4.1.
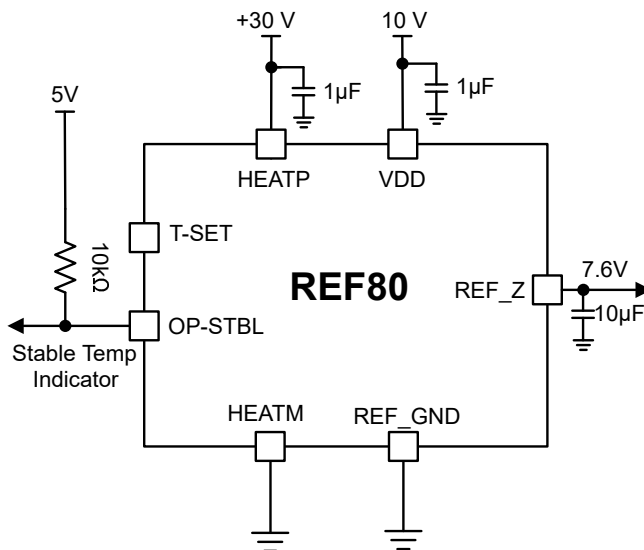

Figure 9-1. Basic Reference Connection

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Product Folder Links: REF80

9.2.1.1 Design Requirements

A detailed design procedure is based on a design example. For this design example, use the parameters listed in Table 9-1 as the input parameters.

Table 9-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{DD}	10V
Heater Voltage VHET (HEATP - HEATM)	30V
Supply decoupling capacitor	1µF
Heater supply decoupling capacitor	1µF
OP-STBL pull-up resistor	10kΩ
OP-STBL pull-up supply	5V

9.2.1.2 Detailed Design Procedure

A bulk capacitor (0.1µF to 10µF) must be connected to the VDD, HEATP and HEATM (when not connected to GND) pins to improve transient response in the applications where the supply voltage can fluctuate. Connect an additional 0.1µF capacitor at VDD, HEATP and HEATM pins closer to the device to bypass high frequency supply noise.

A low ESR (maximum 400mΩ) capacitor of 1µF to 100µF must be connected to the REF_Z pin to provide stable output. For very low noise applications, special care must be taken with X7R and other MLCC capacitors due to the piezoelectric effect. More information on how the piezoelectric effect can be explored in systems can be found in Stress-induced outbursts: Microphonics in ceramic capacitors (Part 1) and Stress-induced outbursts: Microphonics in ceramic capacitors (Part 2) . Designer must use C0G or film capacitors for noise sensitive applications. OP-STBL indicates that the on chip heater is regulating the temperature. Connect a pullup resistor of 10kΩ with suitable logic voltage on this pin. The transient start-up response of the REF80 is shown in REF80 Startup Behavior.
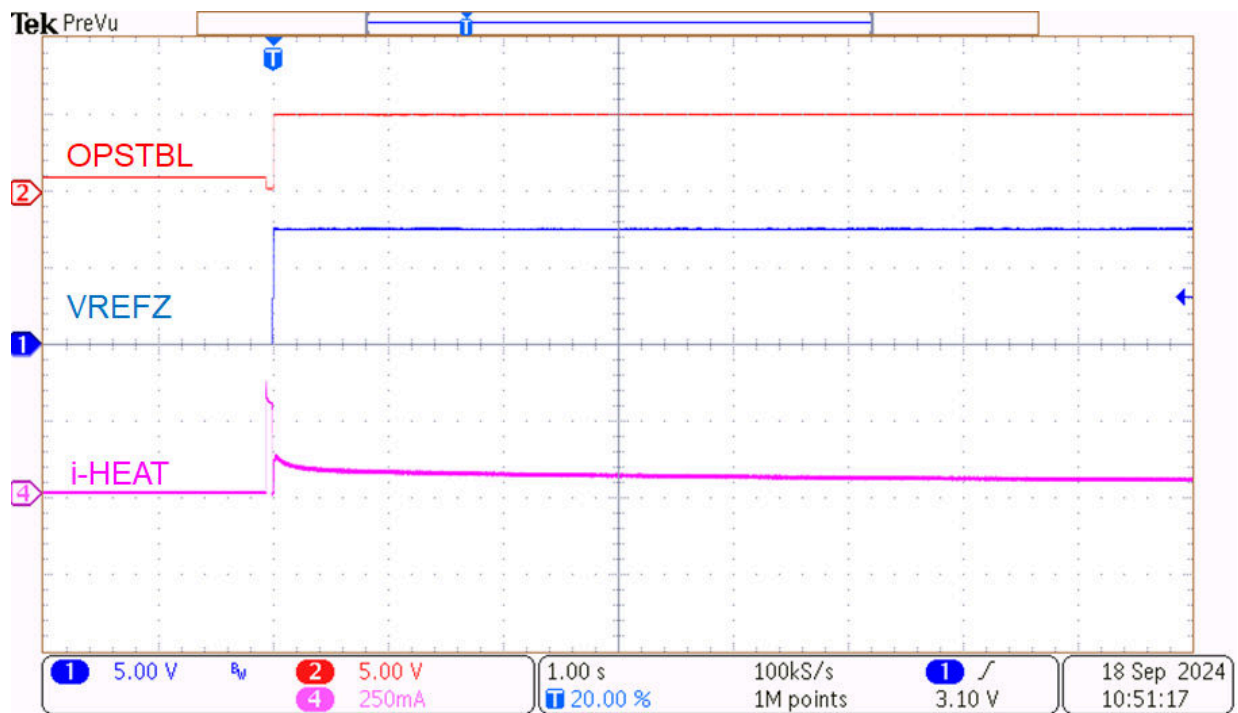
9.2.1.3 Application Curve

Figure 9-2. REF80 Startup Behavior

9.2.2 Typical Application Circuits

9.2.2.1 Precision Voltage Divider Connection

Precision data converters typically require voltage reference which is less than or equal to 5V. REF80 requires a precision resistor divider followed by low noise buffer to generate reference voltage for data converters as shown in Figure 9-3.

The selection of resistor depends on the current capability (< 1mA is preferred) and noise requirement. Minimum value of resistors are decided by the output current as per Equation 4.

$$R1 + R2 \geq 7.6k\Omega \tag{4}$$

Maximum value of the resistors are decided by the noise consideration. Thermal noise of the resistors (parallel equivalent) is added as per Equation 5

$$VREF_{Noise} = \sqrt{\left(\left(\frac{R2}{R1 + R2} \times REF\_Z_{Noise}\right)^2 + \left(R1||R2_{Thermal\ Noise}\right)^2\right)} \tag{5}$$

Where
- $VREF_{Noise}$ = Reference noise requirement in desired frequency band
- REF_Z_{Noise} = REF80 noise in desired frequency band
- $R1||R2_{Thermal\ noise}$ = Thermal noise of parallel equivalent of R1 and R2 resistor

R1 and R2 must be precision foil resistors with matched temperature drift for best performance.
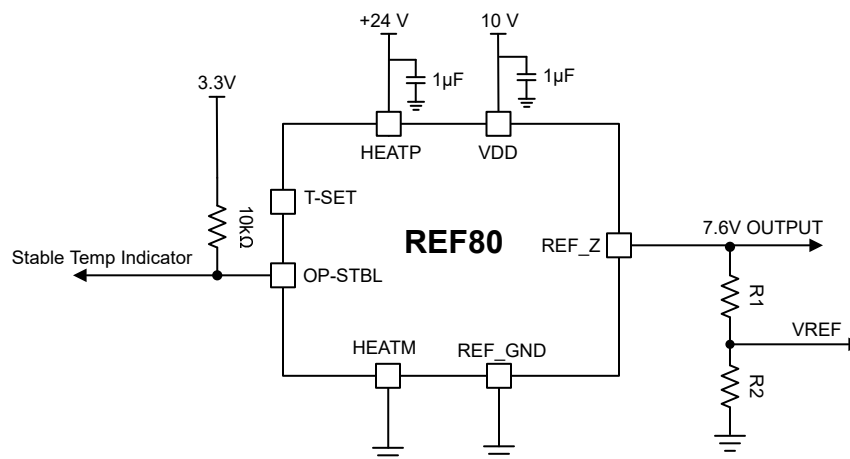

Figure 9-3. Precision Resistor Divider Connection

9.2.2.2 Calibration Signal

Ultra low long term stability and temperature drift makes REF80 an excellent choice for metrology grade calibration signal generation.
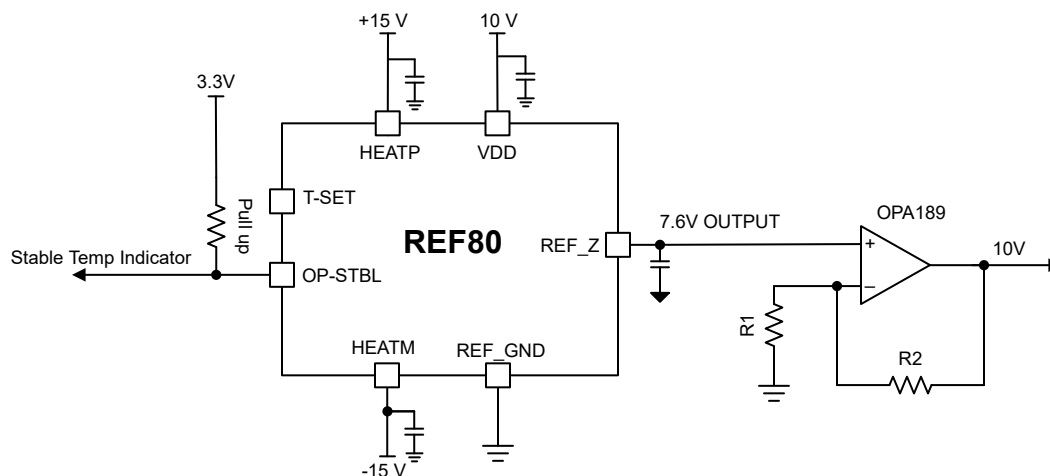
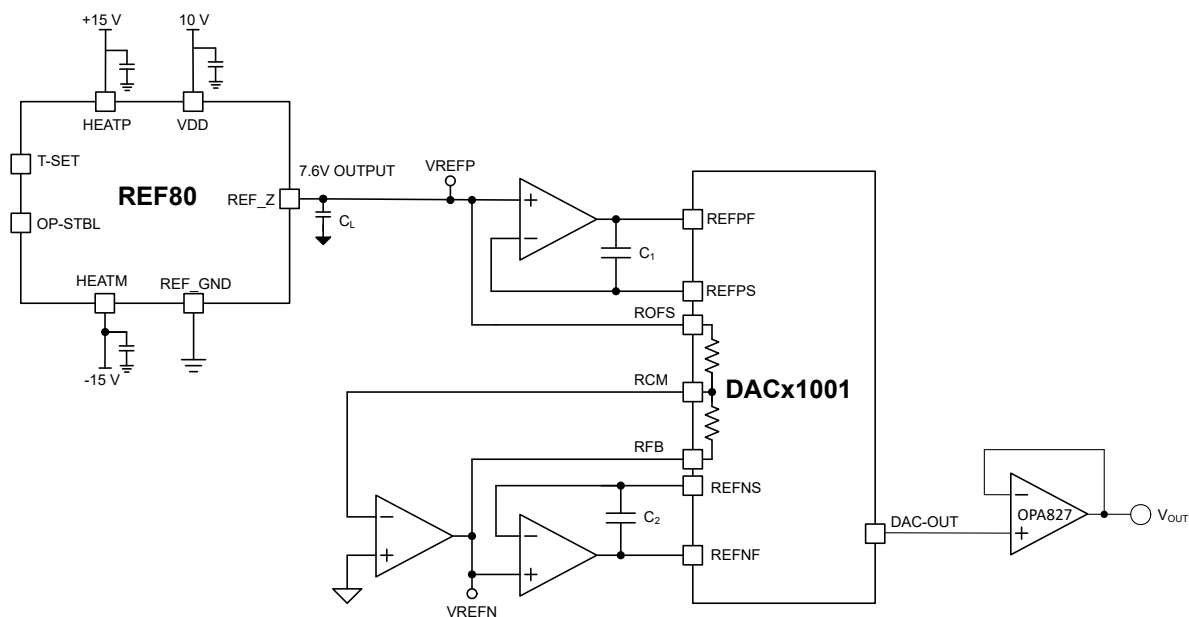**Figure 9-4. 10V Precision Signal With Amplifier And Precision Resistors**

Figure 9-5. Precision Signal With DACx1001

9.3 Power Supply Recommendation

The buried zener reference requires a stable power supply of 10V to 16.5V for stable operation of the REF_Z pin. Potential difference between HEATP and HEATM pin must be 10V to 42V. HEATP must always be connected to a positive supply or ground. HEAM must always be connected to a negative supply or ground. The heater supply must be able to provide high inrush current for fast start-up of the device. TI recommends a supply bypass capacitor ranging between 0.1µF to 10µF.

9.4 Layout

9.4.1 Layout Guidelines

Section 9.4.2 illustrates an example of a PCB layout (two layer routing) for a data acquisition system using the REF80. Some key considerations are:

- **Noise performance**
  - Connect low-ESR, 0.1µF ceramic bypass capacitors at V_{DD}, HEATM and HEATP of the REF80.
  - Connect 10uF to 100uF class 1 capacitor at REF_Z of the REF80.
  - Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.
- **Thermal performance**
  - The layout must minimize the heat dissipation to maintain good thermal resistance for REF80.
  - Use minimum copper to route V_{DD}, REF_Z, REF_GND signal.
  - Use copper as per current requirement for HEATP and HEATM pin.
  - Avoid direct copper pours underneath the package.
  - A shield around the device is recommended to achieve best heater regulation.
- **Seebeck effect**
  - Avoid multiple metal-metal junction to minimize Seebeck effect.
- **Long term stability performance**
  - Provide strain relief directly to pins as shown in the Layout Example.
  - Provide cuts near to the pin, perpendicular to the pins and corners.
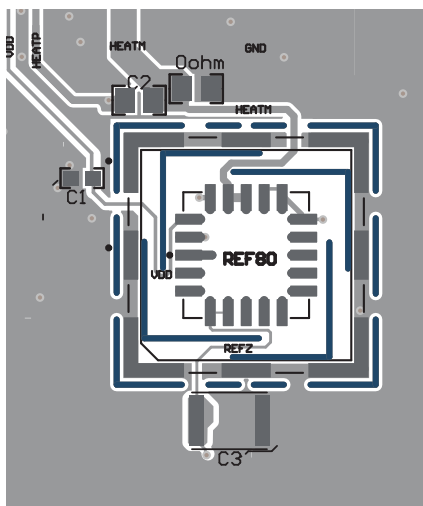 - Avoid single point strain accumulation.

9.4.2 Layout Example

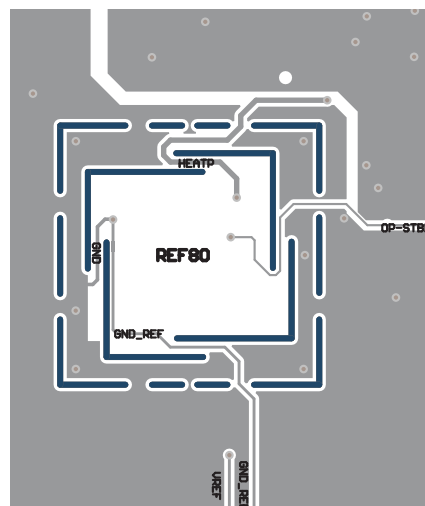**Figure 9-6. Top Layer Layout example for REF80**

Figure 9-7. Bottom Layer Layout example for REF80

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

• Texas Instruments, *Voltage Reference Design Tips For Data Converters*
• Texas Instruments, *Voltage Reference Selection Basics*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF80000B1NAJT	Active	Production	LCCC (NAJ) | 20	250 | SMALL T&R	Yes	Call TI	N/A for Pkg Type	-55 to 125	REF80A1
REF80000B1NAJT.A	Active	Production	LCCC (NAJ) | 20	250 | SMALL T&R	Yes	Call TI	N/A for Pkg Type	-55 to 125	REF80A1

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
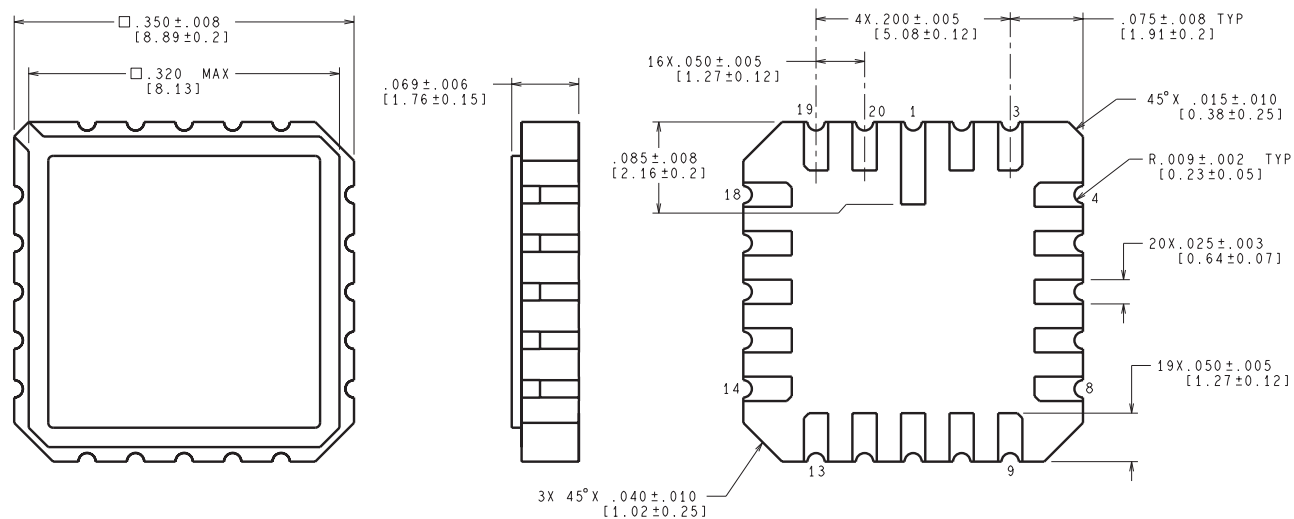
(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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.350±.008
[8.89±0.2]

.320   MAX
[8.13]

.069±.006
[1.76±0.15]

4X.200±.005
[5.08±0.12]

.075±.008 TYP
[1.91±0.2]

16X.050±.005
[1.27±0.12]

.085±.008
[2.16±0.2]

45°X .015±.010
[0.38±0.25]

R.009±.002 TYP
[0.23±0.05]

20X.025±.003
[0.64±0.07]

19X.050±.005
[1.27±0.12]

19 20 1   3

18

14   8

13   9

4

3X 45°X .040±.010
[1.02±0.25]

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