PGA854 Low-Noise, Wide-Bandwidth, Decade Gain, Precision Programmable Gain Instrumentation Amplifier

1 Features

- Eight pin-programmable decade (scope) gains
  - G (V/V) = ½, 1, 2, 5, 10, 20, 50, and 100
- Fully differential outputs
- Output common-mode control
- Low gain error drift: ±2ppm/°C (maximum)
- Faster signal processing:
  - Wide bandwidth: 6.2MHz (G < 10), 2.4MHz (G = 50, 100)
  - Input stage noise: 8.5nV/√Hz at G > 10V/V
  - Filter option to achieve better SNR
- Input overvoltage protection to ±40V beyond supplies
- Input-stage supply range:
  - Single supply: 9V to 36V
  - Dual supply: ±4.5V to ±18V
- Independent output power-supply pins
- Output-stage supply range:
  - Single supply: 4.5V to 36V
  - Dual supply: ±2.25V to ±18V
- Specified temperature range: –40°C to +125°C
- Small package: 3mm × 3mm VQFN

2 Applications

- Factory automation and control
- Analog input module
- Data acquisition (DAQ)
- Test and measurement
- Parametric measurement unit (PMU)

3 Description

The PGA854 is a wide-bandwidth, high-voltage, low-noise programmable gain instrumentation amplifier with differential output. The PGA854 is equipped with eight decade (scope) gain settings, from an attenuating gain of 0.5V/V to a maximum of 100V/V. Gain is set using three digital gain selection pins.

The PGA854 architecture is optimized to drive inputs of high-resolution, precision analog-to-digital converters (ADCs) with sampling rates up to 1MSPS without the need for an additional ADC driver. The output-stage power supplies are decoupled from the input stage to protect the ADC or downstream devices against overdrive damage.

The super-beta input transistors offer an impressively low input bias current, which in turn provides a very low input current noise density of 0.3pA/√Hz, making the PGA854 a versatile choice for virtually any sensor type. The low-noise current-feedback front-end architecture offers exceptional gain flatness even at high frequencies, making the PGA854 an excellent high-impedance sensor readout device. Integrated protection circuitry on the input pins handles overvoltages of up to ±40V beyond the power-supply voltages.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
PGA854	RGT (VQFN, 16)	3mm × 3mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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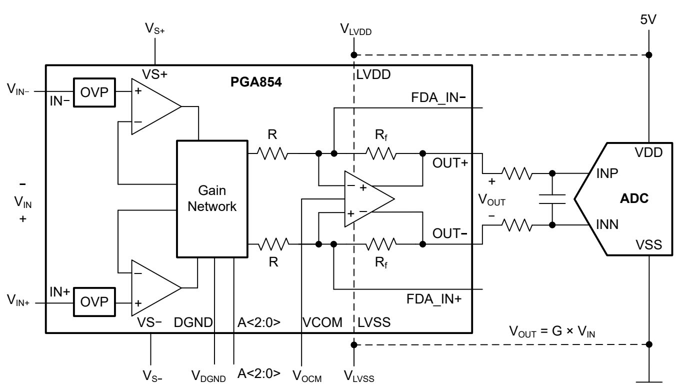
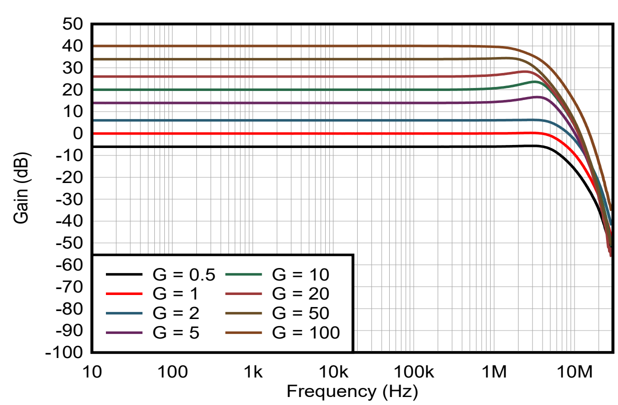


PGA854 Simplified Application



Gain vs Frequency

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4 Device Comparison Table

DEVICE	OUTPUT TYPE	GAIN (V/V)	BANDWIDTH (MHz)	SLEW RATE (V/µs)	NOISE (nV/√Hz)
PGA849	Single-ended	⅛, ¼, ½, 1, 2, 4, 8, 16	10	35	8.6
INA849	Single-ended	$G = 1 + 6k\Omega / R_G$	28	35	1
PGA848	Single-ended	½, 1, 2, 5, 10, 20, 50, 100	6.2	35	8.5
PGA854	Differential	½, 1, 2, 5, 10, 20, 50, 100	6.2	35	8.5
PGA855	Differential	⅛, ¼, ½, 1, 2, 4, 8, 16	10	35	7.8
INA851	Differential	$G = 1 + 6k\Omega / R_G$	22	37	3.2
INA821	Single-ended	$G = 1 + 49.4k\Omega / R_G$	4.7	2	7
INA819	Single-ended	$G = 1 + 50k\Omega / R_G$	2	0.9	8

5 Pin Configuration and Functions

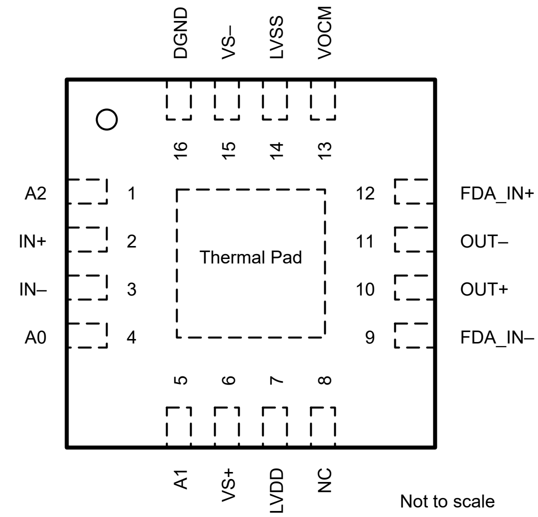

Figure 5-1. RGT Package, 16-Pin VQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A0	4	Input	Gain setting pin 0
A1	5	Input	Gain setting pin 1
A2	1	Input	Gain setting pin 2
DGND	16	Power	Ground reference for digital logic and gain setting pins
FDA_IN–	9	Input	Connection to output driver summing node
FDA_IN+	12	Input	Connection to output driver summing node
IN–	3	Input	Negative (inverting) input
IN+	2	Input	Positive (noninverting) input
LVDD	7	Power	Output driver positive supply. Connect this pin to the positive supply of the ADC to protect from overdriving.
LVSS	14	Power	Output driver negative supply. Connect this pin to the negative supply of the ADC to protect from overdriving.
NC	8	—	Do not connect
OUT–	11	Output	Output (inverting)
OUT+	10	Output	Output (noninverting)
VOCM	13	Input	output common mode control pin
VS+	6	Power	Input stage positive supply
VS–	15	Power	Input stage negative supply
Thermal Pad	Thermal pad	—	Solder the thermal pad to the printed-circuit board (PCB). Connect the thermal pad to a plane or large copper pour that is either floating or electrically connected to VS–. Make this connection even for applications that have low power dissipation.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_S	Supply voltage on VS+, VS– pins; $V_S = (V_{S+}) – (V_{S–})$	0	40	V
V_{SOUT}	Supply voltage on LVDD, LVSS pins; $V_{SOUT} = V_{LVDD} – V_{LVSS}$	0	40	V
	Voltage on power pins LVDD, LVSS	$(V_{S–}) – 0.5$	$(V_{S+}) + 0.5$	V
	Voltage on signal-input pins IN+, IN–	$(V_{S–}) – 40$	$(V_{S+}) + 40$	V
	Voltage on pins DGND, FDA_IN+, FDA_IN–	$(V_{S–}) – 0.5$	$(V_{S+}) + 0.5$	V
	Voltage on gain-select pins A2, A1, A0	$V_{DGND} – 0.5$	$(V_{S+}) + 0.5$	V
V_O	Voltage on output pins OUT+, OUT–	$V_{LVSS} – 0.5$	$V_{LVDD} + 0.5$	V
V_{OCM}	Output common-mode control voltage	$V_{LVSS} – 0.5$	$V_{LVDD} + 0.5$	V
I_O	Output pins OUT+, OUT– current	–100	100	mA
I_{SC}	Output short-circuit current[2]	Continuous		
T_A	Operating temperature	–50	150	°C
T_J	Junction temperature		175	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to V_{SOUT} / 2.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Input stage supply voltage	Single supply	9	36	V
		Dual supply	±4.5	±18	
V_{SOUT}	Output stage supply voltage	Single supply	4.5	36	V
		Dual supply	±2.25	±18	
T_A	Specified temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		PGA854 RGT (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.8	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{OCM} at mid-supply, R_L = 10kΩ, and G = 1V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Differential offset voltage (RTI)	G = 5 to 100			±50	±300	μV
		G = 0.5, 1, 2			±100 / G	±700 / G	
	Differential offset voltage drift (RTI)	T_A = –40°C to +125°C	G > 1		±0.1	±1.0	μV/°C
			G = 0.5, 1		±0.2	±2.0	
PSRR	Power-supply rejection ratio	±4V ≤ V_S ≤ ±18V, RTI	G = 0.5	108	124		dB
			G = 1	114	128		
			G = 2	118	130		
			G ≥ 5	120	134		
z_{id}	Differential input impedance				100 || 1		GΩ || pF
		T_A = –40°C to +125°C		10 || 1			
z_{ic}	Common-mode input impedance				100 || 7		
V_{ICM}	Common-mode input voltage	V_S = ±4.5V to ±18V, T_A = –40°C to +125°C		($V_{S–}$) + 3		(V_{S+}) – 3	V
V_{IN}	Differential input voltage(1)			–20		+20	V
CMRR	Common-mode rejection ratio	At dc to 60Hz, V_{ICM} = ±10V, T_A = –40°C to +125°C, RTI	G = 0.5	69	82		dB
			G = 1	75	88		
			G = 2	81	94		
			G = 5	88	100		
			G = 10	96	106		
			G = 20	102	112		
			G = 50	108	116		
			G = 100	116	124		
BIAS CURRENT							
I_B	Input bias current				±0.5	±2	nA
		T_A = –40°C to +125°C			±1	±3.6	
	Input bias current drift	T_A = –40°C to +125°C				±5	pA/°C
I_{OS}	Input offset current				±0.5	±1	nA
		T_A = –40°C to +125°C			±1	±2	
	Input offset current drift	T_A = –40°C to +125°C				±5	pA/°C

6.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{OCM} at mid-supply, R_L = 10kΩ, and G = 1V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GAIN							
G	Differential gain			0.5		100	V/V
GE	Differential gain error	G = 0.5, 1, 2			±0.005	±0.03	%
		G = 5, 10, 20, 50			±0.015	±0.04	
		G = 100			±0.025	±0.05	
	Differential gain drift	T_A = –40°C to +125°C	G = 2		±0.05	±1	ppm/°C
			G ≠ 2		±0.2	±2	
	Differential gain nonlinearity	G = 0.5 to 20, V_{OUT} = 10V			±2	±5	ppm
		G = 50, 100, V_{OUT} = 10V			TBD	TBD	
		T_A = –40°C to +125°C, V_{OUT} = 10V	G ≤ 20			TBD	
			G = 50, 100			TBD	
OUTPUT							
V_O	Single-ended output voltage	No load, V_{SOUT} = ±2.25V		V_{LVSS} + 0.1		V_{LVDD} – 0.1	V
		R_L = 10kΩ	V_{SOUT} = ±2.25V	V_{LVSS} + 0.2		V_{LVDD} – 0.2	
			V_{SOUT} = ±18V	V_{LVSS} + 0.4		V_{LVDD} – 0.4	
V_{OUT}	Differential output voltage	V_{ICM} and V_{IN} in valid linear operating range(2)			G × V_{IN}		V
C_L	Differential load capacitance	Stable operation for differential load			50		pF
I_{SC}	Short-circuit current	Continuous to V_{SOUT} / 2			±45		mA
			T_A = –40°C to +125°C	±20		±60	
FREQUENCY RESPONSE							
BW	Bandwidth, –3dB	G < 10			6.2		MHz
		G = 10, 20			4.2		
		G = 50, 100			2.4		
SR	Slew rate	G = 0.5 to 100, V_{OUT} > 5V			TBD		V/µs
	Gain switching time				TBD		µs
OUTPUT COMMON-MODE VOLTAGE (V_{OCM}) CONTROL							
V_{OCM}	Output common-mode control voltage(3)	V_S = ±4.5V		V_{LVSS} + 1.5		V_{LVDD} – 1.5	V
		V_S = ±18V		V_{LVSS} + 2		V_{LVDD} – 2	
	Small-signal bandwidth VOCM pin	V_{OCM} = 100mV_{PP}			TBD		MHz
	Large-signal bandwidth VOCM pin	V_{OCM} = 0.6V_{PP}			TBD		MHz
	DC output balance(4)	V_{OCM} fixed at mid-supply (V_{OUT} = ±1V)			95		dB
	Input impedance VOCM pin				250 || 1		kΩ || pF
	V_{OUTCM} offset from mid-supply	VOCM pin floating			±1	±4.5	mV
	V_{OUTCM} offset voltage(5)	V_{OCM} = V_{ICM}, V_{OUT} = 0V			±1	±4.5	mV
	V_{OUTCM} offset voltage drift	V_{OCM} = V_{ICM}, V_{OUT} = 0V, T_A = –40°C to +125°C			±20	±40	µV/°C

6.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{OCM} at mid-supply, R_L = 10kΩ, and G = 1V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT STAGE POWER SUPPLY							
I_{Q_input}	Input stage quiescent current VS+, VS–	V_{IN} = 0V, V_{ICM} = 0V			3	3.7	mA
			T_A = –40°C to +125°C			4.5	
OUTPUT STAGE POWER SUPPLY							
I_{Q_output}	Output stage quiescent current LVDD, LVSS	V_{IN} = 0V, V_{OCM} fixed at mid-supply			2.3	2.8	mA
			T_A = –40°C to +125°C			3.5	
DIGITAL LOGIC							
V_{IL}	Digital input logic low	A0, A1, A2 pins, referred to DGND		V_{DGND}		V_{DGND} + 0.8	V
V_{IH}	Digital input logic high	A0, A1, A2 pins, referred to DGND		V_{DGND} + 1.8		V_{S+}	V
	Digital input pin current	A0, A1, A2 pins			1.5	3	μA
V_{DGND}	DGND voltage			$V_{S–}$		(V_{S+}) – 4	V
	DGND reference current				4	10	μA

(1) Differential Input voltage of the PGA854 amplifier (V_{IN} = V_{IN+} – $V_{IN–}$). The valid input range depends on input common-mode voltage V_{ICM}, gain G, and output common-mode voltage V_{OCM}. See Section 8.1.1.
(2) Differential output voltage V_{OUT} = V_{OUT+} - $V_{OUT–}$ See Section 8.1.1 for valid linear operating range of the amplifier.
(3) V_{OCM} is the Voltage on VOCM pin. Actual output common-mode voltage is calculated from single-ended output voltages V_{OUTCM} = (V_{OUT+} + $V_{OUT–}$) / 2.
(4) DC output balance is defined as |V_{OUTCM}(at V_{IN} = +1) – V_{OUTCM}(at V_{IN} = –1)| / 2.
(5) V_{OUTCM} offset voltage is defined as V_{OUTCM} – V_{OCM}.

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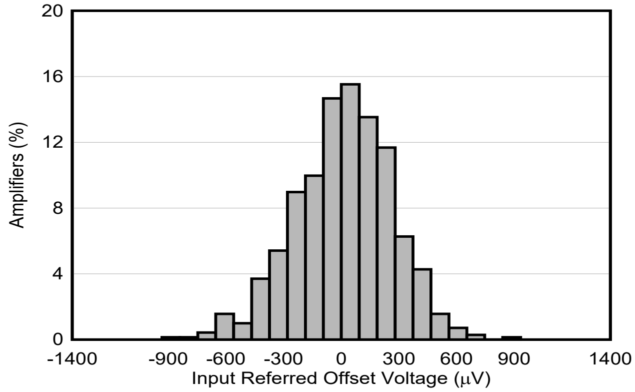
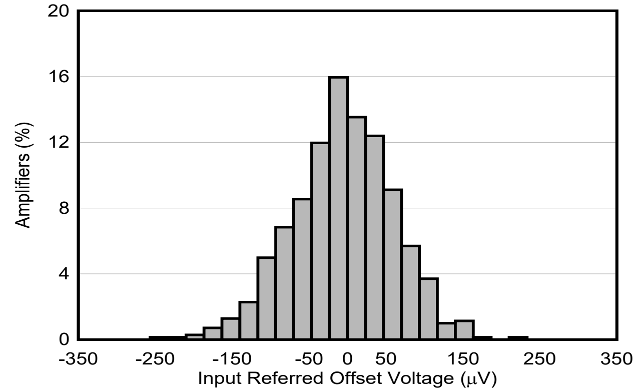
6.6 Typical Characteristics

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{OCM} = 0V, R_L = 10kΩ, and G =1V/V (unless otherwise noted)



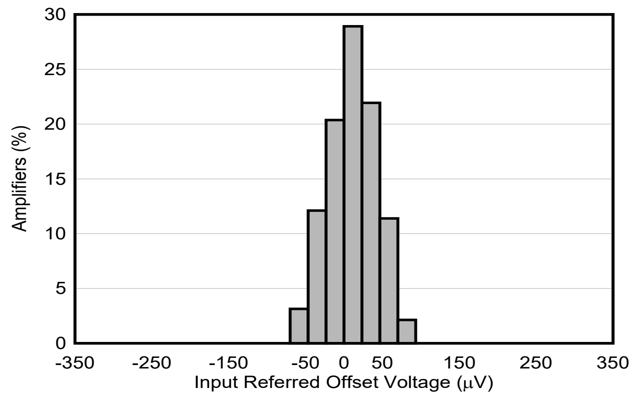
N = 702 Mean = 20.9µV Std. dev. = 253.1µV
G = 0.5V/V

Figure 6-1. Distribution of Offset Voltage (RTI)



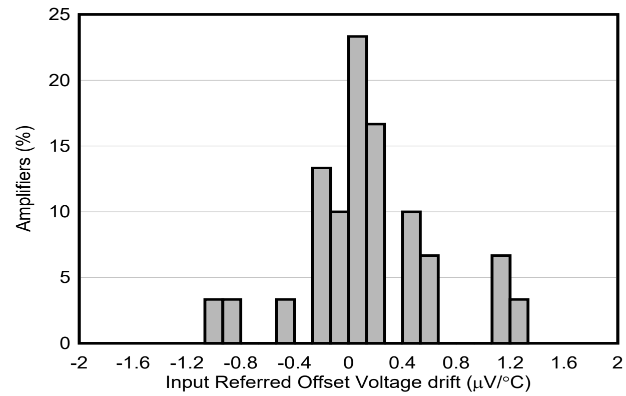
N = 702 Mean = –4.7µV Std. dev. = 66µV
G = 2V/V

Figure 6-2. Distribution of Offset Voltage (RTI)



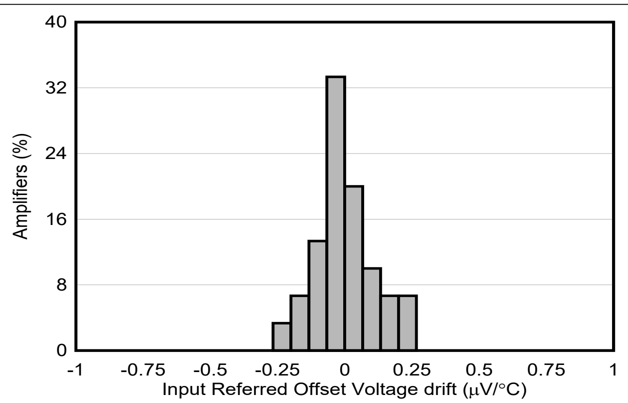
N = 702 Mean = 11µV Std. dev. = 31.1µV
G = 16V/V

Figure 6-3. Distribution of Offset Voltage (RTI)



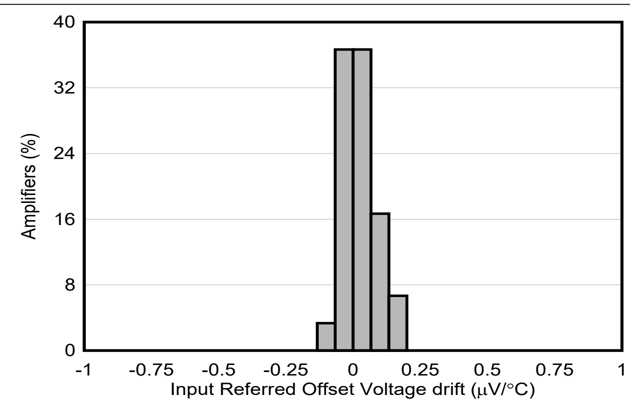
N = 30 Mean = 0.112µV/°C Std. dev. = 0.393µV/°C
G = 0.5V/V

Figure 6-4. Distribution of Offset Voltage Drift (RTI)



N = 30 Mean = –0.02µV/°C Std. dev. = 0.111µV/°C
G = 2V/V

Figure 6-5. Distribution of Offset Voltage Drift (RTI)



N = 30 Mean = 0.022µV/°C Std. dev. = 0.065µV/°C
G = 100V/V

Figure 6-6. Distribution of Offset Voltage Drift (RTI)

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{OCM} = 0V, R_L = 10kΩ, and G =1V/V (unless otherwise noted)

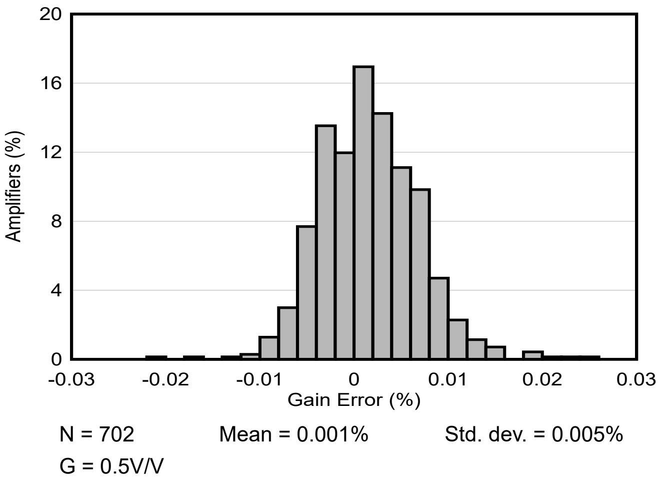


Figure 6-7. Distribution of Gain Error

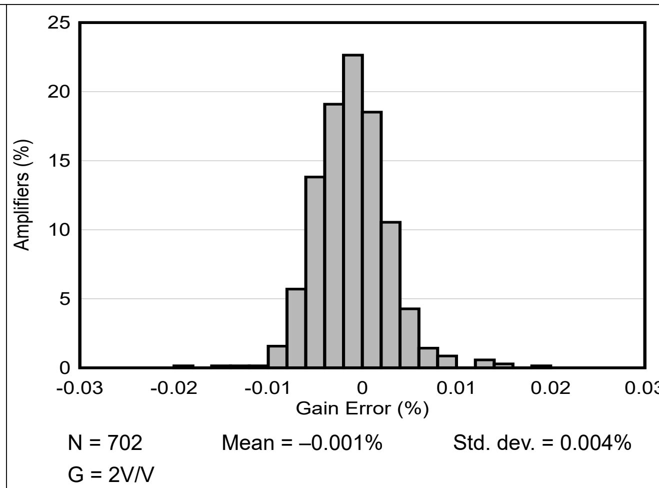


Figure 6-8. Distribution of Gain Error

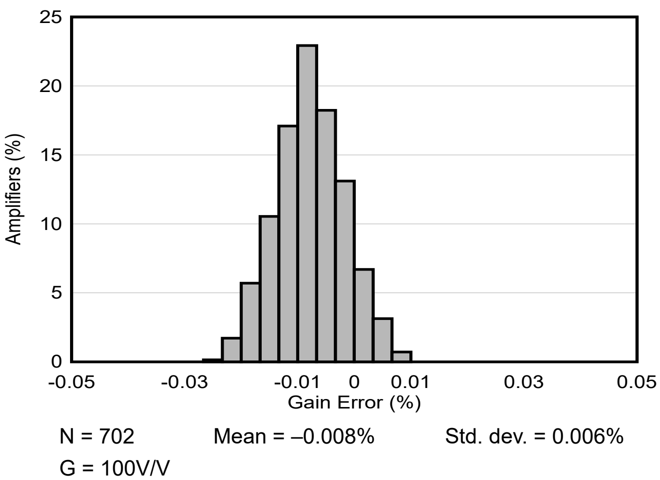


Figure 6-9. Distribution of Gain Error

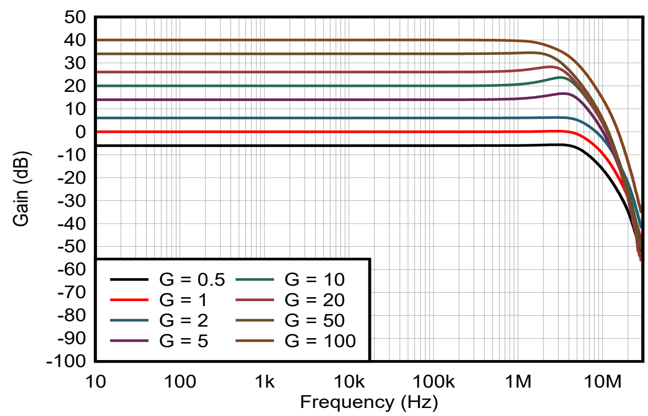


Figure 6-10. Gain vs Frequency

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7 Detailed Description

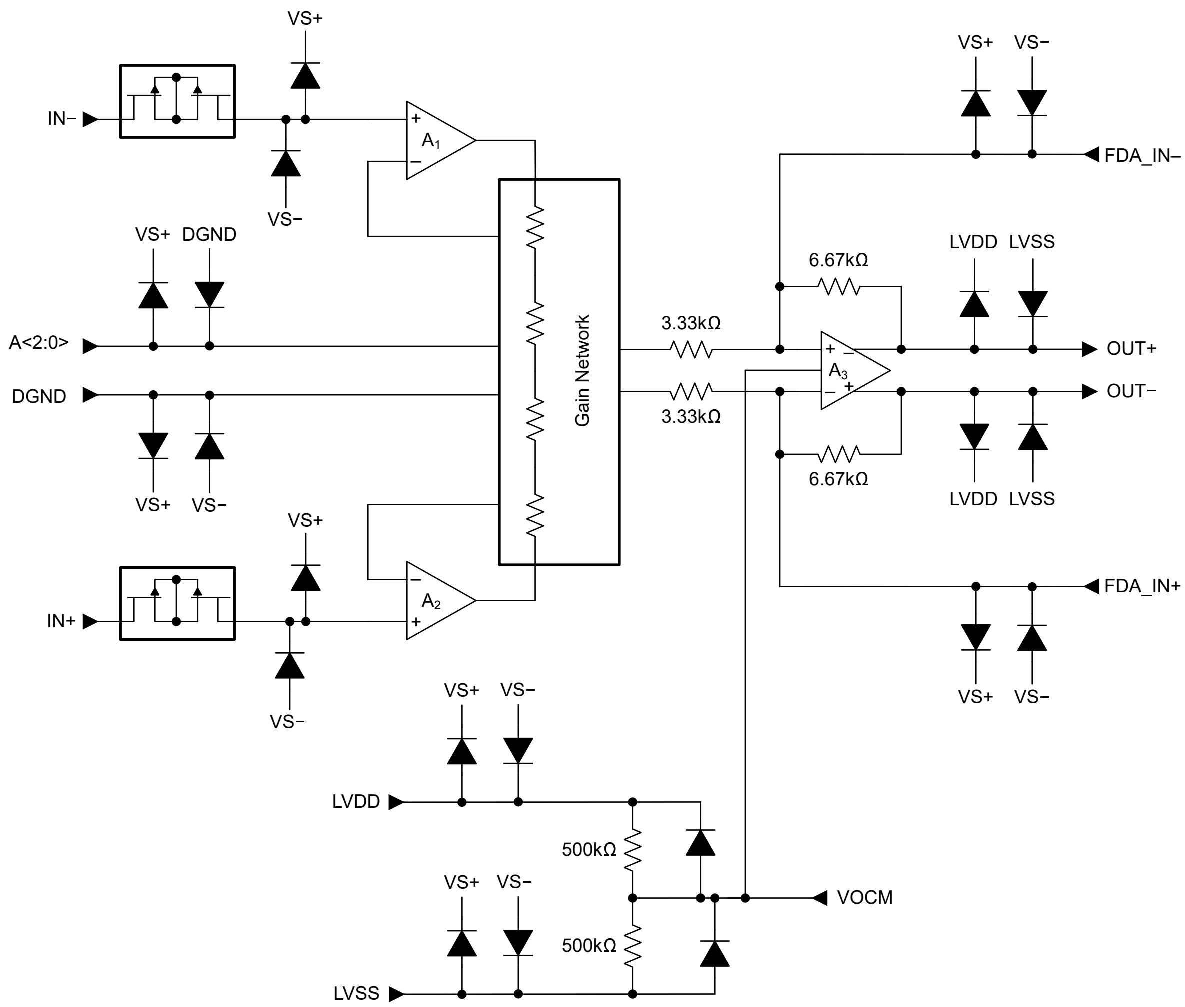
7.1 Overview

The PGA854 is a monolithic, high-voltage, precision programmable-gain instrumentation amplifier. The PGA854 combines a high-speed current-feedback input stage with an internally matched gain resistor network, followed by a four-resistor, difference amplifier output stage. Eight preprogrammed decade gains are selectable using gain-select pins A0, A1, A2. Gains range from 0.5V/V to 100V/V; see also Section 7.3.1.

A functional block diagram for the PGA854 is shown in the next section. The differential input voltage is fed into a pair of matched, high-impedance input, current-feedback amplifiers. An integrated precision-matched gain resistor network is used to amplify the differential input voltage. An output difference amplifier, A_3, rejects the input common-mode component and refers the output signal to the voltage level set by the VOCM pin.

The PGA854 output amplifier bandwidth is optimized to drive high-performance analog-to-digital converters (ADCs) with sampling rates up to 1MSPS without additional ADC drivers. The output amplifier uses a separate power supply that is independent of the input-stage power supply. When driving an ADC, use a low-impedance connection from LVDD and LVSS to the ADC power supplies. This configuration protects the ADC inputs from damage resulting from inadvertent overvoltage conditions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Gain Control

The PGA854 uses three pins to set the amplifier gain. These gain select pins are set with respect to DGND. This configuration simplifies the design when compared to programmable-gain amplifiers requiring a SPI or other digital interface options for gain changes. Figure 7-1 shows the gain-setting block diagram. Table 7-1 lists the gain options. Any gain select pin that is not driven by an external source is automatically biased at DGND using internal pull-down options.

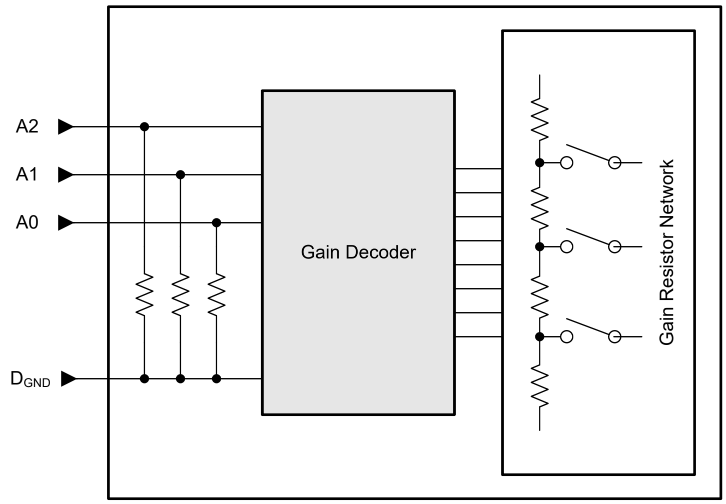


Figure 7-1. PGA854 Gain Setting Block Diagram

Table 7-1. Gain Options

A2:A0	GAIN
000	0.5
001	1
010	2
011	5
100	10
101	20
110	50
111	100

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7.3.2 Input Protection

The inputs of the PGA854 are individually protected for voltages up to ±40V beyond either supply. For example, an input common-mode voltage anywhere between –55V and +55V does not cause damage when powered from ±15V supplies. Internal circuitry on each input provides low series impedance under normal signal conditions, thus maintaining high performance under normal operating conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 4.8mA. Figure 7-2 shows the input protection functionality during an overvoltage condition on IN+ or IN- inputs.

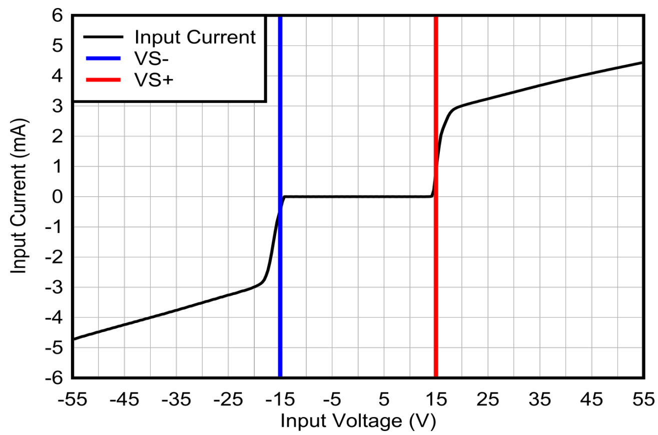

Figure 7-2. Input Current vs Input Overvoltage

Figure 7-3 shows that during an input overvoltage condition, current flows through the input protection diodes into the power supplies. In applications where the power supplies are unable to sink current, place Zener diode clamps (ZD1 and ZD2) on the power supplies to provide a current pathway to ground.

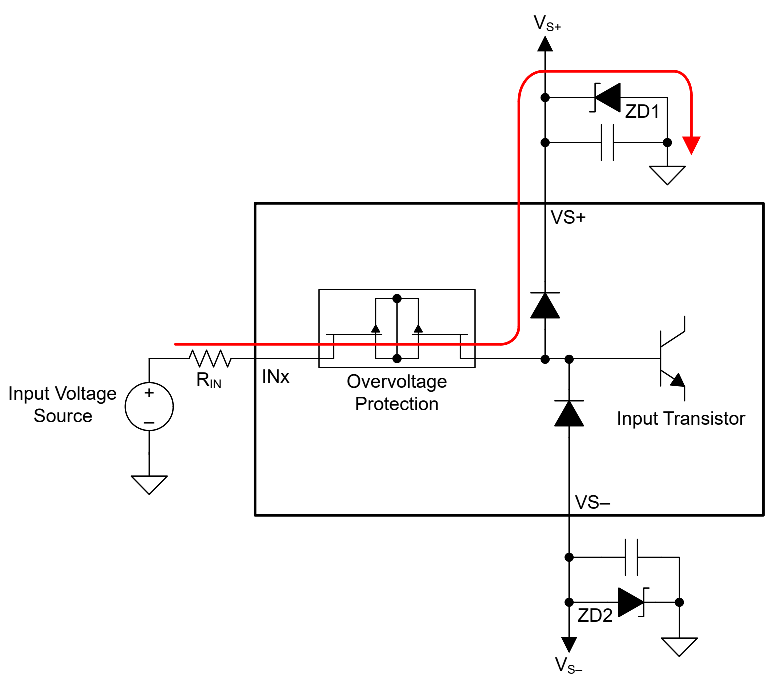

Figure 7-3. Input Current Path During an Overvoltage Condition

7.3.3 Output Common-Mode Pin

The output voltages of the PGA854 are balanced with respect to the voltage on the output common-mode pin, VOCM. The starting point for most designs is to assign an output common-mode voltage for the PGA854. For ac-coupled signal paths, this voltage is often the default mid-supply voltage, so as to retain the most available output swing around the voltage centered at VOCM. For dc-coupled signal paths, set this voltage between a maximum of V_{LVDD} – 1.5V and minimum of V_{LVSS} + 1.5V. For precision ADC applications, this voltage is typically the input common-mode voltage of the ADC.

The voltage at the VOCM pin is internally buffered to bias the fully differential output amplifier, eliminating the need for an external VOCM buffer. In the event that the VOCM pin is left floating, the output common-mode control voltage is biased at output mid-supply using an internal 500kΩ-500kΩ resistor divider network connected between the output-stage power-supply pins.

7.3.4 Using the Fully Differential Output Amplifier to Shape Noise

Section 7.2 shows that the PGA854 output-stage fully-differential amplifier uses 6.67kΩ feedback resistors between the OUT+ output and the inverting input, and the OUT– output and the noninverting input. External direct access to inverting input is provided through the FDA_IN+ pin, and to the noninverting input through the FDA_IN- pin. This option allows circuit designers to add external feedback capacitors in parallel with the internal feedback resistors to implement noise-filtering or noise-shaping techniques. These pins are also usable to implement customized attenuating gains for the output stage. Consider the following important factors when designing parallel circuits with the internal feedback resistors:

- The accuracy of the internal resistor network is 0.01% or better. This accuracy results in a common-mode rejection ratio (CMRR) of 80dB or better. Mismatched leakage currents on these pins potentially causes CMRR degradation.
- The internal resistors have ±15% absolute resistance variation; consider this variation when implementing custom attenuating gains or noise filters.

CAUTION

Do not treat these pins as outputs, nor use the pins to source or sink current. Excessive currents through the feedback resistors potentially cause permanent damage to internal circuitry.

7.4 Device Functional Modes

The PGA854 has a single functional mode and operates when the input-stage power supply is greater than ±4.5V (9V) and the output-stage power supply is greater than ±2.25V (4.5V); see also Section 6.3.

ADVANCE INFORMATION

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

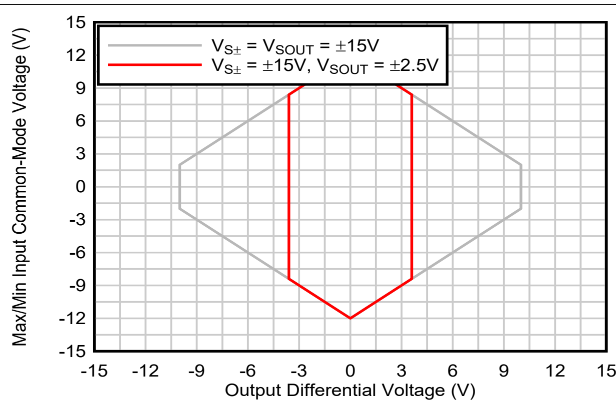
The PGA854 is a monolithic, high-voltage, high-bandwidth, precision programmable gain instrumentation amplifier with fully differential outputs. The PGA854 combines a high-speed current-feedback input stage with an internally matched gain resistor network, followed by a four-resistor, differential amplifier output stage. The PGA854 is equipped with eight decade-gain settings, from 0.5V/V to 100V/V, using three digital gain-selection pins: A0, A1, and A2.

The PGA854 is designed for applications such as factory automation and control, analog input modules, data acquisition, test and measurement, and semiconductor test.

8.1.1 Linear Operating Input Range

The linear operating input voltage range of the PGA854 input circuitry extends within 3V (maximum) of either power supply. This device maintains excellent common-mode rejection throughout this range at all temperatures. The linear operating input common-mode range is a function of the input common-mode voltage, input differential voltage, gain, and output common-mode voltage.

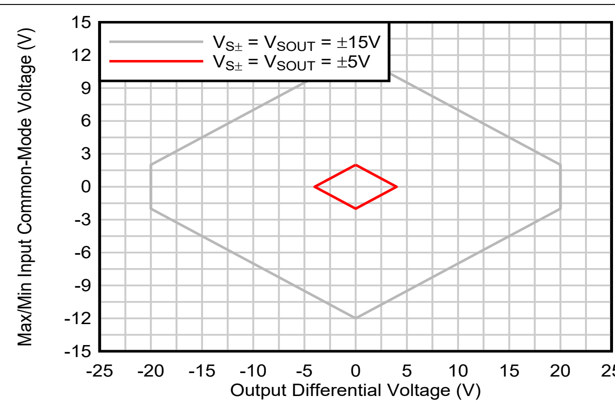
Figure 8-1 to Figure 8-4 show the valid common-mode range to enable valid output voltage at no load condition.



V_S = V_{SOUT} = ±15V, V_{OCM} = 0V

V_S = ±15V, V_{SOUT} = ±5V G = 0.5V/V

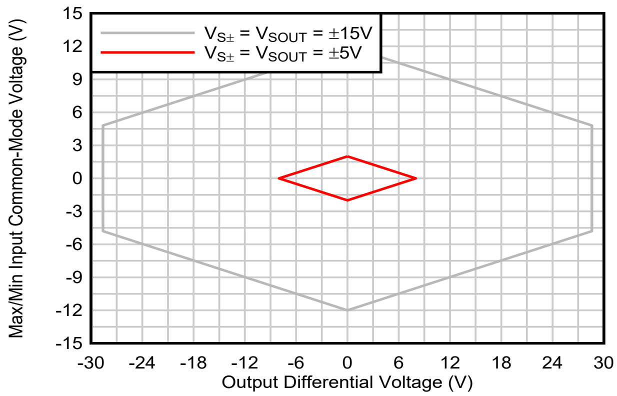
Figure 8-1. Input Common-Mode Voltage vs Output Differential Voltage



V_S = V_{SOUT} = ±15V, V_{OCM} = 0V

V_S = V_{SOUT} = ±5V, G = 1V/V

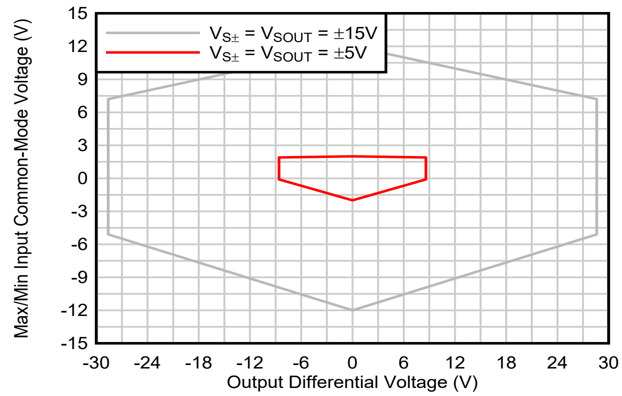
Figure 8-2. Input Common-Mode Voltage vs Output Differential Voltage



$V_S = V_{SOUT} = \pm15V$, $V_{OCM} = 0V$

$V_S = V_{SOUT} = \pm5V$, G = 2V/V

Figure 8-3. Input Common-Mode Voltage vs Output Differential Voltage



$V_S = V_{SOUT} = \pm15V$, $V_{OCM} = 0V$

$V_S = V_{SOUT} = \pm5V$, G = 100V/V

Figure 8-4. Input Common-Mode Voltage vs Output Differential Voltage

8.2 Typical Application

8.2.1 ADS127L11 and ADS127L21, 24-Bit, Delta-Sigma ADC Driver Circuit

The application circuit in Figure 8-5 shows a schematic for a 24-bit wide-bandwidth, delta-sigma ADC. The ADS127Lx1 ADC offers two digital filters to optimize ac applications (wideband filter) or dc applications (sinc4 filter). Table 8-2 and Table 8-3 show measurement results in both filter settings. For a detailed design procedure to operate the ADS127Lx1 ADC, see the ADS127Lx1EVM-PDK evaluation module user's guide.

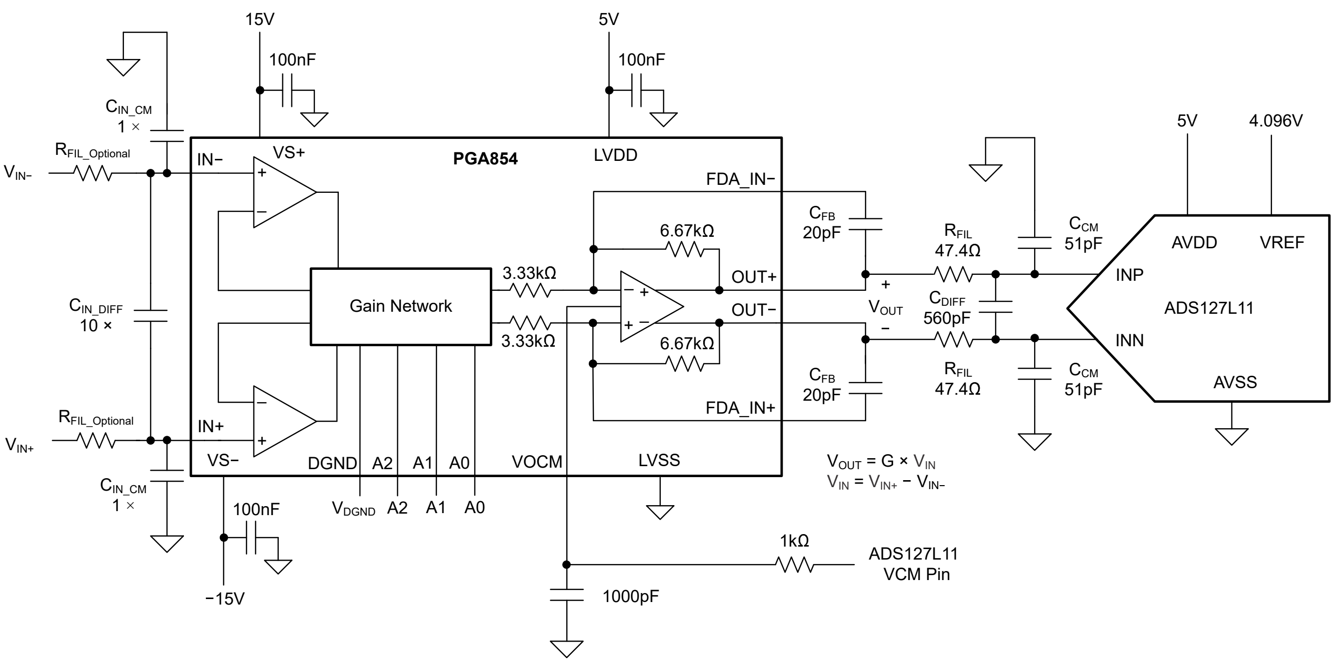


Figure 8-5. Driving the ADS127Lx1 Delta-Sigma ADC

ADVANCE INFORMATION

8.2.2 Design Requirements

The design requirements for the application driving the ADS127Lx1 ADC are listed in Table 8-1.

Table 8-1. Design Parameters

PARAMETER	VALUE
Differential-to-differential conversion	V_{IN} to V_{OUT}
Supply voltages	$V_{S\pm}$ = ±15V, V_{LVDD} = 5V, V_{LVSS} = GND, VREF = 4.096V
Full-scale range of ADC	FSR = ± 4.096V
Data rate of ADC	f_{DATA} = 187.5kSPS
ADC filter configuration	(1) High-speed mode, Sinc4 filter, OSR = 64
	(2) High-speed mode, Wideband filter, OSR = 64
Signal frequency	Tested at f_{IN} = 1kHz
RC kickback filter(1)	R_{FIL} = 47.4Ω, C_{DIFF} = 560pF, C_{CM} = 51pF

(1) Consider a trade-off between THD, frequency response, and drift. The differential current drift into the ADC can interact with the filter resistors and result in higher drift errors. However, lower resistance degrades the phase margin of the PGA854. For low drift applications, keep R_{FIL} < 50Ω.

8.2.3 Detailed Design Procedure

Table 8-2 and Table 8-3 show the typical signal-to-noise (SNR) and total harmonic distortion (THD) of the PGA854 driving the ADS127Lx1 delta-sigma ADC using a sinc4 or wideband filter. For a list of the equivalent input voltage amplitude signals for the different PGA854 gain configurations, see Table 8-2 and Table 8-3. At gain = 1V/V, the design achieves –102.4dB THD and 108.9dB SNR.

Table 8-2. PGA854 and ADS127Lx1 FFT Data Summary, OSR = 64, Sinc4 Filter

PGA GAIN (V/V)	INPUT AMPLITUDE (V_{PP})	SNR (dB)	THD (dB)	ENOB (Bits)
0.5	16.012	106.2	–101.9	16.4
1	8.006	107.3	–102.4	16.5
2	4.002	105.9	–101.9	16.4
5	1.601	101.3	–102.3	16.1
10	0.8	94.7	–101.8	15.3
20	0.4	88.7	–101.5	14.4
50	0.16	79.9	–98.4	13.0
100	0.081	75.6	–93.5	12.2

Table 8-3. PGA854 and ADS127Lx1 FFT Data Summary, OSR = 64, Wideband Filter

PGA GAIN (V/V)	INPUT AMPLITUDE (V_{PP})	SNR (dB)	THD (dB)	ENOB (Bits)
0.5	16.012	108.3	–101.9	16.5
1	8.006	108.9	–102.4	16.6
2	4.002	108.5	–102.0	16.5
5	1.601	107.7	–102.3	16.5
10	0.8	105.5	–101.8	16.4
20	0.4	100.3	–101.7	16.0
50	0.16	91.4	–97.1	14.7
100	0.081	87.1	–95.5	14.1
100	0.081	87.1	–95.5	14.1

The R-C-R differential low-pass filter at the input of the instrumentation amplifier helps reduce EMI/RFI high-frequency extrinsic noise. This filter is customizable per the bandwidth and application requirements. This design example (see Figure 8-5) suggests a filter with the capacitor ratio of C_{IN_DIFF} = 10 × C_{IN_CM}. Using the 10:1 ratio for differential capacitor C_{IN_DIFF} versus common-mode capacitors C_{IN_CM} offers good differential and common-mode noise rejection. This arrangement tends to be less sensitive to the tolerance variation and mismatch of the filter capacitors.

The feedback capacitor, C_{FB}, is in parallel with the PGA854 output-stage 6.67kΩ feedback resistors to help implement additional noise filtering. The internal resistors have ±15% absolute resistance variation; take this variation into account when implementing noise filtering. In this example, C_{FB} is set to 20pF, providing a typical $f_{–3dB}$ corner frequency of 1.19MHz. The estimated minimum $f_{–3dB}$ corner frequency for this circuit is approximately 988kHz when accounting for the feedback-resistor variation.

The filter at the ADS127Lx1 inputs works as a charge reservoir to filter the sampled input of the ADC. The charge reservoir reduces the instantaneous charge demand of the amplifier, maintaining low distortion and low gain error that otherwise potentially degrade because of incomplete amplifier settling. The ADC input filter values are R_{FIL} = 47.4Ω, C_{DIFF} = 560pF, and C_{CM} = 51pF. The ADC input precharge buffers significantly reduce the sample-phase input charge that raises the ADC input impedance to decrease gain error.

High-grade COG (NPO) are used everywhere in the signal path ($C_{IN\_DIFF,}$ $C_{IN\_CM,}$ C_{FB}, C_{DIFF}, C_{CM}) for low distortion. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance accuracy. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

8.3 Power Supply Recommendations

The nominal performance of the PGA854 is specified with input-stage supply and output-stage supply voltages of ±15V, and V_{ICM} and V_{OCM} at mid-supply. Within the specified limits, custom input common-mode and output common-mode voltages are usable without compromising performance; see also Section 6.3. To prevent damage to internal circuitry, the output-stage power supplies are clamped to stay within the input-stage supply voltage levels; see also Section 7.2.

CAUTION

Supply voltages greater than 40V (±20V) permanently damage the device.

8.4 Layout

8.4.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- To avoid converting common-mode signals into differential signals and thermal electromotive forces (EMFs), verify both input paths are symmetrical and well-matched for source impedance and capacitance.
- Noise potentially propagates into analog circuitry through the power pins of the device and of the circuit as a whole. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Leakage on the FDA_IN+ and FDA_IN– pins potentially causes a dc offset error in the output voltages. Additionally, excessive parasitic capacitance at these pins potentially results in decreased phase margin and affects the stability of the output stage. If these pins are not used to implement deliberate capacitive feedback, follow best practices to minimize leakage and parasitic capacitance.
- Follow best practices to minimize leakage and parasitic capacitance, which includes implementing *keep-out* areas in any ground planes located immediately below the input pins.
- Minimize the number of thermal junctions. If possible, route the signal path using a single layer without vias.
- Keep sufficient distance from major thermal energy sources (circuits with high power dissipation). If not possible, place the device so that the thermal energy source effects on both sides of the differential signal path are evenly matched.
- Keep the traces as short as possible.

8.4.2 Layout Example

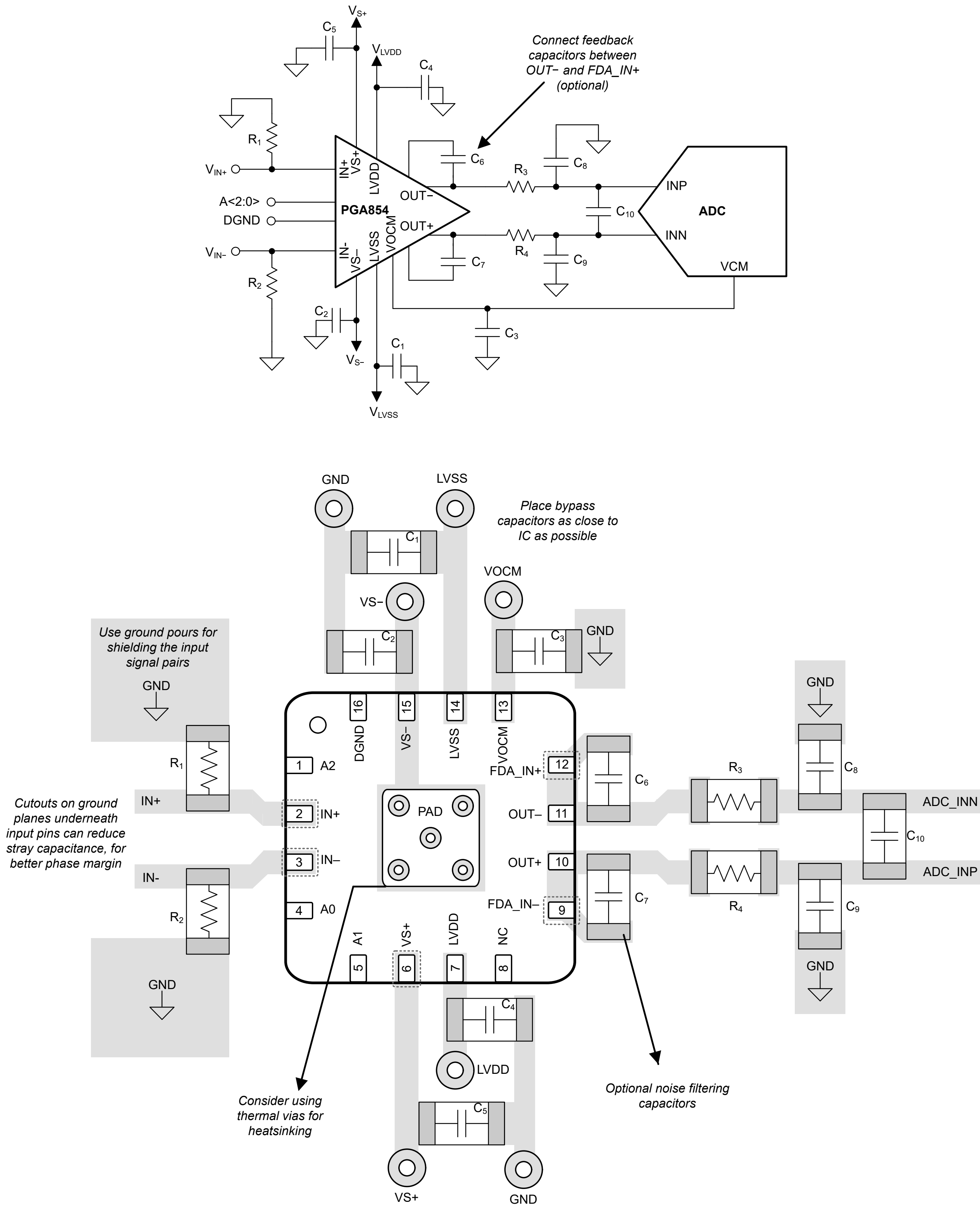


Figure 8-6. Example Schematic and Associated PCB Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

9.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design and simulation tools web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Comprehensive Error Calculation for Instrumentation Amplifiers application note*
- Texas Instruments, *Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications application note*

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XPGA854RGTR	Active	Preproduction	VQFN (RGT) | 16	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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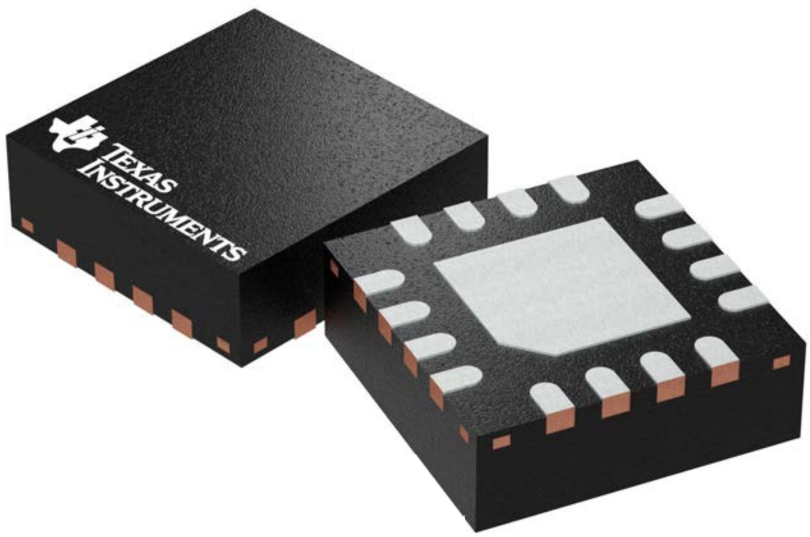

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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