

PCA9545A Low Voltage 4-channel I²C and SMbus Switch With Interrupt Logic and **Reset Functions**

1 Features

- 1-of-4 Bidirectional Translating Switches
- I²C Bus and SMBus Compatible
- Four Active-Low Interrupt Inputs
- **Active-Low Interrupt Output**
- Active-Low Reset Input
- Two Address Terminals, Allowing up to Four Devices on the I²C Bus
- Channel Selection via I²C Bus, in Any Combination
- Power-Up With All Switch Channels Deselected
- Low R_{ON} Switches
- Allows Voltage-Level Translation Between 1.8-V, 2.5-V, 3.3-V, and 5-V Buses
- No Glitch on Power-Up
- Supports Hot Insertion
- Low Standby Current
- Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
- 5.5 V Tolerant Inputs
- 0 to 400-kHz Clock Frequency
- Latch-Up Performance Exceeds 100 mA per JESD
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Servers
- Routers (Telecom Switching Equipment)
- **Factory Automation**
- Products With I²C Slave Address Conflicts (For Example, Multiple, Identical Temp Sensors)

3 Description

The PCA9545A is a quad bidirectional translating switch controlled via the I2C bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCn/SDn channel or combination of channels can be selected, determined by the contents of the programmable control register. Four interrupt inputs (INT3- INT0), one for each of the downstream pairs, are provided. One interrupt (INT) output acts as an AND of the four interrupt inputs.

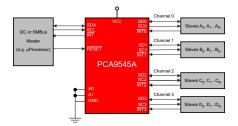
An active-low reset (RESET) input allows the PCA9545A to recover from a situation in which one of the downstream I2C buses is stuck in a low state. Pulling RESET low resets the I²C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed such that the VCC terminal can be used to limit the maximum high voltage, which will be passed by the PCA9545A. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5 V tolerant.

Device Information

| PART NUMBER PACKAGE ⁽¹⁾ BODY SIZE (NO | | | | | | | | |
|--|------------------|-------------------|--|--|--|--|--|--|
| PART NUMBER | PACKAGE | BODT SIZE (NOW) | | | | | | |
| | TVSOP (DGV) (20) | 5.00 mm x 4.40 mm | | | | | | |
| | SOIC (DW) (20) | 12.8 mm x 7.50 mm | | | | | | |
| | TSSOP (PW) (20) | 6.50 mm x 4.40 mm | | | | | | |
| PCA9545A | VQFN (RGW) (20) | 5.00 mm x 5.00 mm | | | | | | |
| | VQFN (RGY) (20) | 4.50 mm x 3.50 mm | | | | | | |
| | BGA (GQN) (20) | 4.00 mm x 4.00 mm | | | | | | |
| | BGA (ZQN) (20) | 4.00 mm x 3.00 mm | | | | | | |

For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application Diagram



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4 Revision History

| С | hanges from Revision June 2014 (D) to Revision E (March 2021) | Page |
|---|---|------|
| • | Changed the Device Information table | 1 |
| • | Moved T _{stq} to the Absolute Maximum Ratings | |
| • | Moved the Package thermal impedance to the <i>Thermal Information</i> table | |
| • | Added the Thermal Information table | 4 |
| • | Changed the V _{PORR} row in the <i>Electrical Characteristics</i> | |
| • | Added V _{PORF} row to the <i>Electrical Characteristics</i> | |
| • | Changed the I _{CC} Low inputs and High inputs values in the <i>Electrical Characteristics</i> | |
| • | Changed the ΔI_{CC} ($\overline{INT3}$ – $\overline{INT0}$) MAX values From: 15 μ A To: 20 μ A in the <i>Electrical Characteristics</i> | |
| • | Changed the R _{on} (4.5 V to 5.5 V) TYP value From: 9 Ω To: 10 Ω in the <i>Electrical Characteristics</i> | |
| • | Changed the R _{on} (3 V to 3.6 V) TYP value From: 11 Ω To: 13 Ω in the <i>Electrical Characteristics</i> | |
| • | Changed Note (2) in the Electrical Characteristics | |
| • | Changed the Application Curves | |
| • | Changed the Power Supply Recommendations | |
| C | hanges from Revision October 2006 (C) to Revision D (February 2014) | Page |
| _ | Added Added RESET Errata section | 12 |

5 Pin Configuration and Functions

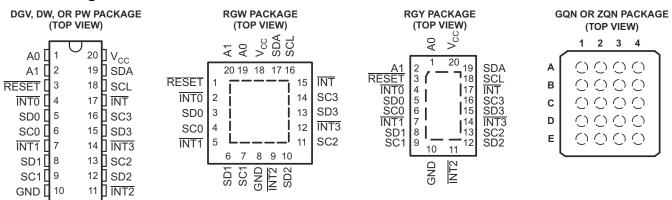


Table 5-1. Pin Functions

| | PI | N | | |
|-------|-------------------------|-----|-------------|--|
| NAME | DGV, DW, PW, AND RGY | RGW | GQN AND ZQN | DESCRIPTION |
| A0 | 1 | 19 | A2 | Address input 0. Connect directly to V _{CC} or ground. |
| A1 | 2 | 20 | A1 | Address input 1. Connect directly to V _{CC} or ground. |
| RESET | 3 | 1 | В3 | Active-low reset input. Connect to V _{DPUM} ⁽¹⁾ through a pull-up resistor, if not used. |
| ĪNT0 | 4 | 2 | B1 | Active-low interrupt input 0. Connect to $V_{DPU0}^{\ (1)}$ through a pull-up resistor. |
| SD0 | 5 | 3 | C2 | Serial data 0. Connect to V _{DPU0} ⁽¹⁾ through a pull-up resistor. |
| SC0 | 6 | 4 | C1 | Serial clock 0. Connect to V _{DPU0} ⁽¹⁾ through a pull-up resistor. |
| ĪNT1 | 7 | 5 | D3 | Active-low interrupt input 1. Connect to V _{DPU1} ⁽¹⁾ through a pull-up resistor. |
| SD1 | 8 | 6 | D1 | Serial data 1. Connect to V _{DPU1} ⁽¹⁾ through a pull-up resistor. |
| SC1 | 9 | 7 | E2 | Serial clock 1. Connect to V _{DPU1} ⁽¹⁾ through a pull-up resistor. |
| GND | 10 | 8 | E1 | Ground |
| ĪNT2 | 11 | 9 | E3 | Active-low interrupt input 2. Connect to V _{DPU2} ⁽¹⁾ through a pull-up resistor. |
| SD2 | 12 | 10 | E4 | Serial data 2. Connect to V _{DPU2} ⁽¹⁾ through a pull-up resistor. |
| SC2 | 13 | 11 | D2 | Serial clock 2. Connect to V _{DPU2} ⁽¹⁾ through a pull-up resistor. |
| INT3 | 14 | 12 | D4 | Active-low interrupt input 3. Connect to V _{DPU3} ⁽¹⁾ through a pull-up resistor. |
| SD3 | 15 | 13 | C3 | Serial data 3. Connect to V _{DPU3} ⁽¹⁾ through a pull-up resistor. |
| SC3 | 16 | 14 | C4 | Serial clock 3. Connect to V _{DPU3} ⁽¹⁾ through a pull-up resistor. |
| ĪNT | 17 | 15 | B2 | Active-low interrupt output. Connect to V _{DPUM} ⁽¹⁾ through a pull-up resistor. |
| SCL | 18 | 16 | B4 | Serial clock line. Connect to V _{DPUM} ⁽¹⁾ through a pull-up resistor. |
| SDA | 19 | 17 | A4 | Serial data line. Connect to V _{DPUM} ⁽¹⁾ through a pull-up resistor. |
| VCC | 20 | 18 | A3 | Supply power |

⁽¹⁾ V_{DPUX} is the pull-up reference voltage for the associated data line. V_{DPUM} is the master I²C reference voltage while V_{DPU0}-V_{DPU3} are the slave channel reference voltages.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | , | MIN | MAX | UNIT |
|------------------|--|------|------|------|
| V _{CC} | Supply voltage range | -0.5 | 7 | V |
| VI | Input voltage range ⁽²⁾ | -0.5 | 7 | V |
| I _I | Input current | | ±20 | mA |
| Io | Output current | | ±25 | mA |
| | Continuous current through V _{CC} | | ±100 | mA |
| | Continuous current through GND | | ±100 | mA |
| P _{tot} | Total power dissipation | | 400 | mW |
| T _A | Operating free-air temperature range | -40 | 85 | °C |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| | | | MIN | MAX | UNIT |
|--------|---|---|------|------|------|
| V | Electrostatic discharge Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | 0 | 2000 | V | |
| V(ESD) | | | 0 | 1000 | V |

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See (1)

| | | | MIN | MAX | UNIT |
|-------------------------------|--------------------------------|---------------------------|-----------------------|-----------------------|------|
| V_{CC} | Supply voltage | | 2.3 | 5.5 | V |
| V High level in motor alterna | SCL, SDA | 0.7 × V _{CC} | 6 | V | |
| V _{IH} | High-level input voltage | A1, A0, ĪNT3– ĪNT0, RESET | 0.7 × V _{CC} | V _{CC} + 0.5 | |
| \/ | Low-level input voltage | SCL, SDA | -0.5 | 0.3 × V _{CC} | V |
| V _{IL} | | A1, A0, ĪNT3– ĪNT0, RESET | -0.5 | 0.3 × V _{CC} | |
| T _A | Operating free-air temperature | | -40 | 85 | °C |

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | PCA9545A | | | | | | |
|-------------------------------|--|----------|---------|---------|---------|---------|----------|------|
| | | DGV | DW | PW | RGY | RGW | GQN, ZQN | UNIT |
| | | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | |
| R _{0JA} | Junction-to-ambient thermal resistance | 92 | 58 | 116.3 | 58.8 | 62.7 | 70 | °C/W |

For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

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⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| | PARAMETER | ₹ | TEST C | ONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--------------------------|---------------------|---|---|---|-----------------|-----|--------------------|-----|------|
| V _{PORR} | Power-on reset vo | Itage, V _{CC} rising | No load, | V _I = V _{CC} or GND | | | 1.2 | 1.5 | V |
| V _{PORF} | Power-on reset vo | Itage, V _{CC} falling ⁽²⁾ | No load, | V _I = V _{CC} or GND | | 0.8 | 1 | | V |
| | | | | | 5 V | | 3.6 | | |
| | | | | | 4.5 V to 5.5 V | 2.6 | | 4.5 | |
| ., | 0 11 1 1 1 | | ., ., | 100 4 | 3.3 V | | 1.9 | | ., |
| V_{pass} | Switch output volta | age | $V_{SWin} = V_{CC},$ | $I_{SWout} = -100 \mu A$ | 3 V to 3.6 V | 1.6 | | 2.8 | V |
| | | | | | 2.5 V | | 1.5 | | |
| | | | | | 2.3 V to 2.7 V | 1.1 | | 2 | |
| I _{OH} | ĪNT | | V _O = V _{CC} | | 2.3 V to 5.5 V | | | 10 | μA |
| | COL CDA | | V _{OL} = 0.4 V | | | 3 | 7 | | |
| I _{OL} | SCL, SDA | | V _{OL} = 0.6 V | | 2.3 V to 5.5 V | 6 | 10 | | mA |
| | ĪNT | | V _{OL} = 0.4 V | | | 3 | | | |
| | SCL, SDA | | | | | | | ±1 | |
| | SC3-SC0, SD3-S | D0 | | | | | | ±1 | |
| I | A1, A0 | | $V_I = V_{CC}$ or GND | | 2.3 V to 5.5 V | | | ±1 | μΑ |
| | INT3- INTO | | 1 | | | | | ±1 | |
| | RESET | | | | | | | ±1 | |
| | Operating mode | f _{SCL} = 100 kHz | | I _O = 0 | 5.5 V | | 3 | 12 | μΑ |
| | | | $V_I = V_{CC}$ or GND, | | 3.6 V | | 3 | 11 | |
| | | | | | 2.7 V | | 3 | 10 | |
| | Standby mode | Low inputs | | | 5.5 V | | 1.6 | 2 | |
| Icc | | | V _I = GND, | I _O = 0 | 3.6 V | | 1 | 1.3 | |
| | | | | | 2.7 V | | 0.7 | 1.1 | |
| | | | $V_I = V_{CC},$ $I_O = 0$ | | 5.5 V | | 1.6 | 2 | |
| | | High inputs | | I _O = 0 | 3.6 V | | 1 | 1.3 | |
| | | | | 2.7 V | | 0.7 | 1.1 | | |
| | | INTO INTO | One INT3- INT0 inp | | | | 8 | 20 | |
| Δ1 | Supply-current | INT3– INTO | One INT3- INT0 inp Other inputs at V _{CC} | out at V _{CC} – 0.6 V, or GND | 2.3 V to 5.5 V | | 8 | 20 | μΑ |
| ΔI _{CC} | change | SCL, SDA | SCL or SDA input a Other inputs at V _{CC} | | 2.3 V to 3.3 V | | 8 | 15 | |
| | | OOL, ODA | SCL or SDA input a Other inputs at V _{CC} | t V _{CC} – 0.6 V, or GND | | | 8 | 15 | |
| | A1, A0 | | V _I = V _{CC} or GND | | | | 4.5 | 6 | |
| Ci | ĪNT3– ĪNT0 | ĪNT3– ĪNT0 | | | 2.3 V to 5.5 V | | 4.5 | 6 | pF |
| | RESET | | | | | | 4.5 | 5.5 | |
| C _{io(OFF)} (3) | SCL, SDA | | V ₁ = V ₂₀ or GND | Switch OFF | 2.3 V to 5.5 V | | 15 | 19 | pF |
| ~10(UFF) ` ` | SC3-SC0, SD3-S | D0 | $V_I = V_{CC}$ or GND, | SWILCH OFF | 2.0 V 10 0.0 V | | 6 | 8 | Ρi |
| | | V = 0.4V | l _o = 15 mΔ | 4.5 V to 5.5 V | 4 | 10 | 16 | | |
| R _{ON} | Switch on-state re | sistance | $V_{O} = 0.4 \text{ V}, \qquad I_{O} = 15 \text{ mA}$ | | 3 V to 3.6 V | 5 | 13 | 20 | Ω |
| | | | $V_0 = 0.4 V$ | I _O = 10 mA | 2.3 V to 2.7 V | 7 | 16 | 45 | |

⁽¹⁾ All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}), $T_A = 25^{\circ}C$.

⁽²⁾ The power-on reset circuit resets the I2C bus logic when $V_{cc} < V_{PORF}$.

⁽³⁾ $C_{io(ON)}$ depends on the device capacitance and load that is downstream from the device.



6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

| | | | STANDARD I ² C BL | - | FAST MODE I ² C BUS | | UNIT |
|------------------------|---|---|---------------------------------|------|---------------------------------------|-----|------|
| | | | MIN | MAX | | MAX | |
| f _{scl} | I ² C clock frequency | | 0 | 100 | 0 | 400 | kHz |
| t _{sch} | I ² C clock high time | | 4 | | 0.6 | | μs |
| t _{scl} | I ² C clock low time | | 4.7 | | 1.3 | | μs |
| t _{sp} | I ² C spike time | | | 50 | | 50 | ns |
| t _{sds} | I ² C serial-data setup time | | 250 | | 100 | | ns |
| t _{sdh} | I ² C serial-data hold time | | 0(1) | | 0(1) | | μs |
| t _{icr} | I ² C input rise time | | | 1000 | 20 + 0.1C _b ⁽²⁾ | 300 | ns |
| t _{icf} | I ² C input fall time | | | 300 | 20 + 0.1C _b ⁽²⁾ | 300 | ns |
| t _{ocf} | I ² C output fall time | 10-pF to 400-pF bus | | 300 | 20 + 0.1C _b ⁽²⁾ | 300 | ns |
| t _{buf} | I ² C bus free time between stop ar | nd start | 4.7 | | 1.3 | | μs |
| t _{sts} | I ² C start or repeated start conditio | n setup | 4.7 | | 0.6 | | μs |
| t _{sth} | I ² C start or repeated start conditio | n hold | 4 | | 0.6 | | μs |
| t _{sps} | I ² C stop condition setup | | 4 | | 0.6 | | μs |
| t _{vdL(Data)} | Valid-data time (high to low) ⁽³⁾ | SCL low to SDA output low valid | | 1 | | 1 | μs |
| t _{vdH(Data)} | Valid-data time (low to high) ⁽³⁾ | SCL low to SDA output high valid | | 0.6 | | 0.6 | μs |
| t _{vd(ack)} | Valid-data time of ACK condition | ACK signal from SCL low to SDA output low | | 1 | | 1 | μs |
| C _b | I ² C bus capacitive load | | | 400 | | 400 | pF |

⁽¹⁾ A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to as the V_{IH} min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.

⁽²⁾ C_b = total bus capacitance of one bus line in pF

⁽³⁾ Data taken using a 1-k Ω pull-up resistor and 50-pF load (see Figure 7-1)



6.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L \le 100 \text{ pF}$ (unless otherwise noted) (see Figure 7-3)

| PARAMETER | | | FROM (INPUT) | TO (OUTPUT) | MIN MAX | UNIT |
|---------------------|-------------------------------------|-----------------------------------|-----------------|----------------|---------|------|
| t _{pd} (1) | Propagation delay time | $R_{ON} = 20 \Omega, C_L = 15 pF$ | SDA or SCL | SDn or SCn | 0.3 | ne |
| | | $R_{ON} = 20 \Omega, C_L = 50 pF$ | | 3011013011 | 1 | ns |
| t _{iv} | Interrupt valid time ⁽²⁾ | | ĪNTn | ĪNT | 4 | μs |
| t _{ir} | Interrupt reset delay time(2) | | ĪNTn | ĪNT | 2 | μs |

⁽¹⁾ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

6.8 Interrupt and Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-3)

| | PARAMETER | MIN | MAX | UNIT |
|-----------------------|--|-----|-----|------|
| t _{PWRL} | Low-level pulse duration rejection of INTn inputs | 1 | | μs |
| t _{PWRH} | High-level pulse duration rejection of INTn inputs | 0.5 | | μs |
| t _{WL} | Pulse duration, RESET low | 6 | | ns |
| t _{rst} (1) | RESET time (SDA clear) | | 500 | ns |
| t _{REC(STA)} | Recovery time from RESET to start | 0 | | ns |

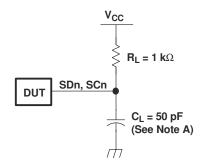
⁽¹⁾ t_{rst} is the propagation delay measured from the time the RESET pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of t_{WL}.

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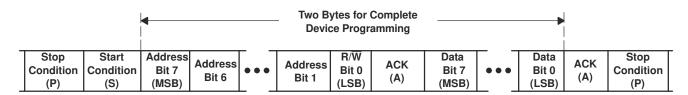
⁽²⁾ Data taken using a 4.7-kΩ pull-up resistor and 100-pF load (see Figure 7-3)



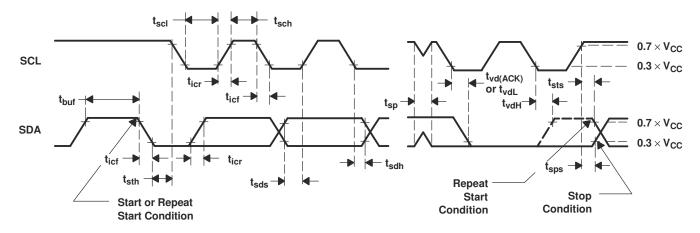
7 Parameter Measurement Information



I²C PORT LOAD CONFIGURATION



| BYTE | DESCRIPTION |
|------|--------------------------------|
| 1 | I ² C address + R/W |
| 2 | Control register data |



VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r/t_f = 30 ns.
- C. The outputs are measured one at a time, with one transition per measurement.

Figure 7-1. I²C Interface Load Circuit, Byte Descriptions, and Voltage Waveforms

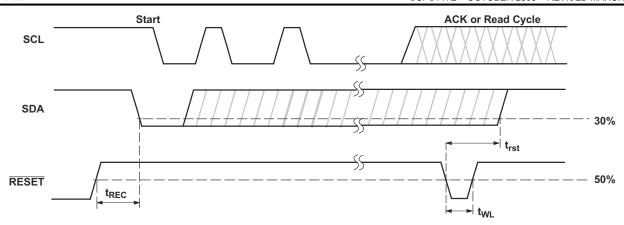
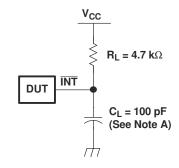
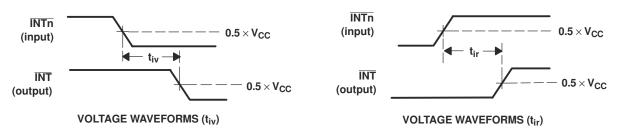


Figure 7-2. Reset Timing



INTERRUPT LOAD CONFIGURATION



- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r/t_f = 30 ns.

Figure 7-3. Interrupt Load Circuit and Voltage Waveforms



8 Detailed Description

8.1 Overview

The PCA9545A is a 4-channel, bidirectional translating I^2C switch. The master SCL/SDA signal pair is directed to four channels of slave devices, SC0/SD0-SC3/SD3. Any individual downstream channel can be selected as well as any combination of the four channels. The PCA9545A also supports interrupt signals in order for the master to detect an interrupt on the \overline{INT} output terminal that can result from any of the slave devices connected to the $\overline{INT3}$ - $\overline{INT0}$ input terminals.

The device offers an active-low $\overline{\text{RESET}}$ input which resets the state machine and allows the PCA9545A to recover should one of the downstream I²C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply, V_{CC}, also known as a power-on reset (POR). Both the $\overline{\text{RESET}}$ function and a POR will cause all channels to be deselected.

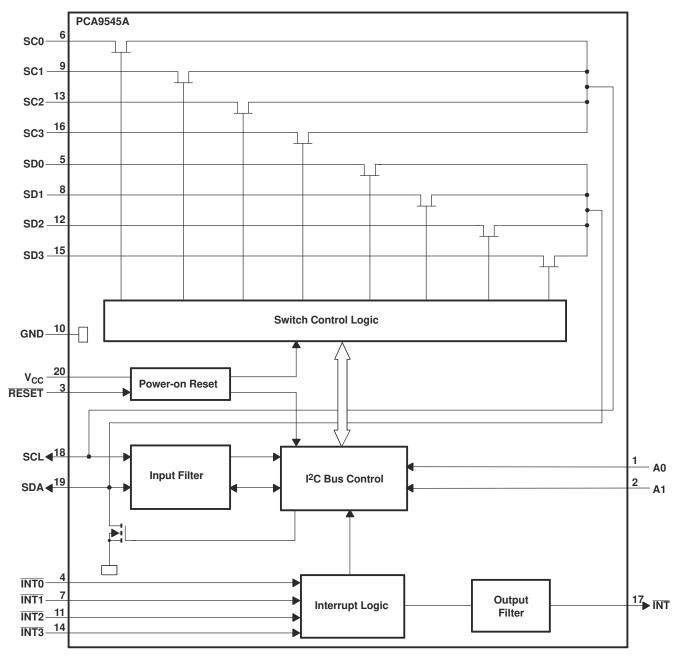
The connections of the I^2C data path are controlled by the same I^2C master device that is switched to communicate with multiple I^2C slaves. After the successful acknowledgment of the slave address (hardware selectable by A0 and A1 terminals), a single 8-bit control register is written to or read from to determine the selected channels and state of the interrupts.

The PCA9545A may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel.

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8.2 Functional Block Diagram



Pin numbers shown are for DGV, DW, PW, and RGY packages.

8.3 Feature Description

The PCA9545A is a 4-channel, bidirectional translating switch for I^2C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The PCA9545A features I^2C control using a single 8-bit control register in which the four least significant bits control the enabling and disabling of the 4 switch channels of I^2C data flow. The PCA9545A also supports interrupt signals for each slave channel and this data is held in the four most significant bits of the control register. Depending on the application, voltage translation of the I^2C bus can also be achieved using the PCA9545A to allow 1.8-V, 2.5-V, or 3.3-V parts to communicate with 5-V parts. Additionally, in the event that communication on the I^2C bus enters a fault state, the PCA9545A can be reset to resume normal operation using the \overline{RESET} pin feature or by a power-on reset which results from cycling power to the device.

8.4 Device Functional Modes

8.4.1 RESET Input

The $\overline{\text{RESET}}$ input can be used to recover the PCA9545A from a bus-fault condition. The registers and the I²C state machine within this device initialize to their default states if this signal is asserted low for a minimum of t_{WL} . All channels also are deselected in this case. $\overline{\text{RESET}}$ must be connected to V_{CC} through a pull-up resistor.

8.4.1.1 RESET Errata

If RESET voltage set higher than VCC, current will flow from RESET pin to VCC pin.

8.4.1.1.1

System Impact

VCC will be pulled above its regular voltage level

8.4.1.1.2

System Workaround

Design such that RESET voltage is same or lower than VCC

8.4.2 Power-On Reset

When power is applied to V_{CC} , an internal power-on reset holds the PCA9545A in a reset condition until V_{CC} has reached V_{PORR} . At this point, the reset condition is released and the PCA9545A registers and I^2C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below at least V_{PORF} to reset the device.

8.5 Programming

8.5.1 I²C Interface

The I²C bus is for two-way two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer can be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse, as changes in the data line at this time are interpreted as control signals (see Figure 8-1).

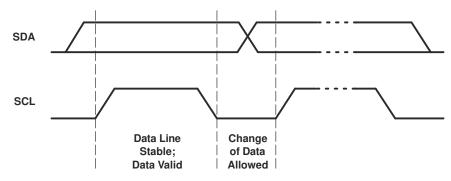


Figure 8-1. Bit Transfer

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see Figure 8-2).

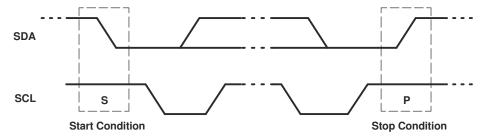


Figure 8-2. Definition of Start and Stop Conditions

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master, and the devices that are controlled by the master are the slaves (see Figure 8-3).

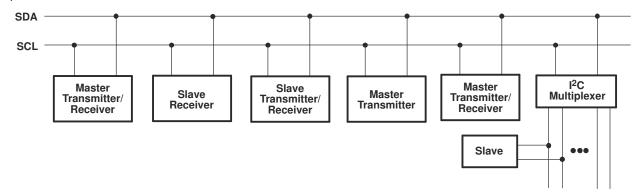


Figure 8-3. System Configuration

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 8-4). Setup and hold times must be taken into account.

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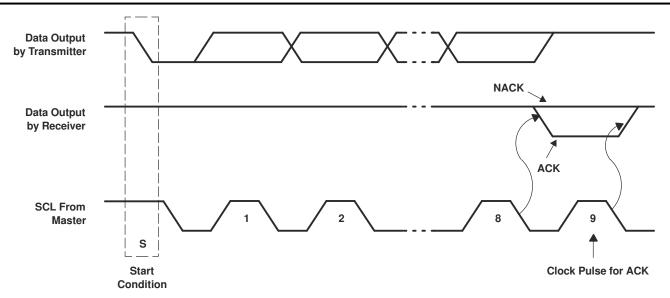


Figure 8-4. Acknowledgment on the I²C Bus

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

Data is transmitted to the PCA9545A control register using the write mode shown in Figure 8-5.

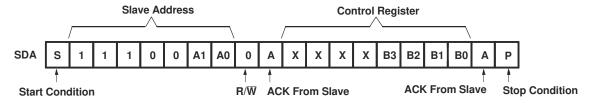


Figure 8-5. Write Control Register

Data is read from the PCA9545A control register using the read mode shown in Figure 8-6.

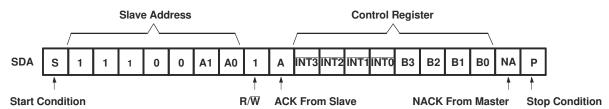


Figure 8-6. Read Control Register

8.6 Control Register

8.6.1 Device Address

Following a start condition, the bus master must output the address of the slave it is accessing. The address of the PCA9545A is shown in Figure 8-7. To conserve power, no internal pull-up resistors are incorporated on the hardware-selectable address terminals, and they must be pulled high or low.

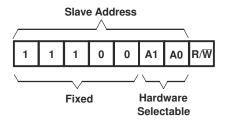


Figure 8-7. PCA9545A Address

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

8.6.2 Control Register Description

Following the successful acknowledgment of the slave address, the bus master sends a byte to the PCA9545A, which is stored in the control register (see Figure 8-8). If multiple bytes are received by the PCA9545A, it saves the last byte received. This register can be written and read via the I²C bus.

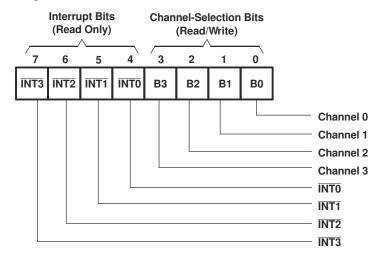


Figure 8-8. Control Register

8.6.3 Control Register Definition

One or several SCn/SDn downstream pairs, or channels, are selected by the contents of the control register (see Table 8-1). After the PCA9545A has been addressed, the control register is written. The four LSBs of the control byte are used to determine which channel or channels are to be selected. When a channel is selected, the channel becomes active after a stop condition has been placed on the I²C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition must occur always right after the acknowledge cycle.

Table 8-1. Control Register Write (Channel Selection), Control Register Read (Channel Status) (1)

| ĪNT3 | ĪNT2 | ĪNT1 | ĪNT0 | В3 | B2 | B1 | В0 | COMMAND |
|------|------|------|------|----|----|----|----|--------------------|
| V | | v | v | v | v | | 0 | Channel 0 disabled |
| ^ | ^ | ^ | ^ | ^ | ^ | ^ | 1 | Channel 0 enabled |

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Table 8-1. Control Register Write (Channel Selection), Control Register Read (Channel Status) (1) (continued)

| | | | | , | , | | | |
|------|------|------|------|----|----|-----|----|---|
| ĪNT3 | ĪNT2 | INT1 | ĪNT0 | В3 | B2 | B1 | В0 | COMMAND |
| Х | Х | Х | X | Х | Х | 0 | X | Channel 1 disabled |
| ^ | ^ | ^ | ^ | ^ | ^ | 1 | ^ | Channel 1 enabled |
| Х | X | Х | X | Х | 0 | Х | Х | Channel 2 disabled |
| ^ | ^ | ^ | ^ | ^ | 1 | 1 ^ | ^ | Channel 2 enabled |
| Х | Х | Х | V | 0 | X | Х | V | Channel 3 disabled |
| ^ | ^ | ^ | ^ | 1 | ^ | ^ | X | Channel 3 enabled |
| 0 | 0 | 0 | 0 | 0 | 0 | Х | 0 | No channel selected, power-up/reset default state |

⁽¹⁾ Several channels can be enabled at the same time. For example, B3 = 0, B2 = 1, B1 = 1, B0 = 0 means that channels 0 and 3 are disabled, and channels 1 are 2 and enabled. Care should be taken not to exceed the maximum bus capacity.

8.6.4 Interrupt Handling

The PCA9545A provides four interrupt inputs (one for each channel) and one open-drain interrupt output (see Table 8-2). When an interrupt is generated by any device, it is detected by the PCA9545A and the interrupt output is driven low. The channel does not need to be active for detection of the interrupt. A bit also is set in the control register.

Bits 4–7 of the control register correspond to channels 0–3 of the PCA9545A, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master then can address the PCA9545A and read the contents of the control register to determine which channel contains the device generating the interrupt. The master then can reconfigure the PCA9545A to select this channel and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs can be used as general-purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to V_{CC}.

Table 8-2. Control Register Read (Interrupt) (1)

| | | | | | | (| | |
|------|------|------|------|----|----|----|----|---------------------------|
| ĪNT3 | ĪNT2 | INT1 | ĪNT0 | В3 | B2 | B1 | В0 | COMMAND |
| Х | ~ | V | 0 | V | Х | Х | | No interrupt on channel 0 |
| ^ | ^ | ^ | 1 | ^ | ^ | ^ | ^ | Interrupt on channel 0 |
| Х | X | 0 | X | V | Х | Х | | No interrupt on channel 1 |
| ^ | ^ | 1 | ^ | ^ | ^ | ^ | ^ | Interrupt on channel 1 |
| Х | 0 | Х | Х | | Х | Х | V | No interrupt on channel 2 |
| ^ | 1 | ^ | ^ | ^ | ^ | ^ | X | Interrupt on channel 2 |
| 0 | ~ | | Х | Х | Х | | | No interrupt on channel 3 |
| 1 | ^ | X | ^ | ^ | ^ | ^ | ^ | Interrupt on channel 3 |

⁽¹⁾ Several interrupts can be active at the same time. For example, $\overline{\text{INT3}}$ = 0, $\overline{\text{INT2}}$ = 1, $\overline{\text{INT1}}$ = 1, $\overline{\text{INT0}}$ = 0 means that there is no interrupt on channels 0 and 3, and there is interrupt on channels 1 and 2.

Product Folder Links: PCA9545A

9 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Applications of the PCA9545A will contain an I^2C (or SMBus) master device and up to four I^2C slave devices. The downstream channels are ideally used to resolve I^2C slave address conflicts. For example, if four identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0, 1, 2, and 3. When the temperature at a specific location needs to be read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the I^2C master can move on and read the next channel.

In an application where the I²C bus will contain many additional slave devices that do not result in I²C slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels. If multiple switches will be enabled simultaneously, additional design requirements must be considered (See *Design Requirements* and *Detailed Design Procedure*).

9.2 Typical Application

A typical application of the PCA9545A will contain anywhere from 1 to 5 separate data pull-up voltages, V_{DPUX} , one for the master device (V_{DPUM}) and one for each of the selectable slave channels ($V_{DPU0} - V_{DPU3}$). In the event where the master device and all slave devices operate at the same voltage, then the pass voltage, $V_{pass} = V_{DPUX}$. Once the maximum V_{pass} is known, V_{cc} can be selected using Figure 9-2. In an application where voltage translation is necessary, additional design requirements must be considered (See *Design Requirements*).

Figure 9-1 shows an application in which the PCA9545A can be used.

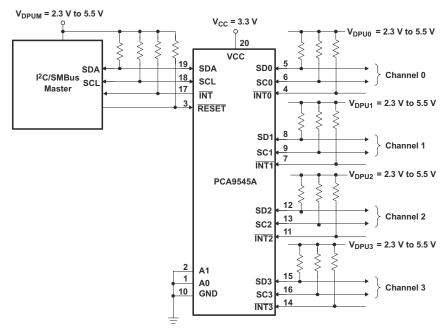


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

The pull-up resistors on the INT3- INT0 terminals in the application schematic are not required in all applications. If the device generating the interrupt has an open-drain output structure or can be tri-stated, a pull-up resistor is required. If the device generating the interrupt has a push-pull output structure and cannot be tri-stated, a pull-up resistor is not required. The interrupt inputs should not be left floating in the application.

The A0 and A1 terminals are hardware selectable to control the slave address of the PCA9545A. These terminals may be tied directly to GND or V_{CC} in the application.

If multiple slave channels will be activated simultaneously in the application, then the total I_{OL} from SCL/SDA to GND on the master side will be the sum of the currents through all pull-up resistors, R_p .

The pass-gate transistors of the PCA9545A are constructed such that the V_{CC} voltage can be used to limit the maximum voltage that is passed from one I^2C bus to another.

Figure 9-2 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the *Electrical Characteristics* section of this data sheet). In order for the PCA9545A to act as a voltage translator, the V_{pass} voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V, V_{pass} must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 9-2, V_{pass(max)} is 2.7 V when the PCA9545A supply voltage is 4 V or lower, so the PCA9545A supply voltage could be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 9-1).

9.2.2 Detailed Design Procedure

Once all the slaves are assigned to the appropriate slave channels and bus voltages are identified, the pull-up resistors, R_p , for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of V_{DPUX} , $V_{OL,(max)}$, and I_{OL} :

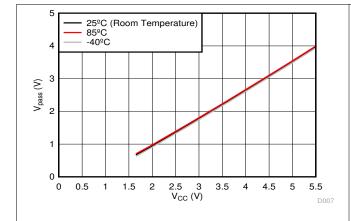
$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}}$$
(1)

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b :

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \tag{2}$$

The maximum bus capacitance for an I^2C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCA9545A, $C_{io(OFF)}$, the capacitance of wires/connections/traces, and the capacitance of each individual slave on a given channel. If multiple channels will be activated simultaneously, each of the slaves on all channels will contribute to total bus capacitance.

9.2.3 Application Curves



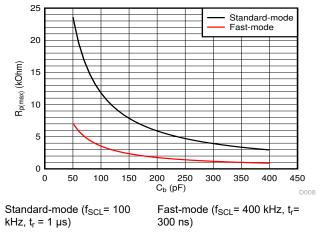
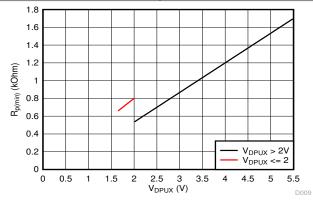


Figure 9-2. Pass-Gate Voltage (V_{pass}) vs Supply Voltage (V_{CC}) at Three Temperature Points

Figure 9-3. Maximum Pull-up resistance $(R_{p(max)})$ vs Bus Capacitance (C_b)



 V_{OL} = 0.2* V_{DPUX} , I_{OL} = 2 mA when $V_{DPUX} \le 2$ V V_{OL} = 0.4 V, I_{OL} = 3 mA when $V_{DPUX} > 2$ V

Figure 9-4. Minimum Pull-up Resistance (R_{p(min)}) vs Pull-up Reference Voltage (V_{DPUX})



10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, PCA9545A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 10-1 and Figure 10-2.

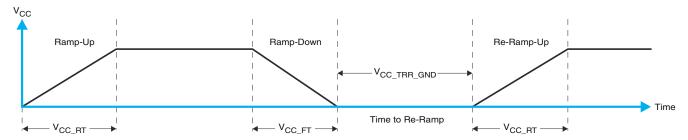


Figure 10-1. V_{CC} Is Lowered Below 0.2 V Or 0 V And Then Ramped Up To V_{CC}

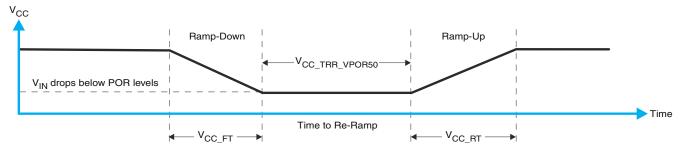


Figure 10-2. V_{CC} Is Lowered Below The Por Threshold, Then Ramped Back Up To V_{CC}

Table 10-1 specifies the performance of the power-on reset feature for PCA9545A for both types of power-on reset.

| Table 10-1. Recommended Supply Sequencing And Ramp Rates |
|--|
|--|

| | rabio io iritocommonaca cappiy coquen | | | | | |
|---------------------------|--|-----------------|-------|-----|-------|------|
| | PARAMETER | | MIN | TYP | MAX | UNIT |
| V _{CC_FT} | Fall rate | See Figure 10-1 | 1 | | 100 | ms |
| V _{CC_RT} | Rise rate | See Figure 10-1 | 0.01 | | 100 | ms |
| V _{CC_TRR_GND} | Time to re-ramp (when V _{CC} drops to GND) | See Figure 10-1 | 0.001 | | | ms |
| V _{CC_TRR_POR50} | Time to re-ramp (when V _{CC} drops to V _{POR_MIN} – 50 mV) | See Figure 10-2 | 0.001 | | | ms |
| V _{CC_GH} | Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 μs | See Figure 10-3 | | | 1.2 | V |
| V _{CC_GW} | Glitch width that will not cause a functional disruption when $V_{\text{CCX_GH}} = 0.5 \times V_{\text{CCx}}$ | See Figure 10-3 | | | | μs |
| V _{PORF} | Voltage trip point of POR on falling V _{CC} | | 0.767 | | 1.144 | V |
| V _{PORR} | Voltage trip point of POR on rising V _{CC} | | 1.033 | | 1.428 | V |

(1) $T_A = -40$ °C to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and the device impedance are factors that affect power-on reset performance. Figure 10-3 and Table 10-1 provide more information on how to measure these specifications.

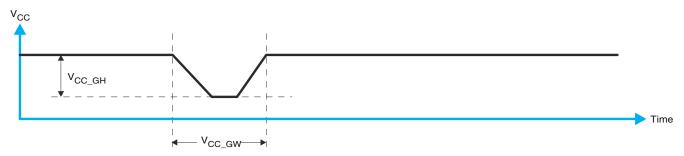


Figure 10-3. Glitch Width And Glitch Height

 V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 10-4 and Table 10-1 provide more details on this specification.

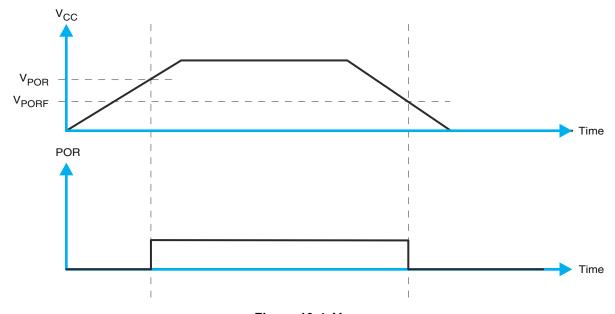


Figure 10-4. V_{POR}



11 Layout

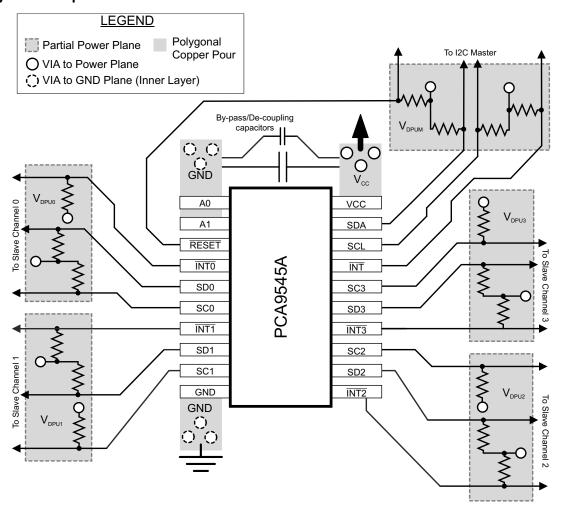
11.1 Layout Guidelines

For PCB layout of the PCA9545A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I²C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and terminals that are connected to ground should have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC terminal, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all V_{DPUX} voltages and V_{CC} could be at the same potential and a single copper plane could connect all of pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V_{DPUM} , V_{DPU0} , V_{DPU1} , V_{DPU2} , and V_{DPU3} may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I²C bus capacitance added by PCB parasitics, data lines (SCn, SDn and INTn) should be a short as possible and the widths of the traces should also be minimized (e.g. 5-10 mils depending on copper weight).

11.2 Layout Example



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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

| Orderable part number | Status | Material type | Package Pins | Package qty Carrier | RoHS | Lead finish/ | MSL rating/ | Op temp (°C) | Part marking |
|-----------------------|----------|---------------|-----------------|-----------------------|------|---------------|---------------------|--------------|--------------|
| | (1) | (2) | | | (3) | Ball material | Peak reflow | | (6) |
| | | | | | | (4) | (5) | | |
| PCA9545ADW | NRND | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCA9545A |
| PCA9545ADW.A | NRND | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCA9545A |
| PCA9545ADWR | NRND | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCA9545A |
| PCA9545ADWR.A | NRND | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCA9545A |
| PCA9545APWR | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PD545A |
| PCA9545APWR.B | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PD545A |
| PCA9545APWT | Obsolete | Production | TSSOP (PW) 20 | - | - | Call TI | Call TI | -40 to 85 | PD545A |
| PCA9545ARGYR | Active | Production | VQFN (RGY) 20 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PD545A |
| PCA9545ARGYR.B | Active | Production | VQFN (RGY) 20 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PD545A |
| PCA9545ARGYRG4 | Active | Production | VQFN (RGY) 20 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PD545A |
| PCA9545ARGYRG4.B | Active | Production | VQFN (RGY) 20 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PD545A |

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





| A0 | Dimension designed to accommodate the component width |
|----|---|
| В0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|-----------------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| PCA9545ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| PCA9545APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| PCA9545ARGYR | VQFN | RGY | 20 | 3000 | 330.0 | 12.4 | 3.71 | 4.71 | 1.1 | 8.0 | 12.0 | Q1 |
| PCA9545ARGYRG4 | VQFN | RGY | 20 | 3000 | 330.0 | 12.4 | 3.71 | 4.71 | 1.1 | 8.0 | 12.0 | Q1 |

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*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| PCA9545ADWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| PCA9545APWR | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| PCA9545ARGYR | VQFN | RGY | 20 | 3000 | 367.0 | 367.0 | 35.0 |
| PCA9545ARGYRG4 | VQFN | RGY | 20 | 3000 | 367.0 | 367.0 | 35.0 |

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| PCA9545ADW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| PCA9545ADW.A | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SOIC



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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Last updated 10/2025