











SBAS883A - FEBRUARY 2018 - REVISED JUNE 2018

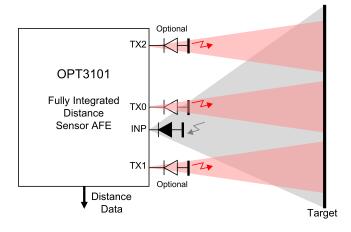
**OPT3101** 

# **OPT3101 ToF-Based Long-Range Proximity and Distance Sensor AFE**

#### **Features**

- Long-Range Distance Measurement, Obstacle **Detection and Avoidance**
- Flexibility to Customize Design With a Wide Variety of Photodiodes and Emitters
- Sample Rate up to 4 kHz
- 16-Bit Distance Output at 15-m Unambiguous Range
- De-Aliasing to Extend the Distance Range
- Supports 3 Transmitter Channels for Multi-Zone Operation
- **Excellent Ambient and Sunlight Rejection**
- 200-nA Full-Scale Signal Current
- 88-dB Signal Phase Dynamic Range at 1 kHz
- Supports DC Ambient up to 200 µA, 60-dB Rejection for Ambient at 1 kHz
- Distance Measurement Independent of Object Reflectivity
- Adaptive HDR to Save Power and Increase the Dynamic Range
- Configurable Event Detection and Interrupt Output Mechanism
- I<sup>2</sup>C Interface for Control and Data
- Integrated Illumination Driver With Programmable Current Control up to 173 mA
- Integrated Temperature Sensor for Calibration
- Single 3.3-V or 1.8-V and 3.3-V Supply Operation
- Operating Ambient Temperature: -40 to 85°C

#### Application Block Diagram



## 2 Applications

- Precise Long-Range Distance Measurement
  - Background Suppression and Accurate Object Counting in High-Speed Conveyor Belt Systems
  - Precise Displacement Sensing in Factory Automation
  - Non-Contact Distance and/or Level Measurement in Harsh Environments (High-Temperature or Hazardous Conditions)
- Obstacle Detection and Avoidance
  - Precise Distance Measurement for Drone Landing and Navigation
  - Cliff and Edge Detection in Vacuum Cleaners (No False Triggers From Dark Carpets)
  - Perimeter Scan in Automatic Guided Vehicle Like Lawnmowers, Robots
  - Obstruction Sensing in Applications Such as Smoke Detectors, Emergency Exits

## 3 Description

The OPT3101 device is a high-speed, high-resolution for continuous-wave, time-of-flight based proximity sensing and range finding. The device integrates the complete depth processing pipeline that includes the ADC, timing sequencer, and the digital processing engine. The device also has a builtin illumination driver that covers most of the target applications.

Given the high ambient rejection ratio, the device can support very high ambient conditions, including full sunlight of 130 klx.

The timing sequencer is highly configurable to provide for application-specific trade-offs of power versus performance.

The device provides depth data that consists of phase, amplitude, and ambient measurements. The calibration subsystem supports phase-data calibration for inaccuracies resulting from temperature and crosstalk.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPT3101	VQFN (28)	5.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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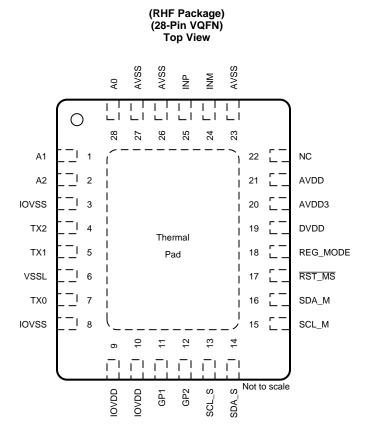
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# 4 Revision History

Cł	nanges from Original (February 2018) to Revision A	Page
•	Changged several items in the Features list	1
•	Changed the Application Block Diagram	1
•	Changed several items in the Applications section	1
•	Changed all occurrences of "free-air temperature" in the data sheet to "junction temperature"	5
•	Changed all occurrances of VCC in the data sheet to V <sub>CC</sub>	5
•	Added a row to the Absolute Maximum Ratings table for Vo, Output voltage	5
•	Added two rows to the Recommended Operating Conditions table for V <sub>I</sub> and V <sub>O</sub>	5
•	Changed subscripting of some parameter symbols in the Electrical Characteristics condition statement	6
•	Changed subscripting for t <sub>PU,Deepsleep</sub> and t <sub>PU,Standby</sub>	6
•	Changed table rulings for V <sub>OH</sub> , V <sub>OL</sub> , and I <sub>I</sub>	7
•	Changed Figure 15	
•	Changed Figure 16	14
•	Changed the contents of numerous cells in the <i>Table 29</i> table	
•	Added the Table 30 table	40
•	Changed the content in most of the subsections of Register Descriptions	40



# 5 Pin Configuration and Functions



NC - No internal connection

## **Pin Functions**

PIN	N	I/O TYPE <sup>(1)</sup>		DESCRIPTION
NAME	NO.	I/O	ITPE	DESCRIPTION
A0	28	I	AVDD	I <sup>2</sup> C slave LSB0 address bit
A1	1	I	AVDD	I <sup>2</sup> C slave LSB1 address bit
A2	2	I	AVDD	I <sup>2</sup> C slave LSB2 address bit
AVDD	21	_	_	1.8-V analog supply
AVDD3	20	_	_	3.3-V analog supply
AVSS	23, 26, 27	_	_	Analog ground
DVDD	19	_	_	1.8-V digital supply
GP1	11	0	IOVDD	General-purpose output
GP2	12	I/O	IOVDD	General-purpose output, CLKREF input
INM	24	1	AVDD	AFE negative input. Connect photodiode equivalent capacitance. Connect the other end of the capacitor to ground AVSS.
INP	25	I	AVDD	AFE positive input. Connect photodiode cathode. Connect the Anode of the photodiode to ground AVSS.
IOVDD	9, 10	_	_	Supply for I/O and illumination driver
IOVSS	3, 8	_	_	Ground for digital and I/O
NC	22		_	No internal connection
REG_MODE	18	ı	IOVDD	Mode to select internal regulator for 1.8-V supplies (AVDD, DVDD)

(1) This column provides the I/O voltage domain of the input and output pins.



# Pin Functions (continued)

PIN	ı	1/0	TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.	I/O	ITPE	DESCRIPTION
RST_MS	17	I	IOVDD	Active-low global reset, monoshot trigger. There is no internal pullup on this pin. Connect this pin to the host controller or add a pullup resistor.
SCL_M	15	0	IOVDD	$I^2$ C master clock. Connect with a 10-kΩ resistor to a 3.3-V supply.
SCL_S	13	I	IOVDD	$I^2$ C slave clock. Connect with a 10-kΩ resistor to a 3.3-V supply.
SDA_M	16	I/O	IOVDD	$I^2C$ master data. Connect with a 10-k $\Omega$ resistor to a 3.3-V supply.
SDA_S	14	I/O	IOVDD	$I^2$ C slave data. Connect with a 10-kΩ resistor to a 3.3-V supply.
TX0	7	0	IOVDD	Illumination driver output. Connect to LED cathode. Anode should be connected to a supply.
TX1	5	0	IOVDD	Illumination driver output. Connect to LED cathode. Anode should be connected to a supply.
TX2	4	0	IOVDD	Illumination driver output. Connect to LED cathode. Anode should be connected to a supply.
VSSL	6	_	_	Illumination driver ground.
Thermal pad	_	_	_	Thermal pad of the device. Connect thermal pad to AVSS PCB ground plane using multiple vias for good thermal performance.

Product Folder Links: OPT3101

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## 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
IOVDD	Digital I/O supply	-0.3	4	V
AVDD3	Analog supply	-0.3	4	V
AVDD	Analog supply	-0.3	2.2	V
DVDD	Digital supply	-0.3	2.2	V
VI	Input voltage at input pins	-0.3	V <sub>CC</sub> + 0.3 <sup>(2)</sup>	V
Vo	Output voltage at output pins	-0.3	V <sub>CC</sub> + 0.3 <sup>(2)</sup>	V
TJ	Junction temperature	-40	125	°C
T <sub>stg</sub>	Storage temperature	-40	125	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

			VALUE	UNIT
V	Flactrostatia disebarga	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±1000	<b>V</b>
V (ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±250	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IOVDD	Digital I/O supply	1.7	1.8 to 3.3	3.6	V
AVDD3	Analog supply	3	3.3	3.6	V
AVDD	Analog supply	1.7	1.8	1.9	V
DVDD	Digital supply	1.7	1.8	1.9	V
$V_{DRV}$	TX0, TX1, TX2 pin voltage	0.7		3.6	V
VI	Input voltage at input pins	-0.1		$V_{CC} + 0.3$	V
Vo	Output voltage at output pins	-0.1		V <sub>CC</sub> + 0.3	V
T <sub>A</sub>	Ambient temperature	-40		85	°C

(1) V<sub>CC</sub> is equal to IOVDD or AVDD, based on the I/O voltage domain listed in the *Pin Functions* table.

<sup>(2)</sup> V<sub>CC</sub> is equal to IOVDD or AVDD, based on the I/O voltage domain listed in the *Pin Functions* table.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



#### 6.4 Thermal Information

		OPT3101	
	THERMAL METRIC (1)	RHF (QFN)	UNIT
		28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.8	°C/W
$\Psi_{\text{JT}}$	Junction-to-top characterization parameter	0.3	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	10.7	°C/W
R <sub>0</sub> JC(bot)	Junction-to-case (bottom) thermal resistance	1.6	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics.

#### 6.5 Electrical Characteristics

All specifications at  $T_A$  = 25°C,  $V_{AVDD}$  = 1.8 V,  $V_{AVDD3}$  = 3.3 V,  $V_{DVDD}$  = 1.8 V,  $V_{IOVDD}$  = 3.3 V,  $I_{ambMax}$  = 20  $\mu$ A, photodiode with a capacitance of 2 pF at AFE input unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN	TYP MAX	UNIT
AFE			,		
I <sub>ref</sub>	Full-scale signal current at f <sub>mod</sub>			200	nA
I <sub>noise</sub>	AFE input-referred current noise			1.5 <sup>(1)</sup>	pA/√Hz
I <sub>ambMax</sub>	Maximum ambient dc current at input	AVDD3 = 3.3 V	20	00 <sup>(2)</sup>	μA
µ <sub>1000Hz</sub>	Ambient attenuation at 1000 Hz			60	dB
V <sub>R</sub>	Bias voltage at INM, INP			1	V
C <sub>in</sub>	Maximum external photodiode capacitance at input			6	pF
f <sub>mod</sub>	Modulation frequency			10	MHz
sps	Sample rate			4000	Hz
t <sub>PU,Deepsleep</sub>	Deep sleep recovery time	Monoshot mode only		1	ms
t <sub>PU,Standby</sub>	Standby recovery time (3)			50	μs
ILLUMINATI	ON DRIVER				
I <sub>DRV</sub>	Maximum built-in illumination driver current			173.6	mA
POWER (AC	TIVE MODE AT MAXIMUM FRAME RAT	TE)			
I <sub>AVDD</sub>	1.8-V analog supply current			11.6	mA
I <sub>DVDD</sub>	1.8-V digital supply current			5.7	mA
I <sub>AVDD3</sub>	3.3-V analog supply current			0.5	mA
I <sub>IOVDD</sub>	3.3-V I/O supply current			0.7	mA
POWER (DE	EP SLEEP MODE)				
I <sub>AVDD</sub>	1.8-V analog supply current			1	μA
$I_{DVDD}$	1.8-V digital supply current			3	μΑ
I <sub>AVDD3</sub>	3.3-V analog supply current			1	μΑ
I <sub>IOVDD</sub>	3.3-V I/O current			2	μA
POWER (AC	TIVE MODE AT MAXIMUM FRAME RAT	E), INTERNAL LDO MODE			
I <sub>AVDD3</sub>	3.3-V analog supply current	Internal LDO mode		17.9	mA
I <sub>IOVDD</sub>	3.3-V I/O supply current	Internal LDO mode		0.7	mA
POWER (DE	EP SLEEP MODE), INTERNAL LDO MO	DE			
I <sub>AVDD3</sub>	3.3-V analog supply current	Internal LDO mode		80	μΑ
I <sub>IOVDD</sub>	3.3-V I/O supply current	Internal LDO mode		2	μA
CMOS I/Os	·				

- (1) Noise is higher by 20% with a photodiode capacitance of 6 pF at the AFE input.
- (2) I<sub>ambMax</sub> is programmable through register setting IAMB\_MAX\_SEL.
- (3) Reference, oscillator, and ambient cancellation are not powered down.



## **Electrical Characteristics (continued)**

All specifications at  $T_A$  = 25°C,  $V_{AVDD}$  = 1.8 V,  $V_{AVDD3}$  = 3.3 V,  $V_{DVDD}$  = 1.8 V,  $V_{IOVDD}$  = 3.3 V,  $I_{ambMax}$  = 20  $\mu$ A, photodiode with a capacitance of 2 pF at AFE input unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>IH</sub>	Input high-level threshold		0.7 × V <sub>CC</sub>			V
V <sub>IL</sub>	Input low-level threshold				0.3 × V <sub>CC</sub>	V
	O dead birth hand	I <sub>OH</sub> = -2 mA		V <sub>CC</sub> <sup>(4)</sup> – 0.45		
V <sub>OH</sub>	Output high level	I <sub>OH</sub> = -8 mA		V <sub>CC</sub> <sup>(4)</sup> – 0.5		V
\/	Output low lovel	I <sub>OL</sub> = 2 mA		0.35		V
$V_{OL}$	Output low level	$I_{OL} = 8 \text{ mA}$		0.65		V
	land nin lankana admant	Pins with pullup, pulldown resistor		±50		
Ц	Input pin leakage current	Pins without pullup, pulldown resistor			±10	μΑ
C <sub>I</sub>	Input capacitance			5		pF
I <sub>OH</sub>	Maximum output current high level			10		mA
I <sub>OL</sub>	Maximum output current low level		·	10		mA

<sup>(4)</sup> V<sub>CC</sub> is equal to IOVDD or AVDD, based on the I/O voltage domain listed in the *Pin Functions* table.

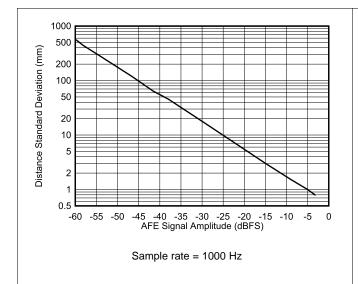
## 6.6 Timing Requirements

		MIN	NOM N	ИАХ	UNIT
RSTZ_MS I	Pin				
t <sub>PWMonoShot</sub>	Pulse duration of monoshot trigger	0.1		1	μs
t <sub>PWReset</sub>	Reset pulse duration	30			μs
I <sup>2</sup> C Slave					
f <sub>SCL</sub>	I <sup>2</sup> C slave SCL operating frequency			400	kHz



## 6.7 Typical Characteristics

All specifications at  $T_A$  = 25°C,  $V_{AVDD}$  = 1.8 V,  $V_{AVDD3}$  = 3.3 V,  $V_{DVDD}$  = 1.8 V,  $V_{IOVDD}$  = 3.3 V,  $I_{ambMax}$  = 20  $\mu$ A, photodiode with a capacitance of 2 pF at INP and INM, unless otherwise noted.



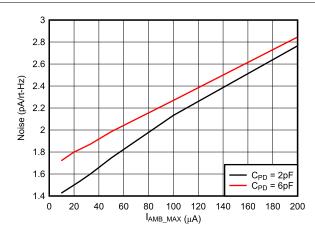


Figure 1. Distance Standard Deviation vs AFE Input Signal

Figure 2. AFE Thermal Noise vs Maximum Ambient Current Supported

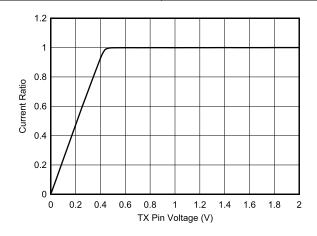


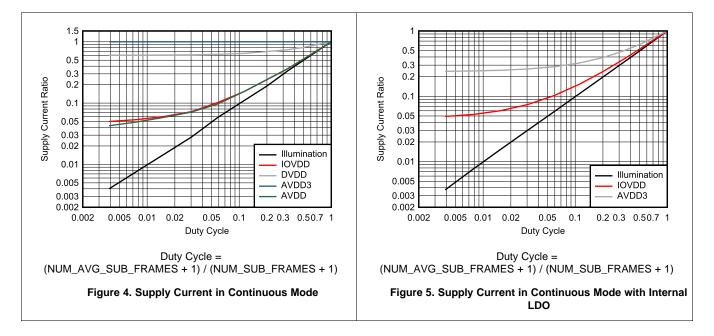
Figure 3. Illumination Driver I-V Characteristics

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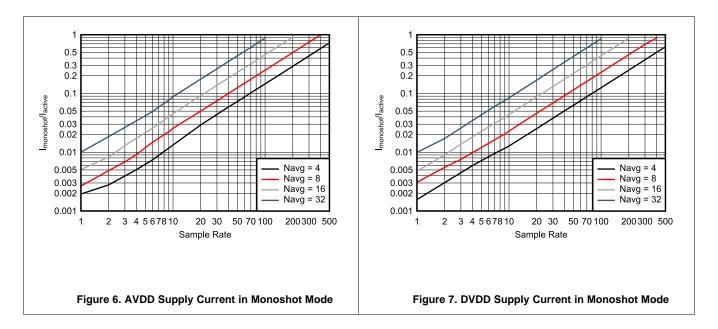
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#### 6.7.1 Continuous Mode

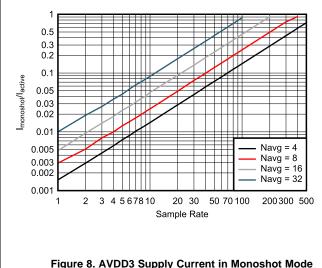


#### 6.7.2 Monoshot Mode



# **NSTRUMENTS**

## **Monoshot Mode (continued)**



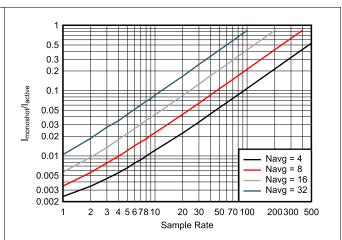
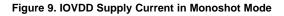


Figure 8. AVDD3 Supply Current in Monoshot Mode



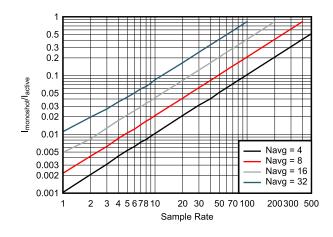


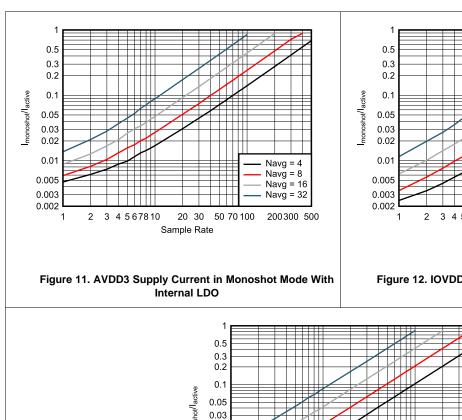
Figure 10. Illumination Supply Current in Monoshot Mode

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#### 6.7.3 Monoshot Mode With Internal LDO



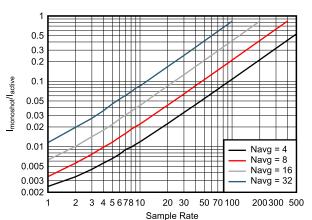


Figure 12. IOVDD Supply Current in Monoshot Mode With Internal LDO

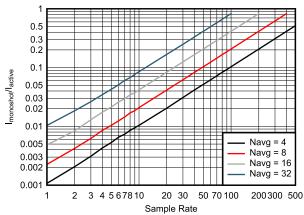


Figure 13. Illumination Supply Current in Monoshot Mode With Internal LDO



## 7 Detailed Description

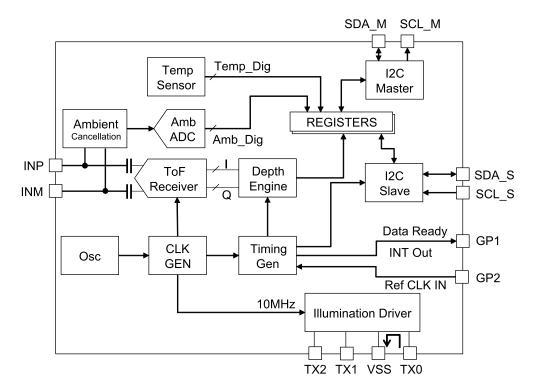
#### 7.1 Overview

The OPT3101 device is a fully integrated analog front end (AFE) based on the time-of-flight (ToF) principle using active illumination. The OPT3101 AFE connects to an external illuminator (LED, VCSEL, or LASER) to transmit modulated optical signals, and reflected signals are received by an external photodiode which connects to the input of the AFE. The received signal is converted to amplitude and phase information by the AFE and depth engine. This output is stored in registers, which can be read out through the device I<sup>2</sup>C interface.

The OPT3101 AFE has the following blocks:

- Timing generator: generates the sequencing signals for the sensor, illumination, and depth processor
- ToF receiver AFE
- Illumination driver
- Depth engine: calculates phase and amplitude
- I<sup>2</sup>C slave for configuration and output data interface of the device registers by the host processor
- I<sup>2</sup>C master for external temperature sensing, auto load registers from an external EEPROM

## 7.2 Functional Block Diagram



#### 7.3 Feature Description

## 7.3.1 Timing Generator

The timing generator (TG) generates the timing sequence for each frame. The TG has the following features:

- Frame rate control
- Sequencing

The following are various modes of operation:

- Continuous or monoshot mode
- Auto high-dynamic-range (HDR) mode or non-HDR mode
- Single-LED or multi-LED mode



## Feature Description (continued)

Different modes of operation are explained below.

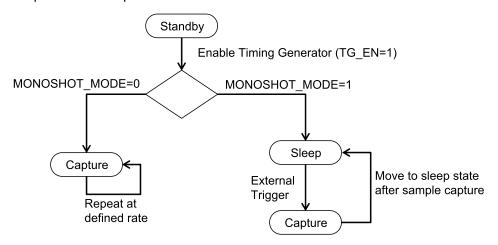


Figure 14. Continuous and Monoshot Modes

#### 7.3.1.1 Continuous Operating Mode

In this mode, the device runs continuously at the programmed sample rate. More details about the frame timing are described in Non-HDR Mode and Auto HDR Mode.

#### 7.3.1.2 Monoshot Mode

Monoshot mode is a low-power mode. In this mode, the device is in a deep sleep state and waits for an external trigger. The sample can be initiated by an  $\overline{RST_MS}$  pin (active-low) trigger or the register trigger (MONOSHOT\_BIT). On trigger, the device comes out of power down, waits for the programmed delay (POWERUP\_DELAY) to start a frame, captures the specified number of samples (MONOSHOT\_NUMFRAME), then goes into a deep sleep state to save power. A new interrupt is serviced only after completing the current frame capture. Any interrupt during the capture of a frame is discarded. Figure 15 shows the timing diagram of the monoshot mode with the  $\overline{RST_MS}$  pin trigger. From the trigger, the frame start can be delayed by setting the POWERUP\_DELAY register. The delay between the trigger and the sample start (FR\_VD signal in Figure 15) is (64 × POWERUP\_DELAY + 2) ×  $t_{CLK}$ . A minimum delay of 0.4 ms is required for the device to come out of the deep sleep state. A maximum of 26.2 ms delay can be programmed. This mode can also be used for synchronized capture from an external host.

The  $\overline{RST\_MS}$  pin is a dual-purpose pin used for reset and monoshot triggering. For reset, give a pulse duration that is > 30  $\mu$ s. For monoshot trigger, give a pulse duration that is < 1  $\mu$ s and > 100 ns.

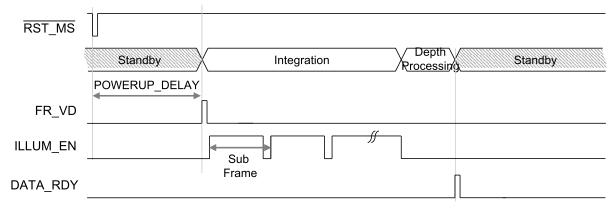


Figure 15. Timing for Pin-Triggered Monoshot Mode With RST MS



## Feature Description (continued)

For register-triggered monoshot mode, the host writes 1 to the interrupt register (MONOSHOT\_BIT) to initiate sample capture. Once the data ready of the Nth sample is available, the device automatically clears the interrupt register bit and goes into deep sleep state.

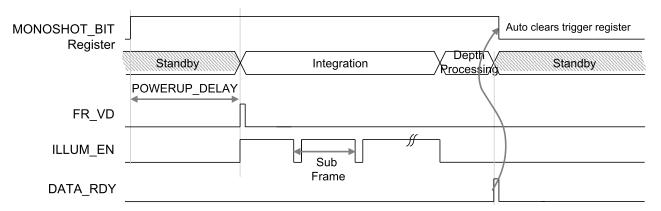


Figure 16. Timing for Register (MONOSHOT\_BIT) Triggered Monoshot Mode

Table 1. Monoshot Mode Register Settings		
	ADDRESS	DESCRIPTION

PARAMETER	ADDRESS	DESCRIPTION
MONOSHOT_MODE	27h[1:0]	0: Continuous mode   3: Monoshot mode   Other values: Not valid
MONOSHOT_NUMFRAME	27h[7:2]	Number of frames to be captured for every trigger.
POWERUP_DELAY	26h[23:10]	Register to program the delay from the external trigger to start of frame (FRAME_VD). Delay = $(64 \times POWERUP\_DELAY + 2) \times t_{CLK}$ , $t_{CLK} = 25$ ns.
MONOSHOT_BIT	0h[23]	Monoshot trigger register.  Write 1 to start sample capture. The bit is auto cleared after capture completion.

#### 7.3.1.3 Non-HDR Mode

In this mode a fixed LED current is used for the Illumination driver. Figure 17 shows the frame timing. Each frame is divided into multiple sub-frames, which can be varied from 1 to 212. Each sub-frame is 10,000 clocks of 40 MHz, which is equal to a 4-kHz sub-frame rate. In each sub-frame, 8192 clocks is the photodiode signal integration time and the remainder of the time is used for processing the signal and computing amplitude and phase. The device can be operated at the highest frame rate of 4 kHz by setting the number of sub-frames to 1  $(NUM_SUB_FRAMES = 0)$  in a frame.

Sample Rate = 
$$\frac{4000}{1 + \text{NUM\_SUB\_FRAMES}}$$
 (1)

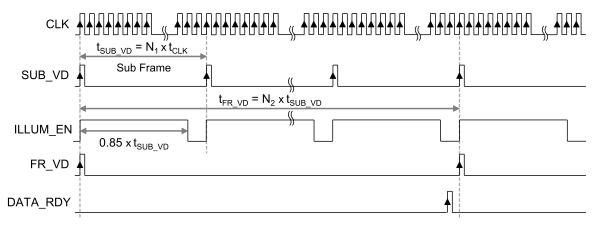
**Table 2. Sample-Rate Configuration Registers** 

PARAMETER	ADDRESS	DESCRIPTION
NUM_SUB_FRAMES	9Fh[11:0]	Total number of sub-frames in a frame. Each sub-frame is 0.25 ms.  Number of sub frames in a frame = NUM_SUB_FRAMES + 1.  This number must be equal or greater than NUM_AVG_SUB_FRAMES.
NUM_AVG_SUB_FRAMES	9Fh[23:12]	Specifies the number of sub-frames to be averaged in a frame. Number of averaged sub-frames should be a power of 2 Averaging sub-frames = NUM_AVG_SUB_FRAMES + 1.

If the number of averaged sub-frames is not a power of 2, the output amplitude AMP OUT scales according Equation 2. This is only a digital scaling factor and does not affect the distance noise of the measurement. It is recommended to use number of averaged sub-frames as a power of 2.

Amplitude Scaling Factor = 
$$\frac{1 + \text{NUM\_AVG\_SUB\_FRAMES}}{2^{\left(\text{ceil}(\log_2^{(1+\text{NUM\_AVG\_SUB\_FRAMES})}\right)}}$$
(2)





- (1)  $N_1 = 10,000$ ; number of 40-MHz clocks in a sub-frame.
- (2)  $N_2 = NUM_SUB_FRAMES + 1$  is the number of sub-frames in a frame, programmable in the range of 1 to  $2^{12}$ .

Figure 17. Frame Timing Diagram

#### 7.3.1.4 Auto HDR Mode

In this mode, the sequencer switches between two illumination driver currents to extend the dynamic range, depending on the signal saturation and lower amplitude threshold. The principle of operation is explained in Figure 18. When the illumination driver current is high and the amplitude exceeds the saturation threshold, HDR\_THR\_HIGH, the illumination driver is switched to the lower current. When the illumination driver current is low and the measured amplitude is below the lower threshold, HDR\_THR\_LOW, the illumination driver is switched to the higher current.

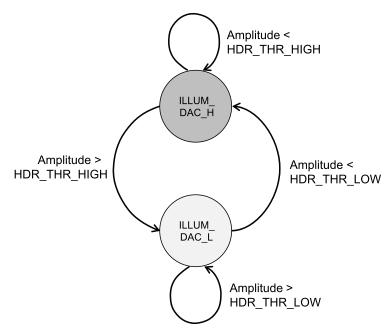
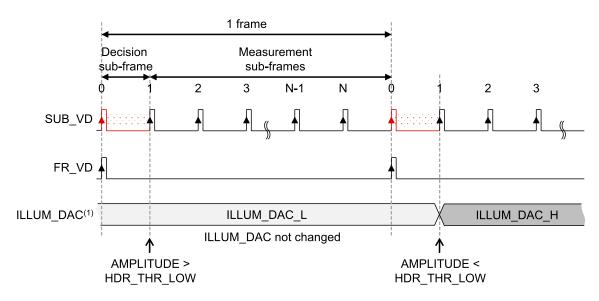


Figure 18. Auto HDR Mode: State Diagram

Figure 19 shows the frame timing diagram for HDR mode. In this mode, the first sub-frame information is used to make a decision about the validity of the output. If the first sub-frame output is valid, the same illumination DAC is used for the rest of the frame, otherwise the illumination driver is switched to the second illumination DAC current.





(1) The illumination driver DAC switching is shown for a particular scenario.

Figure 19. Auto HDR Mode Frame Timing Diagram

Amplitude thresholds for the HDR mode should be chosen according to Equation 3. Choice of the two illumination driver DAC currents depends on the end application.

$$\frac{\text{HDR\_THR\_HIGH}}{\text{HDR\_THR\_LOW}} > \frac{\text{ILLUM\_DAC\_H}}{\text{ILLUM\_DAC\_L}} \tag{3}$$

HDR\_THR\_HIGH is the saturation threshold for the HDR switching, and should be set slightly below the actual saturation amplitude (HDR should trigger before the AFE analog path saturates). HDR\_THR\_LOW is the accuracy threshold, the amplitude below which the distance accuracy is poor. Figure 20 shows an illustration of the HDR operation with distance. At a distance close to the sensor, the lower illumination DAC current is used. As the object moves away from the sensor, ILLUM\_DAC switches to a higher value once the amplitude falls below the lower threshold (HDR\_THR\_LOW). At the switching point, non-saturation is ensured by choosing the DAC currents according to Equation 3. As the object moves towards the sensor, ILLUM\_DAC switches to the lower value once the amplitude reaches the saturation level (HDR\_THR\_HIGH). At this transition, the amplitude with ILLUM\_DAC\_L is above HDR\_THR\_LOW.

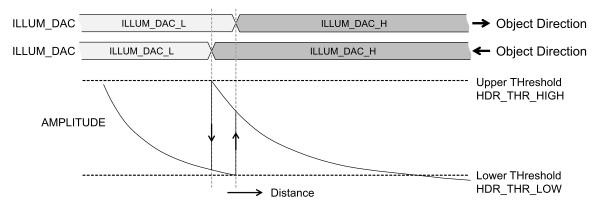


Figure 20. HDR Mode Operation With Distance

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#### **Table 3. HDR Mode Configuration Registers**

PARAMETER	ADDRESS	DESCRIPTION
EN_ADAPTIVE_HDR	2Ah[15]	Enable adaptive HDR mode.  Minimum number of sub-frames in a frame in this mode is 2 (NUM_SUB_FRAMES = 1)
SEL_HDR_MODE	2Ah[16]	Chooses which current to use when EN_ADAPTIVE_HDR = 0. 0 - ILLUM_DAC_L   1 - ILLUM_DAC_H
HDR_THR_HIGH	2Bh[15:0]	Saturation amplitude threshold of the auto HDR for high DAC current (ILLUM_DAC_H) Write a value of 27000
HDR_THR_LOW	2Ch[15:0]	Accuracy threshold of the auto HDR for low DAC current (ILLUM_DAC_L) = HDR_THR_HIGH × (ILLUM_DAC_L / ILLUM_DAC_H) × (1 / 1.2)
ILLUM_DAC_L_TX0	29h[4:0]	ILLUM_DAC_L of TX0 channel
ILLUM_DAC_H_TX0	29h[9:5]	ILLUM_DAC_H of TX0 channel
ILLUM_DAC_L_TX1	29h[14:10]	ILLUM_DAC_L of TX1 channel
ILLUM_DAC_H_TX1	29h[19:15]	ILLUM_DAC_H of TX1 channel
ILLUM_DAC_L_TX2	29h[23:20], 2Ah[23]	ILLUM_DAC_L of TX2 channel
ILLUM_DAC_H_TX2	2Ah[22:18]	ILLUM_DAC_H of TX2 channel

#### 7.3.1.5 Multi Channel Mode

The OPT3101 AFE supports up to three separate illumination channels. Only one illumination channel can be activated at a given point of time. In multi channel mode, the illumination driver switches current between different pins (TX0, TX1, and TX2) across samples. The sequence of switching is programmable (TX\_SEQ\_REG). In single channel mode, the channel to be used can be selected through SEL\_TX\_CH. Each illumination channel has separate current programmability, listed in Table 3. This mode can be combined with continuous mode, monoshot mode, non-HDR mode, or auto HDR mode.

**Table 4. Multi LED Configuration Registers** 

REGISTER	ADDRESS	DESCRIPTION
EN_TX_SWITCH	2Ah[0]	Enable switching between Illumination channels TX0, TX1, TX2.
SEL_TX_CH	2Ah[2:1]	Selects the ILLUM channels when switching is disabled.
TX_SEQ_REG	2Ah[14:3]	Stores the sequence of ILLUM channel switching in this register. For example, register value: 2-1-0-2-1-0. The sequence will be 0-1-2-0-1-2

Separate calibration registers are provided for each illumination channel to support different currents for each channel in the same system.

#### 7.3.2 AFE

The diode current is capacitively coupled to the AFE as shown in Figure 21. The AFE processes the input signal and produces digitized in-phase and quadrature-phase components of the input signal. The AFE has a full-scale current of 200 nA peak-to-peak and supports a photodiode capacitance up to 6 pF.

(5)



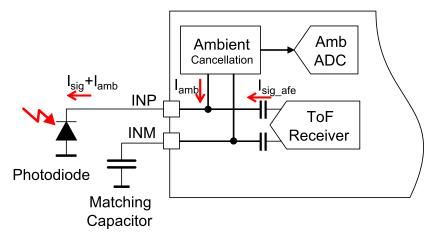


Figure 21. AFE, Photodiode Interface

The signal-to-noise ratio (SNR) for a given signal current and sample rate can be calculated from the following equation.

$$SNR = \frac{I_{SIG\_AFE}}{I_{noise} \times \sqrt{BW}} = \frac{I_{SIG\_AFE}}{94.8 \text{ pA} / \sqrt{(NUM\_AVG\_SUB\_FRAMES} + 1)}$$

#### where

- I<sub>sig afe</sub> = signal current entering the AFE
- I<sub>noise</sub> = Input referred current noise floor of the AFE = 1.5 pA/√Hz with I<sub>AMB MAX</sub>=20 μA and C<sub>PD</sub>= 2pF (Figure 2)

$$\sigma_{phase} = \frac{1}{SNR} radians$$

#### where

- σ<sub>phase</sub>= Phase standard deviation in radians
- SNR is calculated from Equation 4

$$\sigma_{\text{distance}} = \frac{c / (2f_{\text{MOD}})}{2\pi} \times \frac{1}{\text{SNR}} \text{meters}$$

#### where

- σ<sub>distance</sub>= Distance standard deviation in meters
- c = Speed of light

For example, with an AFE signal current of 20 nA peak-to-peak (–20 dBFS), frame rate of 125 Hz (NUM\_AVG\_SUB\_FRAMES = 31), SNR = 1193 = 61.5 dB. Depth noise standard deviation for this scenario is  $\sigma_{distance} = 15 \text{ m} / (2\pi) / 1193 = 2 \text{ mm}$ .

#### 7.3.3 Ambient Cancellation

The ambient cancellation circuit provides the dc and low-frequency diode current while biasing the diode at 1 V. Figure 22 shows the frequency response of the ambient cancellation circuit. A diode current with frequency below  $f_{c2}$  has second-order rejection. The corner frequency  $f_{c2}$  is designed to be at 50 kHz for IAMB\_MAX\_SEL = 0 (20  $\mu$ A ambient current support). Below frequency  $f_{c1}$  (approximately at 10 Hz), attenuation becomes first-order. So for a frequency of 1 kHz, the rejection would be (50 kHz / 1 kHz) × 2 = 2500 = 68 dB.

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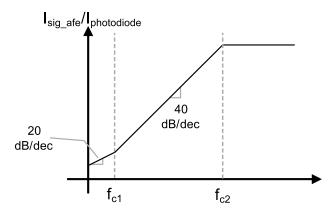


Figure 22. Ambient Cancellation Circuit Frequency Response

The maximum ambient current supported is programmable from 10  $\mu$ A to 200  $\mu$ A, listed in Table 5. Noise contribution from the ambient cancellation block increases with increase in ambient current support, shown in Figure 2. For low-ambient systems, the lower value of maximum ambient support should be used to reduce the noise contribution from the ambient cancellation. Ambient current is also converted to digital using an ADC (AMB\_DATA) at the output of the ambient cancellation block. Ambient ADC resolution is 0.104  $\mu$ A/LSB with 20- $\mu$ A support. Ambient ADC resolution scales linearly with maximum ambient current supported. Ambient current can be calculated from the AMB\_DATA using Equation 7.

$$I_{AMB} = \frac{AMB\_DATA - AMB\_CALIB}{192} \times I_{AMB\_MAX}$$

where

- I<sub>AMB MAX</sub>= Maximum ambient current supported. Listed in Table 5
- AMB\_CALIB = ambient ADC output in the dark. Typical value is 64, could vary by few codes from device to device.

**Table 5. Ambient Cancellation Register Settings** 

PARAMETER	ADDRESS	DESCRIPTION
IAMB_MAX_SEL	72h[7:4]	Selects the value of maximum ambient current support 0: 20 $\mu$ A   5: 10 $\mu$ A   10: 33 $\mu$ A   11: 50 $\mu$ A   12: 100 $\mu$ A   14: 200 $\mu$ A   Other values: Not valid

#### 7.3.4 Oscillator

The system clock is generated using an on-chip oscillator with high stability across temperature. This oscillator is trimmed to a nominal frequency of 80 MHz within ±3%. For accurate distance conversion, this frequency is trimmed digitally to 10-bit accuracy. Additionally, the device can accept an external reference clock and correct for the on-chip oscillator variations for continuous background frequency calibration.

#### **7.3.5 CLKGEN**

CLKGEN takes the clock from the oscillator and generates the clocks required for various blocks. CLKGEN generates a 10-MHz clock for the illumination driver. The phase of the illumination CLK can be changed in 16 steps. This feature is useful for phase nonlinearity correction resulting from square wave modulation. Phase nonlinearity from ideal square wave demodulation is approximately  $\pm 4$  degrees. OPT3101 has a filter to reject the higher-order harmonics of a square wave and the resulting nonlinearity is small,  $\pm 0.5$  degrees. For de-aliasing, CLKGEN also generates an additional frequency of 10  $\times$  (6 / 7) MHz or 10  $\times$  (6 / 5) MHz for the illumination clock.

Table 6. Register Settings to Change the Phase of Illumination

PARAMETER	ADDRESS	DESCRIPTION
SHIFT_ILLUM_PHASE	71h[6:3]	Mode to generate different Illumination clock phases. Illumination clock phase = SHIFT_ILLUM_PHASE × 22.5 degrees



#### 7.3.6 Illumination Driver

Figure 23 shows the illumination driver block diagram. The illumination driver supports three illumination channels. The same current source is multiplexed onto three channels. Only one channel can be used at any given time.

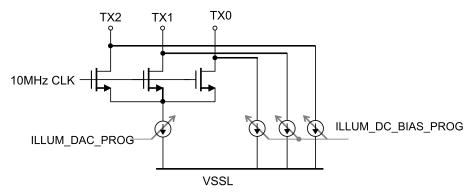


Figure 23. Illumination Driver Block Diagram

Illumination driver current can be programmed using a 5-bit DAC, listed in Table 7. Step size of the DAC can also be scaled from 1.4 mA to 5.6 mA using ILLUM\_SCALE. A dc bias-current option is also provided. DC bias is useful if the system requires a very small switching illumination current. This dc bias can be programmed in the range of 0.5 mA to 7.5 mA in steps of 0.5 mA using ILLUM\_DC\_CURR\_DAC.

**Table 7. Illumination Driver Register Settings** 

REGISTER	ADDRESS	DESCRIPTION
EN_LED_DRV	79h[0]	Enable the illumination driver
ILLUM_DAC_L_TX0	29h[4:0]	Illumination driver-current DAC register, ILLUM_DAC_L of TX0 channel. Illumination current = ILLUM_DAC_L_TX0 × DAC step
ILLUM_DAC_H_TX0	29h[9:5]	Illumination driver current DAC register, ILLUM_DAC_H of TX0 channel. Illumination current = ILLUM_DAC_L_TX0 × DAC step
ILLUM_SCALE_L_TX0	2Bh[18:16]	Scale the illumination current DAC step size for ILLUM_DAC_L_TX0 0: 5.6 mA   1: 4.2 mA   2: 2.8 mA   3: 1.4 mA   Other values: Not valid.
ILLUM_SCALE_H_TX0	2Bh[21:19]	Scale the illumination current DAC step size for ILLUM_DAC_H_TX0 0: 5.6 mA   1: 4.2 mA   2: 2.8 mA   3: 1.4 mA   Other values: Not valid.
ILLUM_DC_CURR_DAC	79h[11:8]	Program the illumination driver DC bias current DC current = 0.5 mA × ILLUM_DC_CURR_DAC

#### 7.3.7 Depth Engine

The depth engine computes the phase and amplitude from in-phase and quadrature-phase components of the received signal. The depth engine also performs the following calibrations:

- Phase offset
- Phase correction with temperature
- Crosstalk
- Frequency
- Square wave nonlinearity
- Phase correction with ambient

For a detailed calibration procedure, see OPT3101 Distance Sensor System Calibration

**Table 8. Phase Offset Correction Registers** 

PARAMETER	ADDRESS	DESCRIPTION
EN_PHASE_CORR	43h [0]	Enables phase offset correction
PHASE_OFFSET_HDR0_TX0	42h[15:0]	Phase offset for TX0 illumination channel with current of ILLUM_DAC_L_TX0
PHASE_OFFSET_HDR1_TX0	51h[15:0]	Phase offset for TX0 illumination channel with current of ILLUM_DAC_H_TX0



## **Table 8. Phase Offset Correction Registers (continued)**

PARAMETER	ADDRESS	DESCRIPTION
PHASE_OFFSET_HDR0_TX1	52h[15:0]	Phase offset for TX1 illumination channel with current of ILLUM_DAC_L_TX1
PHASE_OFFSET_HDR1_TX1	53h[15:0]	Phase offset for TX1 illumination channel with current of ILLUM_DAC_H_TX1
PHASE_OFFSET_HDR0_TX2	54h[15:0]	Phase offset for TX2 illumination channel with current of ILLUM_DAC_L_TX2
PHASE_OFFSET_HDR1_TX2	55h[15:0]	Phase offset for TX2 illumination channel with current of ILLUM_DAC_H_TX2

# **Table 9. Phase Temperature Coefficient Registers**

PARAMETER	ADDRESS	DESCRIPTION
EN_TEMP_CORR	43h[1]	Enable temperature correction
SCALE_PHASE_TEMP_COEFF	43h[8:6]	Adjust scale factor for temperature coefficient
TMAIN_CALIB_HDR0_TX0	47h[11:0]	Calibration temperature for sensor offset for TX0 illumination channel with current of ILLUM_DAC_L_TX0
TEMP_COEFF_MAIN_HDR0_TX0	45h[11:0]	Phase temperature coefficient for sensor temperature for TX0 illumination channel with current of ILLUM_DAC_L_TX0
TMAIN_CALIB_HDR1_TX0	48h[11:0]	Calibration temperature for sensor offset for TX0 illumination channel with current of ILLUM_DAC_H_TX0
TEMP_COEFF_MAIN_HDR1_TX0	2Dh[11:0]	Phase temperature coefficient for sensor temperature for TX0 illumination channel with current of ILLUM_DAC_H_TX0
TMAIN_CALIB_HDR0_TX1	49h[11:0]	Calibration temperature for sensor offset for TX1 illumination channel with current of ILLUM_DAC_L_TX1
TEMP_COEFF_MAIN_HDR0_TX1	2Dh[23:12]	Phase temperature coefficient for sensor temperature for TX1 illumination channel with current of ILLUM_DAC_L_TX1
TMAIN_CALIB_HDR1_TX1	41h[23:12]	Calibration temperature for sensor offset for TX1 illumination channel with current of ILLUM_DAC_H_TX1
TEMP_COEFF_MAIN_HDR1_TX1	2Fh[23:16], 30h[23:20]	Phase temperature coefficient for sensor temperature for TX1 illumination channel with current of ILLUM_DAC_H_TX1
TMAIN_CALIB_HDR0_TX2	3Fh[11:0]	Calibration temperature for sensor offset for TX2 illumination channel with current of ILLUM_DAC_L_TX2
TEMP_COEFF_MAIN_HDR0_TX2	31h[23:16], 32h[23:20]	Phase temperature coefficient for sensor temperature for TX2 illumination channel with current of ILLUM_DAC_L_TX2
TMAIN_CALIB_HDR1_TX2	45h[23:12]	Calibration temperature for sensor offset for TX2 illumination channel with current of ILLUM_DAC_H_TX2
TEMP_COEFF_MAIN_HDR1_TX2	33h[23:16], 34h[23:20]	Phase temperature coefficient for sensor temperature for TX2 illumination channel with current of ILLUM_DAC_H_TX2

Table 10. Phase Temperature Coefficient Registers for External Temperature Sensor

PARAMETER	ADDRESS	DESCRIPTION
TILLUM_CALIB_HDR0_TX0	47h[23:12]	Calibration temperature of external temperature sensor
TEMP_COEFF_ILLUM_HDR0_TX0	46h[11:0]	Phase temperature coefficient for illumination using external temperature sensor.
TILLUM_CALIB_HDR1_TX0	48h[23:12]	Calibration temperature of external temperature sensor
TEMP_COEFF_ILLUM_HDR1_TX0	51h[23:16], 52h[23:20]	Phase temperature coefficient for illumination using external temperature sensor.
TILLUM_CALIB_HDR0_TX1	49h[23:12]	Calibration temperature of external temperature sensor
TEMP_COEFF_ILLUM_HDR0_TX1	53h[23:16], 54h[23:20]	Phase temperature coefficient for illumination using external temperature sensor.
TILLUM_CALIB_HDR1_TX1	43h[23:12]	Calibration temperature of external temperature sensor
TEMP_COEFF_ILLUM_HDR1_TX1	55h[23:16], 56h[23:20]	Phase temperature coefficient for illumination using external temperature sensor.
TILLUM_CALIB_HDR0_TX2	3Fh[23:12]	Calibration temperature of external temperature sensor
TEMP_COEFF_ILLUM_HDR0_TX2	57h[23:16], 58h[23:20]	Phase temperature coefficient for illumination using external temperature sensor.
TILLUM_CALIB_HDR1_TX2	46h[23:12]	Calibration temperature of external temperature sensor



# Table 10. Phase Temperature Coefficient Registers for External Temperature Sensor (continued)

PARAMETER	ADDRESS	DESCRIPTION
TEMP_COEFF_ILLUM_HDR1_TX2	59h[23:16], 5Ah[23:20]	Phase temperature coefficient for illumination using external temperature sensor.

## **Table 11. Ambient-Dependent Phase Correction Registers**

REGISTER	ADDRESS	DESCRIPTION
AMB_PHASE_CORR_PWL_X0	B8h[9:0]	First knee point of PWL phase correction with ambient
AMB_PHASE_CORR_PWL_X1	B9h[19:10]	Second knee point of PWL phase correction with ambient
AMB_PHASE_CORR_PWL_X2	B9h[9:0]	Third knee point of PWL phase correction with ambient
AMB_PHASE_CORR_PWL_COEFF0	0Ch[23:16]	Slope of first segment for PWL phase correction with ambient
AMB_PHASE_CORR_PWL_COEFF1	B4h[7:0]	Slope of second segment for PWL phase correction with ambient
AMB_PHASE_CORR_PWL_COEFF2	B4h[15:8]	Slope of third segment for PWL phase correction with ambient
AMB_PHASE_CORR_PWL_COEFF3	B4h[23:16]	Slope of fourth segment for PWL phase correction with ambient
SCALE_AMB_PHASE_CORR_COEFF	B5h[2:0]	Scaling factor for ambient-based PWL phase correction.

# **Table 12. Internal Crosstalk Correction Registers**

REGISTER	ADDRESS	DESCRIPTION					
INT_XTALK_CALIB	2Eh[4]	The device initializes the internal electrical crosstalk measurement upon setting this bit.  Use the following sequence: INT_XTALK_CALIB = 1 Delay (at least 5 × 2 <sup>XTALK_FILT_TIME_CONST</sup> frames) INT_XTALK_CALIB = 0 See OPT3101 Distance Sensor System Calibration.					
XTALK_FILT_TIME_CONST	2Eh[23:20]	Time constant for crosstalk filtering. Time constant $\tau = 2^{\text{XTALK\_FILT\_TIME\_CONST}}$ frames. At least $5\tau$ should be allowed for settling of crosstalk measurement.					
USE_XTALK_FILT_INT	2Eh[5]	Select filter or direct sampling for internal crosstalk measurement.  0 – Direct sampling, 1 – Filter					
USE_XTALK_REG_INT	2Eh[6]	Select register value or internally calibrated value for internal crosstalk 0 – Calibration value, 1 – Register value					
IPHASE_XTALK_INT_REG	3D[15:0]	Register for in-phase component of internal crosstalk					
QPHASE_XTALK_INT_REG	3E[15:0]	Register for quadrature-phase component of internal crosstalk					
IPHASE_XTALK	3Bh[23:0]	Read-only register. In-phase component. Different values can be selected to be read out with IQ_READ_DATA_SEL					
QPHASE_XTALK	3Ch[23:0]	Read-only register. Quadrature-phase component. Different values can be selected to be read out with IQ_READ_DATA_SEL					
IQ_READ_DATA_SEL	2Eh[11:9]	Mux select for IPHASE_XTALK, QPHASE_XTALK 0 – Internal crosstalk   1 – Illum crosstalk   2 – Raw I, Q   3 – 16-bit frame counter					
INT_XTALK_REG_SCALE	2E[16:14]	Scale factor for internal crosstalk register (IPHASE_XTALK_INT_REG, QPHASE_XTALK_INT_REG). Scale = 2 <sup>INT_XTALK_REG_SCALE</sup>					

## **Table 13. Illumination Crosstalk Correction Registers**

REGISTER	ADDRESS	DESCRIPTION
ILLUM_XTALK_CALIB	2Eh[12]	The device initializes the illumination crosstalk measurement upon setting this bit. This measurement should be done with the photodiode masked such that no modulated light is received.  Use following sequence:  ILLUM_XTALK_CALIB = 1  Delay (at least 5 x 2 <sup>XTALK_FILT_TIME_CONST</sup> frames)  ILLUM_XTALK_CALIB = 0  See OPT3101 Distance Sensor System Calibration.
USE_XTALK_FILT_ILLUM	2Eh[7]	Select filter or direct sampling for illumination crosstalk measurement.  0 – Direct sampling, 1 – Filter



## Table 13. Illumination Crosstalk Correction Registers (continued)

REGISTER	ADDRESS	DESCRIPTION
USE_XTALK_REG_ ILLUM	2Eh[8]	Select register value or internally calibrated value for illumination crosstalk correction.  0 - Calibration value, 1 - Register value
ILLUM_XTALK_REG_SCALE	2E[19-17]	Scale factor for Illumination crosstalk register (IPHASE_XTALK_REG_HDR <i>&gt;_TX<j>, QPHASE_XTALK_REG_HDR<i>&gt;_TX<j>, i = 0,1, j = 0,1,2). Scale = 2INT_XTALK_REG_SCALE</j></i></j></i>
IPHASE_XTALK_REG_HDR0_TX0	2Fh[15:0]	Register for illumination crosstalk in-phase component for TX0 channel with ILLUM_DAC_L_TX0 current
QPHASE_XTALK_REG_HDR0_TX0	30h[15:0]	Register for illumination crosstalk quadrature-phase component for TX0 channel with ILLUM_DAC_L_TX0 current
IPHASE_XTALK_REG_HDR1_TX0	31h[15:0]	Register for illumination crosstalk in-phase component for TX0 channel with ILLUM_DAC_H_TX0 current
QPHASE_XTALK_REG_HDR1_TX0	32h[15:0]	Register for illumination crosstalk quadrature-phase component for TX0 channel with ILLUM_DAC_H_TX0 current
IPHASE_XTALK_REG_HDR0_TX1	33h[15:0]	Register for illumination crosstalk in-phase component for TX1 channel with ILLUM_DAC_L_TX1 current
QPHASE_XTALK_REG_HDR0_TX1	34h[15:0]	Register for illumination crosstalk in quadrature-phase component for TX1 channel with ILLUM_DAC_L_TX1 current
IPHASE_XTALK_REG_HDR1_TX1	35h[15:0]	Register for illumination crosstalk in-phase component for TX1 channel with ILLUM_DAC_H_TX1 current
QPHASE_XTALK_REG_HDR1_TX1	36h[15:0]	Register for illumination crosstalk quadrature-phase component for TX1 channel with ILLUM_DAC_H_TX1 current
IPHASE_XTALK_REG_HDR0_TX2	37h[15:0]	Register for illumination crosstalk in-phase component for TX2 channel with ILLUM_DAC_L_TX2 current
QPHASE_XTALK_REG_HDR0_TX2	38h[15:0]	Register for illumination crosstalk quadrature-phase component for TX2 channel with ILLUM_DAC_L_TX2 current
IPHASE_XTALK_REG_HDR1_TX2	39h[15:0]	Register for illumination crosstalk in-phase component for TX2 channel with ILLUM_DAC_H_TX2 current
QPHASE_XTALK_REG_HDR1_TX2	3Ah[15:0]	Register for illumination crosstalk quadrature-phase component for TX2 channel with ILLUM_DAC_H_TX2 current

## **Table 14. Frequency Correction Registers**

Table 141 Feducity Confession Regional								
REGISTER	ADDRESS	DESCRIPTION						
EN_AUTO_FREQ_COUNT	0Fh[21]	Determines which value to be used for frequency correction 0 – Trimmed value 1 – Measured value from frequency calibration						
EN_FLOOP	0Fh[22]	Enables the frequency calibration block.						
EN_FREQ_CORR	0Fh[23]	Enables frequency correction for the phase output						
REF_COUNT_LIMIT	0Fh[14:0]	This sets the limit for reference-clock count. Write this register with value = $(40 \times 10^6 / 2^{SYS\_CLK\_DIVIDER}) / f_{EXT}$						
SYS_CLK_DIVIDER	0Fh[20:17]	Programs system clock divider for frequency calibration. This should be adjusted to get it closer to the external reference frequency. The default is 10, system clock = 40 MHz / $2^{10}$ = 39.0625 kHz to bring close to 32.768 kHz.						
EN_CONT_FCALIB	10h[15]	Enables continuous frequency calibration.  0 – Frequency is measured only when START_FREQ_CALIB = 1  1 – Frequency is continuously measured.						
FREQ_COUNT_READ_REG	10h[14:0]	Read the register which holds the value of frequency calibration.						
START_FREQ_CALIB	0Fh[16]	Starts the frequency calibration.						

# **Table 15. Phase Nonlinearity Correction Registers**

REGISTER	ADDRESS	DESCRIPTION
EN_NL_CORR	4Ah[0]	Enables square wave non-linearity correction
SCALE_NL_CORR_COEFF	4Ah[19:18]	Scaling factor for nonlinearity correction coefficients (A*_COEFF_HDR*_TX*)
A0_COEFF_HDR0_TX0	4Ah[17:2]	Oth-order coefficient for square wave nonlinearity correction

(8)



Table 15. Phase Nonlinearity Correction Registers (continued)

REGISTER	ADDRESS	DESCRIPTION
A1_COEFF_HDR0_TX0	4Bh[15:0]	1st-order coefficient for square wave nonlinearity correction
A2_COEFF_HDR0_TX0	4Ch[15:0]	2nd-order coefficient for square wave nonlinearity correction
A3_COEFF_HDR0_TX0	4D[15:0]	3rd-order coefficient for square wave nonlinearity correction
A4_COEFF_HDR0_TX0	4Eh[15:0]	4th-order coefficient for square wave nonlinearity correction
A0_COEFF_HDR1_TX0	A2[15:0]	Oth-order coefficient for square wave nonlinearity correction
A1_COEFF_HDR1_TX0	A7[15:0]	1st-order coefficient for square wave nonlinearity correction
A2_COEFF_HDR1_TX0	AC[15:0]	2nd-order coefficient for square wave nonlinearity correction
A3_COEFF_HDR1_TX0	B1[15:0]	3rd-order coefficient for square wave nonlinearity correction
A4_COEFF_HDR1_TX0	AA[23:16], AB[23:16]	4th-order coefficient for square wave nonlinearity correction

### 7.3.8 Output Data

Phase and amplitude information is stored in registers which can be read out using the  $I^2C$  interface. The device gives data ready after computation of the depth information on the general purpose I/O (GP1 or GP2) which can be used trigger the host to read the data from the device. Distance can be calculated from the phase using Equation 8. A single code of PHASE\_OUT is 228.7 $\mu$ m.

$$\mbox{Distance} = \frac{\mbox{PHASE\_OUT}}{2^{16}} \times \frac{\mbox{c}}{2\mbox{f}_{\mbox{MOD}}} \mbox{meters}$$

where

- c = Speed of light
- f<sub>MOD</sub> = 10 MHz, modulation frequency

Along with phase and amplitude of the signal, ambient ADC output and temperature sensor output are also stored in the registers. All the output data is stored in contiguous registers 8, 9, and 10.

#### **Table 16. Output Data Registers**

REGIST ER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG 8	FRAME_COUNT0	AMB_OVL_FLAG	MOD_FREQ	FRAME_STATUS			HDR_MODE	PHASE_OVER_FLOW			РНА	SE_C	) TUC	15:8]					PH#	\SE_(	) ТИС	7:0]		
REG 9	DEA	ALIAS	s_BIN	[3:0]	PHASE _OVER FLOW_ F2	SIG_O VL_FL AG	EDAME COLINT 1				AM	/IP_O	UT[15	:8]					Αľ	МР_О	·UT[7:	0]		
REG 10			٦	ΓΜΑΙΝ	N[11:4				•	TMAI	N[3:0]	]	AM	IB_D/	ATA[9	:6]		ΑM	 1B_D/	ATA[5	i:0]		FRA COL 2	



**Table 17. Output Data Registers Description** 

FIELD	BIT	DESCRIPTION						
PHASE_OUT	08h[15:0]	Final calibrated phase.						
PHASE_OVERFLOW	08h[16]	Phase overflow during frequency correction.						
AMP_OUT	09h[15:0]	Amplitude of the signal.						
SIG_OVL_FLAG	09h[18]	Overload flag to indicate signal saturation						
AMB_OVL_FLAG	08h[22]	Overload flag to indicate ambient saturation						
HDR_MODE	08h[17]	Indicates the illumination driver DAC current used. 0: ILLUM_DAC_L   1: ILLUM_DAC_H						
TX_CHANNEL	08h[19:18]	Indicates which Illumination channel of TX0/TX1/TX2 is used.						
FRAME_STATUS	08h[20]	0 = Invalid frame   1= Valid frame. Frame can be invalid during crosstalk measurement.						
MOD_FREQ	08h[21]	Indicates the frequency used. 0: 10 MHz   1: De-alias frequency (10 MHz $\times$ 6 / 7 or 1 MHz $\times$ 6 / 5)						
FRAME_COUNT0	08h[23]	Frame counter LSB bit [0]						
FRAME_COUNT1	09h[17:16]	Frame counter bits [2:1]						
FRAME_COUNT2	0Ah[1:0]	Frame counter bits [4:3]. Frame counter = FRAME_COUNT2 × 8 + FRAME_COUNT1 × 2 + FRAME_COUNT0						
DEALIAS_BIN	09h[23:20]	Distance bin in de-alias mode						
PHASE_OVER_FLOW_F2	09h[19]	Phase overflow of second modulation frequency during frequency correction.						
AMB_DATA	0Ah[11:2]	Ambient ADC output. Indicates the ambient light. In no ambient light condition AMB_DATA is 64 typically.						
TMAIN	0Ah[23:12]	Temperature sensor output Temperature (°C) = (TMAIN / 8) – 256						

## 7.3.9 General Purpose I/O

There are two general purpose I/Os which can be used to bring out various digital signals like DATA\_RDY, FRAME\_VD, ILLUM\_CLK, ILLUM\_EN. GP2 can also be used as an input pin for external clock reference for device on-chip oscillator frequency calibration.

**Table 18. GPIO Configuration Registers** 

REGISTER	ADDRESS	DESCRIPTION
GPO1_MUX_SEL	78h[8:6]	Select signal for the GP1 output multiplexer.  0: DVSS   2: DIG_GPO_0   3: DIG_GPO_1   7: ILLUM_CLK   Other values: Not valid
GPIO1_OBUF_EN	78h[12]	Enable output buffer of GP1 pin
GPIO2_IBUF_EN	78h[16]	Enable input buffer of GP2 pin. External reference clock should be connected to this pin for frequency calibration.
GPIO2_OBUF_EN	78h[15]	Enable output buffer of GP2 pin
GPO2_MUX_SEL	78h[11:9]	Select signal for the GP2 output multiplexer. 0: DVSS   2: DIG_GPO_0   3: DIG_GPO_1   7: ILLUM_EN_TX0   Other values: Not valid
DIG_GPO_SEL0	0Bh[3:0]	Mux selection bits for digital signal DIG_GPO_0, which can be brought out on GP1 or GP2 0: FRAME_VD   1: SUB_VD   4: SEQUENCER_INTERRUPT 8: COMP_STATUS   9: DATA_RDY   10: FRAME_COUNTER_LSB   Other values: Not valid
DIG_GPO_SEL1	0Bh[7:4]	Mux selection bits for digital signal DIG_GPO_1 which can be brought out on GP1 or GP2 0: FRAME_VD   1: SUB-VD   4: SEQUENCER_INTERRUPT 8: COMP_STATUS   9: DATA_RDY   10: FRAME_COUNTER_LSB   Other values: Not valid

## 7.3.10 Temperature Sensor

The device has an internal temperature sensor to monitor the temperature of the sensor core. The temperature sensor has a range of –25°C to 125°C. The output of this temperature sensor is accessible from register TMAIN. It can be used for phase temperature compensation.



#### 7.3.11 On-Chip Regulator

AFE has an internal regulator for generating the 1.8-V supplies (AVDD, DVDD) from the AVDD3 supply. In this mode, only one 3.3-V supply is sufficient for the device operation. Because the power is drawn from the 3.3-V supply for AVDD, DVDD, power consumption is higher. The REG\_MODE pin controls the regulator. Connect this pin to IOVDD to enable regulator mode. In non-regulator mode, the REG\_MODE pin should be connected to IOVSS. Figure 177 show the block diagram of the regulator. A decoupling capacitor of 100 nF minimum should be connected at the pins AVDD and DVDD. The decoupling capacitor on AVDD should be connected to AVSS, and the decoupling capacitor on DVDD should be connected to IOVSS.

#### 7.3.12 Sequencer

AFE has an on-chip sequencer which can be used to perform various operations. The sequencer commands are tabulated in Table 19. Each instruction is 12 bits with the first four MSB bits as the opcode and next eight bit as operand. The sequencer can perform a comparison of amplitude or phase with register thresholds COMPARE\_REG1, COMPARE\_REG2 and generate a signal COMP\_STATUS, which can be observed on GP1 with the DIG\_GPO\_SEL0 = 8 and gpo1\_mux\_sel = 2 settings. The comparison input type can be selected using COMP\_IN\_SEL. The sequencer executes one command per sample. The sequencer interrupt to execute a command can be positioned either at the beginning of the sample or at the end of the sample after data is ready and before the next sample starts. The sequencer interrupt can be programmed with the TG\_SEQ\_INT\_START, TG\_SEQ\_INT\_END, TG\_SEQ\_INT\_MASK\_START, and TG\_SEQ\_INT\_MASK\_END registers. TG\_SEQ\_INT\_START and TG\_SEQ\_INT\_END define the position of the interrupt pulse within a sub-frame. TG\_SEQ\_INT\_MASK\_START and TG\_SEQ\_INT\_MASK\_END define the sub-frame during which the pulse is enabled.

Some of the use cases of the sequencer are:

- · Switching of transmitter channels
- Generating an interrupt based on a phase or amplitude comparison with defined thresholds
- · Generating an interrupt based on a phase or amplitude comparison with hysteresis
- Extending the dynamic range using four illumination driver currents
- Performing a de-alias operation to extend the distance range from 15 m to 75 m.

**Table 19. Sequencer Commands** 

OPCODE	FUNCTION	DESCRIPTION
0000	NOP	The operand indicates the number of cycles for which NOP should be executed. 0 means 1 cycle, 1 means 2 cycle, and so on. For example 0000-0000 1111 indicates that for the next 16 cycles the sequencer does not do anything.
0001	WRITE	This command writes the operand to the STATUS_OUT register. For example 0001-0110 0110 makes the value on the STATUS_OUT port 0110 01100. The STATUS_OUT port is mapped to certain key registers listed in Table 20. STATUS_OUT values override the register values only if EN_PROCESSOR_VALUES = 1.
0010	GOTO	Program counter (PC) goes to the line indicated by the operand. This command is useful for looping. The next command is executed on the next sequencer interrupt. For example, 0010-0000 0000 sets the PC to the first line of the program memory so that the instructions are executed in a loop.
0011	DGOTO	In this command, the PC goes to the line indicated by the operand only if STATUS_IN_REG bit is 1. If not, the PC stays in the same command until the STATUS_IN_REG register value becomes 1. The next command is executed on the next frame VD. For example, 0011-0000 0000 suspends the program until the STATUS_IN_REG bit is set to 1. Once it is set, the loop is restarted.
0100	DrGOTO	In this instruction, the PC goes to the line indicated by operand without any delay. This executes next instruction as well. The next command is executed on the same frame VD.
0101	COMP0	In this command, the CPU compares COMP_IN and COMPARE_REG1. If COMP_IN ≤ COMPARE_REG1, the program counter stays where it is and the COMP_STATUS port is 0. If the comparison fails, the program counter moves to the line indicated by the operand, and COMP_STATUS becomes 1.
0110	COMP0_INV	Similar to COMP but the comparison used is: COMP_IN ≥ COMPARE_REG2
0111	COMP_WINDOW	In this command, the PC stays at the same command forever. If (COMP_IN ≥ COMPARE_REG1) and (COMP_IN ≤ COMPARE_REG2) then COMP_STATUS becomes 1 else COMP_STATUS = 0.



#### **Table 19. Sequencer Commands (continued)**

OPCODE	FUNCTION	DESCRIPTION
1000	COMP2	If (COMP_IN ≥ COMPARE_REG1) and (COMP_IN ≤ COMPARE_REG2) then COMP_STATUS becomes 1 else COMP_STATUS = 0. If the condition is TRUE the program counter stays at the same command else moves to the line indicated by the operand.
1001	COMP3	Similar to COMP2. The difference is that regardless of the comparison result, the program counter moves to the instruction pointed to by the operand. If comparison is met, COMP_STATUS is set to 1, else to 0.
1010	COMP_HYST	In this command, the PC stays at the same command forever. There is hysteresis in the comparison. If (COMP_IN ≤ COMPARE_REG1) then COMP_STATUS = 0, elsif (COMP_IN ≥ COMPARE_REG2) then COMP_STATUS = 1.
1011	COMP1	In this command, the CPU compares COMP_IN and COMPARE_REG1. If COMP_IN ≤ COMPARE_REG1, the program counter stays where it is and the COMP_STATUS port is 0. If the comparison fails the program counter moves to the line indicated by the operand and COMP_STATUS becomes 1. Executes this command and moves to next command at the same interrupt.
1100	COMP1_INV	Similar to COMP1 but the comparison used is COMP_IN ≥ COMPARE_REG2. Sequencer executes the command and moves to next command at the same interrupt.
1101–1111	Not valid	

Table 20. Sequencer STATUS\_OUT Register Mapping

STATUS_OUT	REGISTER MAPPING
[0]	INT_XTALK_CALIB
[1]	EN_DEALIAS_MEAS
[2]	START_FREQ_CALIB
[4:3]	SEL_TX_CH
[5]	SEL_HDR_MODE
[7:6]	Invalid

**Table 21. Sequencer Registers** 

REGISTER	ADDRESS	DESCRIPTION							
COMP_IN_SEL	13h[2:0]	Select the value used for comp_in. 0: AMP_OUT   1: DEALIAS_BIN   2: Phase output in de-alias mode   3: PHASE_OUT							
COMPARE_REG1	13h[18:3]	Sequencer comparison threshold1							
COMPARE_REG2	14h[15:0]	Sequencer comparison threshold2							
EN_SEQUENCER	14h[16]	Enable the sequencer.							
EN_PROCESSOR_VALU 14h[17]		Uses processor values instead of register values.							
STATUS_IN_REG	14h[18]	The register is used to control the program flow in CPU							
DIS_INTERRUPT	14h[19]	Disables the interrupt which triggers the sequencer.							
COMMAND0 to COMMAND19	15h[11:0] to 1Eh[23:12]	Sequencer command registers. A total of 20 command registers are available.							

## 7.3.12.1 Interrupt Output

The sequencer supports various interrupt output modes using the comparison commands listed in Table 19. The register settings to use the sequencer for generating interrupt output using COMP\_WINDOW are listed in Table 22, and the corresponding interrupt output is shown in Figure 24. To use a comparison with hysteresis (COMP\_HYST) use COMMANDO = 0xA00 and the rest of the settings remain the same as when using COMP\_WINDOW.



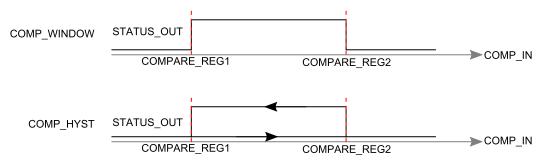


Figure 24. Interrupt Output Using Different Comparison Commands

Table 22. Register Settings to Use Sequencer for Generating Interrupt Output

PARAMETER	VALUE	DESCRIPTION								
Sequencer Interrupt Signal										
TG_SEQ_INT_START	9850									
TG_SEQ_INT_END	9858									
TG_SEQ_INT_MASK_START	NUM_AVG_SUB_FR AMES	Set the sequencer interrupt at the end of the last averaged sub- frame after data ready is available								
TG_SEQ_INT_MASK_END	NUM_AVG_SUB_FR AMES									
Sequencer Commands										
COMMAND0	0x700	COMP_WINDOW. COMP_STATUS = 1 when distance is between the lower (COMPARE_REG1) and upper (COMPARE_REG2) limits else COMP_STATUS = 0								
Get COMP_STATUS on GP1										
GPIO1_OBUF_EN	1	Enable GP1 output buffer.								
GPO1_MUX_SEL	3	Select DIG_GPO_1 on GP1								
GPO_SEL1	8	Select COMP_STATUS on DIG_GPO_1								
Comparison Settings										
COMP_IN_SEL	1	Select amplitude PHASE_OUT for comparison input COMP_IN								
COMPARE_REG1	PHASE1	Phase corresponding to a lower distance (phase) threshold								
COMPARE_REG2	PHASE2	Phase corresponding to an upper distance (phase) threshold								
Sequencer Enable										
EN_SEQUENCER	1	Enable the sequencer. Sequencer enable should be only be changed while TG_EN = 0. Before changing this register disable TG (TG_EN = 0), modify this register and then enable TG (TG_EN = 1).								
EN_PROCESSOR_VALUES	1	Enable processor values to control the STATUS_OUT register bits.								

## 7.3.12.2 Super-HDR Mode Using Sequencer

The on-chip sequencer can be used to extend the dynamic range using four illumination currents. Figure 25 shows the state diagram of the super-HDR mode implemented using the sequencer. For this example, the illumination driver currents should be programmed in the following order:  $I_{ILLUM\_H\_TX1} > I_{ILLUM\_L\_TX1} >$ 

- HDR\_THR\_HIGH × ILLUM\_DAC\_L\_TX0 / ILLUM\_DAC\_H\_TX0
- HDR\_THR\_HIGH × ILLUM\_DAC\_L\_TX1 / ILLUM\_DAC\_H\_TX1



## OPT3101 Sequencer controlled Switching Amplitude > COMPARE\_REG1 OPT3101 Auto HDR OPT3101 Auto HDR Amplitude > Amplitude > HDR\_THR\_HIGH HDR\_THR\_HIGH ILLUM\_ ILLUM\_ **ILLUM ILLUM** DAC\_H\_TX DAC\_H\_TX0 DAC\_L\_TX DAC L TXC Amplitude < HDR\_THR\_LOW Amplitude < HDR\_THR\_LOW

**OPT3101 Sequencer controlled Switching** 

Figure 25. Super-HDR Mode Using Sequencer: State Diagram

Amplitude < COMPARE\_REG2

Table 23. Register Settings to Use Sequencer for Super HDR Mode

PARAMETER	VALUE	DESCRIPTION						
Sequencer Interrupt Signal								
TG_SEQ_INT_START	9850							
TG_SEQ_INT_END	9858							
TG_SEQ_INT_MASK_START	NUM_AVG_SUB_FR AMES	Set the sequencer interrupt at the end of the last averaged sub- frame after data ready is available						
TG_SEQ_INT_MASK_END	NUM_AVG_SUB_FR AMES							
Sequencer Commands								
COMMAND0	0x108	Set illumination to channel TX1						
COMMAND1	0xB02	COMP1 command.  If COMP_IN > COMPARE_REG1, move to COMMAND2.						
COMMAND2	0x100	Set illumination to channel TX0						
COMMAND3	0xC00	COMP1_INV command. If COMP_IN < COMPARE_REG2, move to COMMAND0.						
Comparison Settings								
COMP_IN_SEL	0	Select amplitude AMP_OUT for COMP_IN						
COMPARE_REG1	HDR_THR_HIGH + 500	Should be greater than the hdr High threshold: HDR_THR_HIGH						
COMPARE_REG2	HDR_THR_LOW - 500	Should be less than the hdr low threshold HDR_THR_LOW.						
Sequencer Enable								
EN_SEQUENCER	1	Enable the sequencer. Sequencer enable should be only be changed while TG_EN = 0. Before changing this register, disable TG (TG_EN = 0), modify this register, and then enable TG (TG_EN = 1).						
EN_PROCESSOR_VALUES	1	Enable processor values to control the STATUS_OUT register bits.						



## 7.4 Programming

The OPT3101 device supports the I<sup>2</sup>C interface for register read and write access. The device also has an I<sup>2</sup>C host which can be used to interface with an external temperature sensor or external EEPROM.

#### 7.4.1 I<sup>2</sup>C Slave

The  $I^2C$  slave interface can be accessed with the SDA\_S and SLC\_S device pins. The  $I^2C$  interface supports bus speeds up to 400 kHz. The slave address for this device is  $1011A_2A_1A_0$ . Using the A0, A1, and A2 pins, the address can be configured. By default A0, A1 and A2 are pulled to the AVDD supply and the default address is 1011 111. To change the address, connect these pins to either the AVDD or AVSS supply. The register access can be single R/W or continuous R/W with auto-increment of register address.

Table 24. I<sup>2</sup>C Slave Configuration Registers

FIELD	BIT	DESCRIPTION
I2C_CONT_RW	00h[6]	Enable continuous read/write of registers using device I <sup>2</sup> C slave

The individual registers are 24-bit length in this device. However, the register read/write is in chunks of eight bits. After every 8-bit transfer, the slave expects an acknowledgement from the master in the case of read or gives out an acknowledgement in the case of write. Figure 26 shows the I<sup>2</sup>C timing for register write operation.

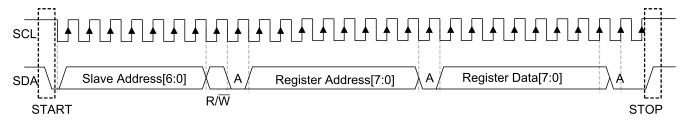


Figure 26. I<sup>2</sup>C Register Write Example

For example, to write 0x654321 to any register, the data should be split as three bytes and ordered as follows, 0x21, 0x43, 0x65. The same ordering is true for read mode. The first byte of data received corresponds to [7:0], followed by [15:8] and then followed by [23:16]. Figure 27 shows the different read/write modes.

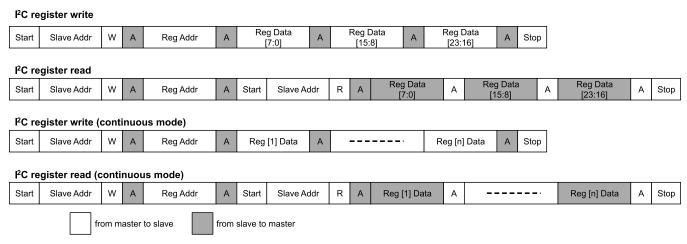


Figure 27. I<sup>2</sup>C Slave Interface R/W Modes

#### 7.4.2 I<sup>2</sup>C Master

The OPT3101 device also has an  $I^2C$  master, which is used to read the calibration and configuration registers from an external memory with the  $I^2C$  interface (EEPROM with  $I^2C$  address of 1010 000) during power up. It can also read temperature from an external temperature sensor with the  $I^2C$  interface (default address of 1001 000). Table 25 lists the register settings to configure the  $I^2C$  Host.



## Table 25. I<sup>2</sup>C Master Register Settings

PARAMETER	BIT	DESCRIPTION
TSENS_SLAVE0	02h[6:0]	I <sup>2</sup> C slave address. In multi-channel illumination operation, the temperature-sensor slave address is selected based on the channel being used for reading the external temperature value (TX0: TSENS_SLAVE0, TX1: TSENS_SLAVE1, TX2: TSENS_SLAVE2)
I2C_HOST_EN	01h[19]	Enable the I <sup>2</sup> C host
FRAME_VD_TRIG	01h[17]	Trigger I <sup>2</sup> C host operation every frame VD
I2C_TRIG_REG	01h[18]	Manual trigger the I <sup>2</sup> C host by writing to this register
I2C_NUM_TRAN	03h[17]	0: 1 transaction   1: 2 transactions
I2C_RW	01h[21:20]	0: Write   1: Read LSB: First transaction MSB: Second transaction
I2C_NUM_BYTES_TRAN1	07h[17:16]	0: 1 byte   1: 2 bytes
I2C_NUM_BYTES_TRAN2	05h[23:22]	0: 1 byte   1: 2 bytes
I2C_WRITE_DATA1	03h[16:9]	First byte of I <sup>2</sup> C write transaction 8-bit register address
I2C_WRITE_DATA2	07h[7:0]	Second byte of I <sup>2</sup> C write transaction 8-bit register data to be written
I2C_SEL_READ_BYTES	07h[19:18]	Selects the byte of read data. 0: 7:0   1: 15:8   2: 23:16   3: 31:24
I2C_READ_DATA	03h[7:0]	I <sup>2</sup> C host read data can be accessed through this register.

## 7.4.2.1 External Temperature Sensor

The temperature sensor address can be configured through internal registers (TSENS\_SLAVE0, TSENS\_SLAVE1, TSENS\_SLAVE2). This sensor can be used for calibrating the system parameters with temperature changes. An external temperature sensor is required if an external illumination driver is used. Typically the on-die temperature sensor is sufficient if the internal illumination driver is used. The temperature readings are refreshed every frame. The device supports up to three temperature sensors to associate with three illumination channels. A single- or two-byte read operation is performed on each of the temperature sensors to read the corresponding temperature. Tl's TMP102 device, 12-bit temperature sensor is suggested if accurate temperature correction with smaller jumps at the temperature code changes is required. The TMP103 8-bit temperature sensor can be used if the temperature-correction accuracy requirement is less. For temperature calibration of phase, the value read from the temperature sensor is assumed to be linear with the actual temperature. Register settings to configure the external temperature sensor read using the I<sup>2</sup>C host are listed in Table 26.

Table 26. Register Settings to Enable External Temperature Readout Using I<sup>2</sup>C master

PARAMETER	VALUE for TMP102	VALUE for TMP103A	DESCRIPTION				
TSENS_SLAVE0	0x48	0x70	I <sup>2</sup> C slave address of the external temperature sensor				
EN_TILLUM_READ	1	1	Enable reading of the external temperature sensor using the I <sup>2</sup> C master				
TEMP_AVG_ILLUM	0	2	0: no averaging for TMP102, this is already 12-bit data. Further averaging not required. 2: 4 averages for TMP103A				
I2C_HOST_EN	1	1	Enable I <sup>2</sup> C master				
I2C_NUM_TRAN	0	0	One read transaction				
I2C_RW	1	1	Read transaction				
I2C_NUM_BYTES_TRAN1	1	0	1: Two-byte read for the TMP102 device 0: One-byte read for the TMP103A device				
FRAME_VD_TRIG	1	1	Trigger temperature read for every frame				



Table 26. Register Settings to Enable External Temperature Readout Using I<sup>2</sup>C master (continued)

PARAMETER	VALUE for TMP102	VALUE for TMP103A	DESCRIPTION
CONFIG_TILLUM_MSB	8	0	Mode to select the correct 12 bits from the read 16 bits in a two-byte read for the TMP102 device
EN_TILLUM_12B	1	0	Enable the 12-bit mode to read 12-bit temperature sensor data from an external temperature sensor.

#### 7.4.2.2 External EEPROM

The I $^2$ C host of the OPT3101 device automatically loads all of the registers (256 bytes) from an external 2KB (256  $\times$  8) EEPROM on device reset to configure the device. Of these 256 bytes, 64 bytes are register address, and 192 bytes are data bytes. So from EEPROM, the device can auto load any of up to 64 device registers of 24 bits each (64  $\times$  24). EEPROM data should be written in the following format. If only part of the memory is used, the rest of the memory should be filled with all 0x00 or 0xFF.

Table 27. External EEPROM
Data Format

ADDRESS	DATA [7:0]					
0	Register address i					
1	Register data i[7:0]					
2	Register data i[15:8]					
3	Register data i[23:16]					
4	Register address j					
5	Register data j[7:0]					
6	Register data j[15:8]					
7	Register data j[23:16]					
	•••					
255	Register data k[23:16]					

The EEPROM I<sup>2</sup>C slave address should be 0x50h. On device reset, I<sup>2</sup>C host initiates auto load from the external EEPROM connected on the SDA\_M, SCL\_M bus. If there is an EEPROM device on the bus, this load operation performs the 256-byte read operation. If there is no EEPROM on the host bus, the device terminates auto load after the first transaction. During I<sup>2</sup>C host auto load, if an external host writes to the OPT3101 I<sup>2</sup>C slave, it acknowledges but data transfer does not happen (write/read). Register address 0 of the OPT3101 device cannot be loaded from the OPT3101 I<sup>2</sup>C host. Register address 0 is always reserved for I<sup>2</sup>C slave. By writing to register bit 0[22] (FORCE\_EN\_SLAVE) of the OPT3101 device, I<sup>2</sup>C slave can take control of register access from host auto load. If there are no pullup resistors connected on the I<sup>2</sup>C host bus SDA\_M and SCL\_M, then register bit 0[22] (FORCE\_EN\_SLAVE) = 1 should be written before any other I<sup>2</sup>C register writes, otherwise the device register read/write does not happen. If the device is to be used in monoshot mode, I<sup>2</sup>C host power down disable should be written first (DIS\_GLB\_PD\_I2CHOST) before writing monoshot mode enable (MONOSHOT\_MODE) bit in the EEPROM.

#### 7.4.2.3 External EEPROM Programming

To simplify the EEPROM programming in the end system, the OPT3101 device supports writing to EEPROM through the device I<sup>2</sup>C slave. The device auto loads from EEPROM on reset. Before programming EEPROM, this auto load might corrupt the registers. First erase the EEPROM and follow the flowchart shown in Figure 28. The register settings to write to external EEPROM on the OPT3101 I<sup>2</sup>C host through the OPT3101 I<sup>2</sup>C slave are listed in Table 28.



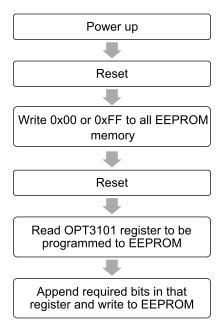


Figure 28. EEPROM Programming Flow Chart

Table 28. Register Settings to Write to External EEPROM Using I<sup>2</sup>C Master

PARAMETER	VALUE	DESCRIPTION							
TSENS_SLAVE0	50h	EEPROM I <sup>2</sup> C address. EEPROM with this I <sup>2</sup> C slave address should be used.							
I2C_HOST_EN	1	Enable device I <sup>2</sup> C host.							
I2C_NUM_TRAN	0	Number of I <sup>2</sup> C master transactions = 1							
I2C_RW	0	Write transaction							
I2C_NUM_BYTES_TRAN1	1	2-byte transaction (register address, register data)							
I2C_WRITE_DATA1		EEPROM register address							
I2C_WRITE_DATA2		Data to be written							
I2C_TRIG_REG	1 → 0	Trigger the I <sup>2</sup> C host write by writing 1 to this register and make it 0							

# TEXAS INSTRUMENTS

# 7.5 Register Maps

## 7.5.1 Serial Interface Register Map

## Table 29. Default Register Map

											29. D		9		-1-									
ADDRE SS (Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	MONO SHOT_ BIT	FORCE _EN_S LAVE	FORCE _EN_B YPASS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	I2C_C ONT_R W	0	0	0	0	0	SOFT WARE_ RESET
01h	0	0	I2C_	_RW	I2C_EN	I2C_TR IG_RE G	FRAME _VD_T RIG	0	0	0 0 0 0 0 0 0 ADDR_SLAVE_EEPROM									SWAP_ READ_ DATA	EEPRO M_REA D_TRI G				
02h	TEMP_A	VG_ILLU M	EN_TIL LUM_R EAD			TS	ENS_SLAV	/E2		TSENS_SLAVE1 TSENS_SLAVE0														
03h		NVG_MAI	0	0	0	0	I2C_NU M_TRA N			INIT_L OAD_D I2C_READ_DATA ONE														
04h	TILLUM _UNSI GNED	0	0	0			,			TILLUM 0 0 0 1 0 1 1							1							
05h		M_BYTE RAN2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
07h	С	ONFIG_TI	LLUM_MS	В		_READ_ TES	I2C_NUM S_TR	M_BYTE RAN1	0	0	0	0	0	0	0	0	I2C_WRITE_DATA2							
08h	FRAME _COUN T0	AMB_O VL_FL AG	MOD_F REQ	FRAME _STAT US	TX_CH	HANNEL	HDR_M ODE	PHASE _OVER _FLOW		1		1		1		PHASI	E_OUT							
09h		DEALI	AS_BIN		PHASE _OVER _FLOW _F2	SIG_O VL_FL AG	FRAME_	COUNT								AMP.	_OUT							
0Ah					1	ТМ	AIN				AMB_DATA FRAM								FRAME	_COUNT				
0Bh					AMB_	CALIB				DIG_GPO_SEL2 0 0 DIG_GPO_SEL1 DIG_GPO_SEL								PO_SEL0						
0Ch			AMB_PF	IASE_CO	RR_PWL_	COEFF0					AMB_	XTALK_Q	PHASE_C	OEFF	•				AMB.	_XTALK_I	PHASE_C	OEFF		
0Dh	EN_TIL LUM_1 2B	0	0	0	0	0	0					AMB_S	AT_THR					0	0	0	0	0	0	0
0Fh	EN_FR EQ_CO RR	EN_FL OOP	EN_AU TO_FR EQ_CO UNT		SYS_CLK	(_DIVIDER		START _FREQ _CALIB	0	REF_COUNT_LIMIT									•					
10h			AMP	LITUDE_	MIN_THR[	[15:8]	EN_CO NT_FC FREQ_COUNT_READ_REG  ALIB																	
11h			AMF	PLITUDE_	_MIN_THR	[7:0]			DIS_O VL_GA TING							FREC	Q_COUNT	Γ_REG						

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## Table 29. Default Register Map (continued)

	Table 29. Default Register Map (Continued)																								
ADDRE																									
SS (Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
13h	0	0	0	0	0						- 10		COMPARE_REG1 MUX_SEL_COMPIN												
	DIS_IN STATU EN_PR EN_SE									1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2															
										COMPARE_REG2															
14h	0	0	0	0	PT	EG	OR_VA LUES	CER									_								
15h	COMMAND1												COMMANDO												
16h	COMMAND3												COMMAND2												
17h	COMMAND5												COMMAND4												
18h	COMMAND7																	COM	MAND6						
19h	COMMAND9																	COM	MAND8						
1Ah	COMMAND11																	COMM	AND10						
1Bh	COMMAND13																	COMM	AND12						
1Ch	COMMAND15												COMMAND14												
1Dh	COMMAND17												COMMAND16												
1Eh	COMMAND19											COMMAND18													
26h	POWERUP_DELAY													0	0	0	0	0	0	1	1	1	1		
27h							МС	NOSHOT	_FZ_CLKC	CNT			MONOSHOT_NUMFRAME MONOSHOT_DE												
29h	ILI	LUM_DAC	C_L_TX2[4	k:1]		ILLU	M_DAC_H	_TX1			ILLU	JM_DAC_L	L_TX1 ILLUM_DAC_H_TX0 ILLUM_DAC_L_TX0												
2Ah									EN_AD APTIVE _HDR	APTĪVE TX_SEQ_REG SEL_TX_CH SWIT															
2Bh	0	0	ILLUM	1_SCALE	H TX0	ILLUM	I_SCALE_		_				HDR_THR_HIGH												
2Ch	0	0		 1_SCALE			SCALE_						HDR_THR_LOW												
2Dh		II.	II.		TEMP	_COEFF_N	MAIN_HDF	R0_TX1					TEMP_COEFF_MAIN_HDR1_TX0												
2Eh	XTALK_FILT_TIME_CONST											IQ_READ_DATA_SEL USE_X USE_X USE_X TALK_ T					CE_SCAL	CE_SCALE_VAL							
2Fh			TEMP C	OEFF M	AIN HDR1	_TX1[11:4]							IPHASE_XTALK_REG_HDR0_TX0												
	TEMP C	OEFF_MA			1	,																			
30h			]		0	0	0	0					QPHASE_XTALK_REG_HDR0_TX0												
31h			TEMP_C	OEFF_M/	AIN_HDR0	_TX2[11:4]	ı	I					IPHASE_XTALK_REG_HDR1_TX0												
32h	TEMP_C	OEFF_MA	AIN_HDRO	)_TX2[3:0	0	0	0	0					QPHASE_XTALK_REG_HDR1_TX0												
33h	TEMP_COEFF_MAIN_HDR1_TX2[11:4]											IPHASE_XTALK_REG_HDR0_TX1													
	TEMP_COEFF_MAIN_HDR1_TX2[3:0																								
34h		] 0 0 0 0										QPHASE_XTALK_REG_HDR0_TX1													
35h	0 0 0 0 0 0 0										IPHASE_XTALK_REG_HDR1_TX1														
36h	TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR0_TX0											QPHASE_XTALK_REG_HDR1_TX1													
37h	TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR0_TX0										IPHASE_XTALK_REG_HDR0_TX2														
38h	TEMP_COEFF_XTALK_IPHASE_HDR0_TX0									QPHASE_XTALK_REG_HDR0_TX2															
39h	TEMP_COEFF_XTALK_QPHASE_HDR0_TX0														IPHAS	SE_XTALK	_REG_HD	R1_TX2							

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# **Table 29. Default Register Map (continued)**

ADDRESS   PRINCE													· vog.oc		. (		-,								
SCALE_AMB_COEFF_XTA	SS	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	Da	D8	D7	De	D5	D4	D3	D2	D1	D0
SCALE AMB_COFF_XTA   MR_ATT   MR_ATT	(I ICA)	D23	DZZ	DZI	D20	Dia	Dio	DII		DIS	D14	DIS	DIZ	DII	DIU	Da	D0	DI .	D0	D3	D4	- 53	DZ	Di	D0
SCH	3Ah	SCALE_AMB_COEFF_XT   SCALE_TEMP_COEFF_XT   MP_XT   ALK   ALK_C									QPHASE_XTALK_REG_HDR1_TX2														
SCh	3Bh								1				IPHASE	_XTALK											
Sph   0   0   0   0   0   0   0   0   0	3Ch																								
Seh   0   0   0   0   0   0   0   0   0		0	0	0	0	0	0	0	0							IPH	IASE XTA	LK INT F	REG						
SPh	3Eh	0	0	0	0	0	0	0	0																
No.   Color   Color	3Fh																								
42h	40h	0	LTI_FR EQ_PH																0	0	EN_DE ALIAS_ MEAS				
STATE   STAT	41h	TMAIN_CALIB_HDR1_TX1 BETA1_DEALIAS_SCALE ALPHA1_DEALIAS_SCALE																							
A3h	42h	0	0	0	0	0	0	0	0							PHA	SE_OFFS	ET_HDR0	_TX0						
45h	43h										0 SCALE_PHASE_TEMP_CO								0	MP_CO	EN_PH ASE_C ORR				
46h	44h	0	0	0	0	0	0	0	0							PHAS	SE2_OFFS	SET_HDR	D_TX0						
47h	45h					TM	IAIN_CALI	B_HDR1_	TX2					TEMP_COEFF_MAIN_HDR0_TX0											
A8h	46h					TIL	LUM_CAL	IB_HDR1_	TX2					TEMP_COEFF_ILLUM_HDR0_TX0											
A9h	47h					TIL	LUM_CAL	IB_HDR0_	TX0					TMAIN_CALIB_HDR0_TX0											
AAA	48h					TIL	LUM_CAL	IB_HDR1_	TX0					TMAIN_CALIB_HDR1_TX0											
4Ah 0 0 0 0 0 0 R_COEFF	49h					TIL	LUM_CAL	IB_HDR0_	TX1									TN	AIN_CALI	B_HDR0_	TX1				
4Ch 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	4Ah	0	0	0	0																				EN_NL _CORR
4Dh 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	4Bh	0	0	0	0	0	0	0	0							Α	1_COEFF	_HDR0_T	X0						
Align   Color   Colo	4Ch	0	0	0	0	0	0	0	0							Α	2_COEFF	_HDR0_T	X0						
OVER	4Dh	0	0	0	0	0	0	0	0							Α	3_COEFF	_HDR0_T	X0						
Temp_Coeff_Illum_Hdrrl_Tx1[3]   Temp_Coeff_Illum_Hdrrl_Tx1[11:4]   Temp_Coeff_Illum_Hdrrl_Tx1[3]   Temp_Coeff_Illum_Hdrrl_Tx	4Eh	0	0	0	0	0	0	0	0							Α	4_COEFF	_HDR0_T	X0						
52h         TEMP_COEFF_ILLUM_HDR1_TX0[3: 0]         0         0         0         PHASE_OFFSET_HDR0_TX1           53h         TEMP_COEFF_ILLUM_HDR0_TX1[11:4]         PHASE_OFFSET_HDR1_TX1           54h         TEMP_COEFF_ILLUM_HDR0_TX1[3: 0]         0         0         0           55h         TEMP_COEFF_ILLUM_HDR1_TX1[11:4]         PHASE_OFFSET_HDR1_TX2           56h         TEMP_COEFF_ILLUM_HDR1_TX1[3: 0]         0         0         0	50h	0	IDE_CL KGEN_	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	MODE_ OFFSE	MODE_	MODE_	CLIP_ MODE_ FC
52h         0]         0	51h		1	TEMP_CC	DEFF_ILLU	JM_HDR1	_TX0[11:4	.]	1		1	1	-			PHA	SE_OFFS	ET_HDR1	_TX0			1	I	1	1
54h         TEMP_COEFF_ILLUM_HDR0_TX1[3: 0]         0         0         0         0         PHASE_OFFSET_HDR0_TX2           55h         TEMP_COEFF_ILLUM_HDR1_TX1[11:4]         PHASE_OFFSET_HDR1_TX2           56h         TEMP_COEFF_ILLUM_HDR1_TX1[3: 0]         0         0         0         0         PHASE2_OFFSET_HDR1_TX0	52h																								
54h         0]         0         0         0         0         0         PHASE_OFFSET_HDRU_TAZ           55h         TEMP_COEFF_ILLUM_HDR1_TX1[11:4]         PHASE_OFFSET_HDR1_TX2           56h         TEMP_COEFF_ILLUM_HDR1_TX1[3:         0         0         0         0         PHASE2_OFFSET_HDR1_TX0	53h			TEMP_CC	DEFF_ILLU	JM_HDR0	_TX1[11:4	.]								PHA	SE_OFFS	ET_HDR1	_TX1						
56h         TEMP_COEFF_ILLUM_HDR1_TX1[3: 0]         0         0         0         0         PHASE2_OFFSET_HDR1_TX0	54h										PHASE_OFFSET_HDR0_TX2														
56h 0] 0 0 0 0 PHASEZ_OFFSET_HDR1_1X0	55h	TEMP_COEFF_ILLUM_HDR1_TX1[11:4] PHASE_OFFSET_HDR1_TX2																							
57h TEMP_COEFF_ILLUM_HDR0_TX2[11:4] PHASE2_OFFSET_HDR0_TX1	56h										PHASE2_OFFSET_HDR1_TX0														
	57h	TEMP_COEFF_ILLUM_HDR0_TX2[11:4]														PHAS	SE2_OFFS	SET_HDR	D_TX1						

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# **Table 29. Default Register Map (continued)**

								1				tog.or		,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		,	1	1	1	1				
ADDRE																								
SS (Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
58h	TEMP_C	COEFF_ILL	LUM_HDF	R0_TX2[3:	0	0	0	0							PHAS	SE2_OFFS	SET_HDR1	I_TX1						
59h				OEFF ILL	UM_HDR1_	TX2[11:4		Ŭ							PHAS	SE2_OFFS	SET HDRO	) TX2						
	TEMP_C	COEFF_ILL																						
5Ah		(	0]		0	0	0	0								SE2_OFFS	SEI_HDK	1_1 X2						
5Bh		TEMP	_COEFF	_ILLUM_X	TALK_IPHA	SE_HDR	1_TX1			TEMF	_COEFF_	_ILLUM_X	TALK_IPH	ASE_HDR	0_TX1			TEMP	_COEFF_	ILLUM_X	TALK_IPH	ASE_HDR	1_TX0	
5Ch					TALK_QPH							_ILLUM_X									TALK_IPH			
5Dh					TALK_QPH							ILLUM_XT									TALK_QPF			
5Eh					K_IPHASE_							FF_XTAL									TALK_QPF			
5Fh					K_IPHASE_							FF_XTAL									K_IPHASE			
60h			MP_COE	1	K_QPHASE		1	1				FF_XTAL									K_QPHAS			
61h	0	0	0	0	0	0	0	0				FF_XTAL	1	ı	1			1	1	1	K_QPHAS		1	1
64h		_OVLDET	_REFM	PROG	S_OVLDET_	REFP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
65h	DIS_O VLDET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6Eh	0	0	0	0	EN_TE MP_CO NV	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OEII	U	U	0	U	INV		UNMA			U	U	U	U	U	U	U	U	U	U	U	U	U	U	0
71h	0	0	0	0	0	0	SK_ILL UMEN_ INTXTA LK	EN_ILL UM_CL K_GPI O	ILLUM_ CLK_G PIO_M ODE	0	0	DIS_IL LUM_C LK_TX	INVER T_AFE _CLK	0	INVER T_TG_ CLK	SHUT_ CLOCK S	0	S	SHIFT_ILLI	UM_PHAS	SE	DEALIA S_FRE Q	DEALIA S_EN	0
72h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		IAMB_N	IAX_SEL		0	0	0	0
76h	0	0	0	0	0	0	0	0	0	0	0	0	PDN_G LOBAL	0	DIS_GL B_PD_I 2CHOS T	DIS_GL B_PD_ OSC	RESER VED	DIS_GL B_PD_ AMB_A DC	DIS_GL B_PD_ AMB_D AC	DIS_GL B_PD_ AFE_D AC	DIS_GL B_PD_ AFE	DIS_GL B_PD_I LLUM_ DRV	DIS_GL B_PD_ TEMP_ SENS	DIS_GL B_PD_ REFSY S
77h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EN_DY N_PD_I 2CHOS T_OSC	EN_DY N_PD_ OSC	RESER VED	EN_DY N_PD_ AMB_A DC	EN_DY N_PD_ AMB_D AC	EN_DY N_PD_ AFE_D AC	EN_DY N_PD_ AFE	EN_DY N_PD_I LLUM_ DRV	EN_DY N_PD_ TEMP_ SENS	EN_DY N_PD_ REFSY S
78h	0	SEL_G P3_ON _SDAM	0	0	0	0	0	GPIO2 _IBUF_ EN	GPIO2 _OBUF _EN	0	GPIO1 _IBUF_ EN	GPIO1 _OBUF _EN	GP	O2_MUX_	SEL	GP	O1_MUX_	SEL	0	0	0	GP	O3_MUX_	SEL
79h	0	0	0	0	PDN_IL LUM_D RV	0	0	0	0	0	0	PDN_IL LUM_D C_CUR R	IL	LUM_DC_	_CURR_D/	AC	0	0	0	EN_TX _DC_C URR_A LL	SEL_IL LUM_T X0_ON _TX1	EN_TX _CLKZ	0	EN_TX _CLKB
7Ah	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		N_CONFI	TX2_PII	N_CONFI G	TX1_PIN	N_CONFI G
80h	DIS_T G_ACO NF	0	0	0	0	0	0				•	•	•		SUB_VD_	_CLK_CNT	-							TG_EN
83h	0	0	0	0	0	0	0	0							1	ΓG_AFE_R	ST STAR	T						1
84h	0	0	0	0	0	0	0	0								TG_AFE_								
85h	0	0	0	0	0	0	0	0																
	·	I	L		1		1		1															

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# Table 29. Default Register Map (continued)

ADDRE																								i
SS	Doo	Doo	D04	Doo	D40	D40	D47	D40	D45	D44	D40	D40	D44	D40	<b>D</b> 0	<b>D</b> 0	D7	<b>D</b> 0	D.F.	D4	<b>D</b> 0	<b>D</b> 0	<b>D4</b>	<b>D</b> 0
( <b>Hex</b> ) 86h	<b>D23</b>	<b>D22</b>	<b>D21</b>	<b>D20</b>	<b>D19</b>	<b>D18</b>	<b>D17</b>	<b>D16</b>	D15	D14	D13	D12	D11	D10	D9	TG_SEQ	D7	D6	D5	D4	D3	D2	D1	D0
87h	0	0	0	0	0	0	0	0							7	TG_SEQ_								
88h	0	0	0	0	0	0	0	0								TG_CAPT								-
89h	0	0	0	0	0	0	0	0								_OVL_WIN								
8Ah	0	0	0	0	0	0	0	0								G_OVL_WI								
8Fh	0	0	0	0	0	0	0	0								TG_ILLUM								
90h	0	0	0	0	0	0	0	0								TG_ILLUN								
91h	0	0	0	0	0	0	0	0								TG_CAL								
92h	0	0	0	0	0	0	0	0								TG_CAI								
93h	0	0	0	0	0	0	0	0								TG_DYNPI		Т						
94h	0	0	0	0	0	0	0	0								TG_DYNF	PDN_END							
97h			1		TG	_SEQ_INT	_MASK_E	ND									TG_	SEQ_INT	_MASK_S	ΓART				
98h					TG_	_CAPTURI	E_MASK_I	END									TG_C	CAPTURE	_MASK_S	TART				
99h					TG_O	VL_WIND	OW_MASH	_END									TG_OV	L_WINDO	DW_MASK	_START				
9Ch					TG	_ILLUMEN	I_MASK_E	ND									TG_I	ILLUMEN	_MASK_S	TART				
9Dh					Т	G_CALC_	MASK_EN	D									TG	_CALC_N	MASK_STA	RT				
9Eh					TG	_DYNPDN	I_MASK_E	ND									TG_	DYNPDN.	_MASK_S	TART				
9Fh					NU	M_AVG_S	UB_FRAN	1ES									1	NUM_SUI	B_FRAME	S				
A0h	0	0	0	0	0	0	0	0								CAPTURE	_CLK_CN	Т						
A2h			A3_0	COEFF_H	DR0_TX1[	[15:8]									Д	NO_COEFF	_HDR1_T	X0						
A3h			A3_	COEFF_H	IDR0_TX1	[7:0]									Д	NO_COEFF	_HDR0_T	X1						
A4h			A3_0	COEFF_H	DR1_TX1[	[15:8]									Δ	NO_COEFF	_HDR1_T	X1						
A5h			A3_	COEFF_H	IDR1_TX1	[7:0]									Α	NO_COEFF	_HDR0_T	X2						
A6h					DR0_TX2[										Д	NO_COEFF	_HDR1_T	X2						
A7h					IDR0_TX2											A1_COEFF								
A8h					DR1_TX2[											A1_COEFF								
A9h					IDR1_TX2											A1_COEFF								
AAh					DR1_TX0[											A1_COEFF								
ABh					IDR1_TX0											\1_COEFF								
ACh					DR0_TX1[											12_COEFF								
ADh					IDR0_TX1											12_COEFF								
AEh					DR1_TX1[											12_COEFF								
AFh					IDR1_TX1											12_COEFF								
B0h B1h					DR0_TX2[											A2_COEFF A3_COEFF								
B2h	0	0	0	0	IDR0_TX2	0	0	0								4_COEFF								
B2n B4h	U	U		_	RR_PWL_		U	U			AMP DI	HASE CO	RR_PWL_	COEEE2	P	v+_COEFF	יואטני_[]	^∠	AMP DI	HASE_CO	RR D\\/I	COEEE1		
D411			AIVID_PF	INSE_CO	IXIX_F VVL_	COEFF3					AIVID_PI	INSE_CO	IXIX_FVVL_	OUEFFZ									_AMB_PHA	ASE CO
B5h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		RR_COEFF	

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# Table 29. Default Register Map (continued)

ADDRE SS (Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
B8h	0	0	0	GIVE_ DEALIA S_DAT A				AMB_	PHASE_C	ORR_PW	'L_X1							AMB_	_PHASE_0	CORR_PW	/L_X0			
B9h	ILLUM	_SCALE_	H_TX2	ILLUM	_SCALE_	L_TX2	AMB_AD		AMB_AD0		AMB_AC		EN_TX 2_ON_ TX0	EN_TX 1_ON_ TX0				AMB_	_PHASE_(	CORR_PW	/L_X2			



### 7.5.1.1 Register Descriptions

#### **Table 30. Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default	Value	
-n		Value after reset or the default value

### 7.5.1.1.1 Register 0h (Address = 0h) [reset = 0h]

### Figure 29. Register 0h

23	22	21	20	19	18	17	16
MONOSHOT_B		FORCE_EN_B YPASS			RESERVED		
R/W - 0h	R/W - 0h	R/W - 0h			R/W - 0h		
15	14	13	12	11	10	9	8
			RESERVED				0
			R/W	/ - 0h			
7	6	5	4	3	2	1	0
0	I2C_CONT_R W			RESERVED			SOFTWARE_R ESET
R/W - 0h	R/W - 0h			R/W - 0h			R/W - 0h

### Table 31. Register 00 Field Descriptions

Bit	Field	Туре	Reset	Description
23	MONOSHOT_BIT	R/W	0h	Monoshot trigger register. Write a 1 to this bit to start sample capture in monoshot mode. This bit is auto cleared after the sample capture completion.
22	FORCE_EN_SLAVE	R/W	0h	Setting this bit to 1 enables I <sup>2</sup> C slave register access from the device I <sup>2</sup> C host for any address. Set this bit to 1 when the SDA_M and SCL_M pins are left floating.
21	FORCE_EN_BYPASS	R/W	0h	Setting this bit to 1 disables the device I <sup>2</sup> C host and shorts the I <sup>2</sup> C host bus and I <sup>2</sup> C slave bus.
20:7	RESERVED	R/W	0h	Always read or write 0h.
6	I2C_CONT_RW	R/W	0h	Enable continuous read/write of the device I <sup>2</sup> C slave registers.
5:1	RESERVED	R/W	0h	Always read or write 0h.
0	SOFTWARE_RESET	R/W	0h	Generates a device reset on writing this bit and resets all the register settings to default values, including this bit.

# 7.5.1.1.2 Register 1h (Address = 1h) [reset = 120140h]

### Figure 30. Register 1h

23	22	21	20	19	18	17	16
RESERVED	0	I2C	_RW	I2C_EN	I2C_TRIG_RE G	FRAME_VD_T RIG	RESERVED
R/W - 0h	R/W - 0h	R/W	/ - 1h	R/W - 0h	R/W - 0h	R/W - 1h	R/W - 0h
15	14	13	12	11	10	9	8
			RESERVED				ADDR_SLAVE _EEPROM
			R/W - 0h				R/W - 1h



	7	6	5	4	3	2	1	0
			ADDR_SLA\	VE_EEPROM			SWAP_READ_ DATA	RESERVED
İ			R/W	- 10h			R/W - 0h	R/W - 0h

#### **Table 32. Register 01 Field Descriptions**

Bit	Field	Туре	Reset	Description
23	RESERVED	R/W	0h	Always read or write 0h.
21:20	I2C_RW	R/W	1h	Chooses R/W for I <sup>2</sup> C host operation. 0: Write   1: Read LSB: first transaction, MSB: second transaction
19	I2C_EN	R/W	0h	Enables the I <sup>2</sup> C host.
18	I2C_TRIG_REG	R/W	0h	The trigger register for I <sup>2</sup> C transactions
17	FRAME_VD_TRIG	R/W	1h	When this bit is 1, the I <sup>2</sup> C host is triggered on every sample start. Else it is triggered based on the setting of I2C_TRIG_REG.
16:9	RESERVED	R/W	0h	Always read or write 0h.
8:2	ADDR_SLAVE_EEPROM	R/W	50h	External EEPROM I <sup>2</sup> C slave address.
1	SWAP_READ_DATA	R/W	0h	Setting this bit to 1 reverses the data read by I <sup>2</sup> C host from [7:0] to [0:7].
0	RESERVED	R/W	0h	Always read or write 0h.

### 7.5.1.1.3 Register 2h (Address = 2h) [reset = 92A4C8h]

### Figure 31. Register 2h

23	22	21	20	19	18	17	16				
TEMP_AV	/G_ILLUM	EN_TILLUM_R EAD			TSENS_SLAVE2						
R/W	- 2h	R/W - 0h									
15	14	13	12	11	10	9	8				
TSENS_	SLAVE2			TSENS_	SLAVE1						
R/W	- 2h			R/W	- 24h						
7	6	5	4	3	2	1	0				
TSENS_SLAVE 1	·	TSENS_SLAVE0									
R/W - 1h		R/W - 48h									

### Table 33. Register 02 Field Descriptions

Bit	Field	Туре	Reset	Description
23:22	TEMP_AVG_ILLUM	R/W	2h	Average external temperature sensor reading. 0: No average   1: 2-sample average   2: 4-sample average   Other values: Not valid
21	EN_TILLUM_READ	R/W	0h	Enable I <sup>2</sup> C read of appropriate external temperature sensor on I <sup>2</sup> C host bus.  0: Disable external temperature sensor read   1: Enable external temperature sensor read
20:14	TSENS_SLAVE2	R/W	4Ah	Slave address of the external temperature sensor in proximity to the TX2 channel
13:7	TSENS_SLAVE1	R/W	49h	Slave address of the external temperature sensor in proximity to the TX1 channel
6:0	TSENS_SLAVE0	R/W	48h	Slave address of the external temperature sensor in proximity to the TX0 channel

#### 7.5.1.1.4 Register 3h (Address = 3h) [reset = 800000h]



### Figure 32. Register 3h

23	22	21	20	19	18	17	16
TEMP_A	VG_MAIN		RESE	RVED		I2C_NUM_TRA	I2C_WRITE_D ATA1
R/W	/ - 2h		R/W	' - 0h		R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
		l:	2C_WRITE_DATA	11			INIT_LOAD_D ONE
			R/W - 0h				R - 0h
7	6	5	4	3	2	1	0
			I2C_REA	AD_DATA			
			R -	· 0h			

### Table 34. Register 03 Field Descriptions

Bit	Field	Туре	Reset	Description
23:22	TEMP_AVG_MAIN	R/W	0h	Average on-chip temperature sensor reading. 0: No average   1: 2-sample average   2: 4-sample average   3: Not valid
21:18	RESERVED	R/W	0h	Always read or write 0h.
17	I2C_NUM_TRAN	R/W	0h	The number of I <sup>2</sup> C host transactions. 0: 1 transaction   1: 2 transactions.
16:9	I2C_WRITE_DATA1	R/W	0h	The external I <sup>2</sup> C slave device register address connected to the OPT3101 I <sup>2</sup> C host bus where the read would start. Normally in a temperature-sensor read this is not required to be programmed.
8	INIT_LOAD_DONE	R	0h	Can be used to check whether initial auto load from EEPROM is successful or not.  0: Auto load from EEPROM is incomplete   1: Auto load from EEPROM is complete
7:0	I2C_READ_DATA	R	0h	The I <sup>2</sup> C host read data.

#### 7.5.1.1.5 Register 4h (Address = 4h) [reset = 17h]

#### Figure 33. Register 4h

23	22	21	20	19	18	17	16					
TILLUM_UNSI GNED		RESERVED		TILLUM								
R/W - 0h	R/W - 0h R - 0h											
15	14 13 12			11	10	9	8					
			TILL	LUM								
			R -	0h								
7	6 5 4 3 2 1				1	0						
	RESERVED											
			R/W	- 17h		R/W - 17h						

#### Table 35. Register 04 Field Descriptions

Bit	Field	Туре	Reset	Description
23	TILLUM_UNSIGNED	R/W	0h	Set this bit to 1 when the temperature given by the external temperature sensor is in unsigned format.
22:20	RESERVED	R/W	0h	Always read or write 0h.
19:8	TILLUM	R	0h	The temperature value of the external temperature sensor.
7:0	RESERVED	R/W	17h	Always read or write 17h.

### 7.5.1.1.6 Register 5h (Address = 5h) [reset = 80000h]



#### Figure 34. Register 5h

23	22	21	20	19	18	17	16		
I2C_NUM_B	YTES_TRAN2		RESERVED						
R/V	V-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h		
15	14	13	12	11	10	9	8		
	RESERVED								
			R/W	/-0h					
7	6	5	4	3	2	1	0		
RESERVED									
			R/W	/-0h					

#### Table 36. Register 05 Field Descriptions

Bit	Field	Type	Reset	Description
23:22	I2C_NUM_BYTES_TRAN2	R/W		Number of bytes used in transaction 2 of the I <sup>2</sup> C host transaction.  0: 1 byte   1: 2 bytes   Other values: Not valid
21:16	RESERVED	R/W	08h	Always read or write 08h.
15:0	RESERVED	R/W	0h	Always read or write 0h.

#### 7.5.1.1.7 Register 7h (Address = 7h) [reset = 0h]

### Figure 35. Register 7h

23	22	21	20	19	18	17	16
	CONFIG_TII	LLUM_MSB		I2C_SEL_RI	EAD_BYTES	I2C_NUM_BY	TES_TRAN1
	R/W	/-0h		R/V	/-0h	R/W	/-0h
15	14	13	12	11	10	9	8
			RESE	RVED			
			R/V	V-0h			
7	6	5	4	3	2	1	0
	I2C_WRITE_DATA2						
	R/W-0h						

### Table 37. Register 07 Field Descriptions

Bit	Field	Туре	Reset	Description
23:20	CONFIG_TILLUM_MSB	R/W	0h	Configure the data read by the device I <sup>2</sup> C host from the external temperature sensor 8: I <sup>2</sup> C host read data[15:4], to support 12-bit external temperature sensor   Other values: Not valid. Along with this register also set the EN_TILLUM_12B regsiter to 1.
19:18	I2C_SEL_READ_BYTES	R/W	0h	Chooses which byte of the I2C_READ register to be read on the I2C_READ_DATA register 0: 7:0   1: 15:8   2: 23:16   3: 31:24
17:16	I2C_NUM_BYTES_TRAN1	R/W	0h	Number of bytes used in the transaction 1 of I <sup>2</sup> C host transaction. 0: 1 byte   1: 2 bytes
15:8	RESERVED	R/W	0h	Always read or write 0h.
7:0	I2C_WRITE_DATA2	R/W	0h	Second byte of I <sup>2</sup> C write transaction. 8-bit register data to be written

### 7.5.1.1.8 Register 8h (Address = 8h) [reset = 0h]

### Figure 36. Register 8h

23	22	21	20	19	18	17	16
FRAME_COUN T0	AMB_OVL_FLA G	MOD_FREQ	FRAME_STAT US	TX_CH	IANNEL	HDR_MODE	PHASE_OVER _FLOW
R-0h	R-0h	R-0h	R-0h	R	-0h	R-0h	R-0h
15	14	13	12	11	10	9	8



			PHASI	E_OUT			
R-0h							
7	6	5	4	3	2	1	0
PHASE_OUT							
			R-	-0h			

### Table 38. Register 08 Field Descriptions

Bit	Field	Туре	Reset	Description
23	FRAME_COUNT0	R	0h	Frame counter LSB bit.
22	AMB_OVL_FLAG	R	0h	Overload flag to indicate ambient saturation 0: No saturation   1: Ambient saturation
21	MOD_FREQ	R	0h	Indicates the frequency used. 0: 10 MHz   1: De-alias frequency (10 MHz × 6 / 7 or 10 MHz × 6 / 5)
20	FRAME_STATUS	R	0h	O: Invalid frame   1: Valid frame. Frame is invalid during the internal crosstalk calibration frame (INT_XTALK_CALIB = 1) or the illumination crosstalk calibration frame (ILLUM_XTALK_CALIB = 1).
19:18	TX_CHANNEL	R	0h	Indicates which Illumination channel used. 0: TX0   1: TX1   2: TX2   3: Not valid
17	HDR_MODE	R	0h	Indicates the illumination driver DAC current used. 0: ILLUM_DAC_L   1: ILLUM_DAC_H
16	PHASE_OVER_FLOW	R	0h	PHASE_OUT overflow bit during frequency correction 0: No overflow   1: overflow
15:0	PHASE_OUT	R	0h	Final calibrated phase.

#### 7.5.1.1.9 Register 9h (Address = 9h) [reset = 0h]

### Figure 37. Register 9h

23	22	21	20	19	18	17	16
	DEALIA	S_BIN		PHASE_OVER _FLOW_F2	SIG_OVL_FLA G	FRAME_	COUNT1
	R-0	Oh		R-0h	R-0h	R-	0h
15	14	13	12	11	10	9	8
			AMP	_OUT			
			R-	-0h			
7	6	5	4	3	2	1	0
AMP_OUT							
	·	·	R	-0h	·		

### Table 39. Register 09 Field Descriptions

Bit	Field	Туре	Reset	Description
23:20	DEALIAS_BIN	R	0h	Distance bin in de-alias mode.  De-aliased distance = DEALIAS_BIN × 2 <sup>16</sup> × FREQ_COUNT_READ_REG / 16384 + PHASE_OVER_FLOW × 2 <sup>16</sup> + PHASE_OUT
19	PHASE_OVER_FLOW_F2	R	0h	Phase overflow of second modulation frequency used for de-alias operation during frequency correction.  0: No overflow   1: overflow
18	SIG_OVL_FLAG	R	0h	Overload flag to indicate signal saturation 0: No saturation   1: Signal saturation
17:16	FRAME_COUNT1	R	0h	Frame counter bits [2:1]
15:0	AMP_OUT	R	0h	Amplitude of the received signal.

### 7.5.1.1.10 Register Ah (Address = Ah) [reset = 0h]



### Figure 38. Register Ah

23	22	21	20	19	18	17	16		
TMAIN									
R-0h									
15	14	13	12	11	10	9	8		
	TM	AIN			AMB_I	AMB_DATA			
	R-	0h			AMB_DATA R-0h				
7	6	5	4	3	2	1	0		
AMB_DATA							COUNT2		
	R-0h								

### **Table 40. Register 0A Field Descriptions**

Bit	Field	Туре	Reset	Description
23:12	TMAIN	R	0h	On-chip temperature sensor output Temperature (°C) = TMAIN / 8 – 256
11:2	AMB_DATA	R	0h	Ambient ADC output. Indicates the ambient light.
1:0	FRAME_COUNT2	R	0h	Frame counter MSB bits [4:3].

### 7.5.1.1.11 Register Bh (Address = Bh) [reset = FC009h]

### Figure 39. Register Bh

23	22	21	20	19	18	17	16	
	AMB_CALIB							
	R/W - 0Fh							
15	14	13	12	11	10	9	8	
AMB_	_CALIB		GPO_	SEL2		0	0	
R/W	/ - 3h		R/W	- 0h		R/W - 0h	R/W - 0h	
7	6	5	4	3	2	1	0	
	DIG_GPO_SEL1				DIG_GP	O_SEL0		
	R/W - 0h				R/W	- 9h		

### Table 41. Register 0B Field Descriptions

Bit	Field	Туре	Reset	Description
23:14	AMB_CALIB	R/W	3Fh	The ambient ADC value at which device is calibrated for phase offset
13:10	DIG_GPO_SEL2	R/W	0h	Mux selection bits for digital signal DIG_GPO_2 which can be brought out on GP3 (SDA_M)
9:8	0	R/W	0h	Always read or write 0h.
7:4	DIG_GPO_SEL1	R/W	0h	Mux selection bits for digital signal DIG_GPO_1 which can be brought out on GP1 or GP2 0: FRAME VD   1: SUB-VD   4: SEQUENCER INTERRUPT 8: COMP_STATUS   9: DATA_RDY   10: FRAME_COUNTER_LSB   Other values: Not valid
3:0	DIG_GPO_SEL0	R/W	9h	Mux selection bits for digital signal DIG_GPO_0 which can be brought out on GP1 or GP2 0: FRAME VD   1: SUB-VD   4: SEQUENCER INTERRUPT 8: COMP_STATUS   9: DATA_RDY   10: FRAME_COUNTER_LSB   Other values: Not valid

# 7.5.1.1.12 Register Ch (Address = Ch) [reset = 0h]



### Figure 40. Register Ch

23	22	21	20	19	18	17	16			
	AMB_PHASE_CORR_PWL_COEFF0									
	R/W - 0h									
15	14	13	12	11	10	9	8			
			AMB_XTALK_Q	PHASE_COEFF						
			R/W	' - 0h						
7	6	5	4	3	2	1	0			
	AMB_XTALK_IPHASE_COEFF									
	R/W - 0h									

### **Table 42. Register 0C Field Descriptions**

Bit	Field	Туре	Reset	Description
23:16	AMB_PHASE_CORR_PWL _COEFF0	R/W	0h	Coefficient 0 for piecewise linear (PWL) phase correction with ambient.
15:8	AMB_XTALK_QPHASE_C OEFF	R/W	0h	Coefficient to correct for the crosstalk (quadrature component) change with ambient.
7:0	AMB_XTALK_IPHASE_CO	R/W	0h	Coefficient to correct for the crosstalk (in-phase component) change with ambient.

### 7.5.1.1.13 Register Dh (Address = Dh) [reset = 6000h]

### Figure 41. Register Dh

23	22	21	20	19	18	17	16			
EN_TILLUM_1 2B		RESERVED								
R/W - 0h			R/W	′ - 0h			R/W - 0h			
15	14	13	12	11	10	9	8			
	AMB_SAT_THR									
			R/W	- 60h						
7	6	5	4	3	2	1	0			
AMB_SAT_TH R		RESERVED								
R/W - 0h		R/W - 0h								

### **Table 43. Register 0D Field Descriptions**

Bit	Field	Туре	Reset	Description
23	EN_TILLUM_12B	R/W	0h	Enables support for an external temperature sensor with more than 8-bit resolution on the I <sup>2</sup> C host bus. Preferred 12-bit temperature sensor: TMP102.  0: 8-bit temperature read   1: 12-bit temperature read
22:17	RESERVED	R/W	0h	Always read or write 0h.
16:7	AMB_SAT_THR	R/W	C0h	Ambient threshold which is used to detect the ambient overload.  AMB_DATA – AMB_CALIB is compared against this threshold value and AMB_OVL_FLAG is set to 1 if it exceeds the threshold.
6:0	RESERVED	R/W	0h	Always read or write 0h.

#### 7.5.1.1.14 Register Fh (Address = Fh) [reset = 144C4Bh]

### Figure 42. Register Fh

23	22	21	20	19	18	17	16
EN_FREQ_CO RR	EN_FLOOP	EN_AUTO_FR EQ_COUNT		SYS_CLK	_DIVIDER		START_FREQ _CALIB
R/W - 0h	R/W - 0h	R/W - 0h		R/W - 0h			
15	14	13	12	11	10	9	8



RESERVED	REF_COUNT_LIMIT								
R/W - 0h		R/W - 4Ch							
7	6	6 5 4 3 2 1 0							
	REF_COUNT_LIMIT								
	R/W - 4Bh								

### Table 44. Register 0F Field Descriptions

Bit	Field	Туре	Reset	Description
23	EN_FREQ_CORR	R/W	0h	Enable frequency correction for the phase output.  0: Frequency correction disabled   1: Frequency correction enabled
22	EN_FLOOP	R/W	0h	Enables the frequency calibration block.  0: Disable frequency calibration block   1: Enable frequency calibration block
21	EN_AUTO_FREQ_COUNT	R/W	0h	Determines the value to be used for frequency correction.  0 – On-chip trimmed value   1 – Measured value from frequency calibration
20:17	SYS_CLK_DIVIDER	R/W	Ah	Programs the system-clock divider for frequency calibration. This register should be adjusted to get it closer to the external reference frequency connected to GP2 pin.  SYS_CLK_DIVIDER = round(log <sub>2</sub> (40 × 10 <sup>6</sup> / f <sub>EXT</sub> ))
16	START_FREQ_CALIB	R/W	0h	Setting this bit to 1 starts the frequency calibration.
15	RESERVED	R/W	0h	Always read or write 0h.
14:0	REF_COUNT_LIMIT	R/W	4C4Bh	This sets the limit for ref-clock count. REF_COUNT_LIMIT = $(40 \times 10^6 / 2^{SYS\_CLK\_DIVIDER}) / f_{EXT}$

#### 7.5.1.1.15 Register 10h (Address = 10h) [reset = 4000h]

### Figure 43. Register 10h

23	22	21	20	19	18	17	16		
AMPLITUDE_MIN_THR[15:8]									
R/W - 0h									
15	14	13	12	11	10	9	8		
EN_CONT_FC ALIB			FREG	Q_COUNT_READ_	_REG				
R/W - 0h				R/W - 40h					
7	6	5	4	3	2	1	0		
	FREQ_COUNT_READ_REG								
	R/W - 0h								

### **Table 45. Register 10 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:16	AMPLITUDE_MIN_THR[15: 8]	R/W	0h	MSB of minimum amplitude threshold below which phase is made FFFFh.
15	EN_CONT_FCALIB	R/W	0h	Enables continuous frequency calibration.  0: Frequency is measured only when START_FREQ_CALIB = 1   1: Frequency is continuously measured.
14:0	FREQ_COUNT_READ_RE	R	4000h	Read register which holds the value of frequency correction when frequency calibration is enabled. This value is used for frequency correction when EN_AUTO_FREQ_COUNT = 1.

### 7.5.1.1.16 Register 11h (Address = 11h) [reset = 0h]

#### Figure 44. Register 11h

23	22	21	20	19	18	17	16
AMPLITUDE_MIN_THR[7:0]							
			R/W	- 0h			
15	14	13	12	11	10	9	8



DIS_OVL_GATI NG			F	REQ_COUNT_RE	:G		
R/W - 0h				R			
7	6	5	4	3	2	1	0
			FREQ_CC	OUNT_REG			
				R			

#### **Table 46. Register 11 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:16	AMPLITUDE_MIN_THR[7:0	R/W	0h	LSB of minimum amplitude threshold below which phase is made FFFFh.
15	DIS_OVL_GATING	R/W	0h	Disable gating of phase output when SIG_OVL_FLAG becomes 1. 0: PHASE_OUT is gated when SIG_OVL_FLAG = 1   1: PHASE_OUT is not gated
14:0	FREQ_COUNT_REG	R		Digital frequency correction trim value. This value will be used for frequency correction when EN_AUTO_FREQ_COUNT = 0.

### 7.5.1.1.17 Register 13h (Address = 13h) [reset = 0h]

### Figure 45. Register 13h

23	22	21	20	19	18	17	16	
		RESERVED			COMPARE_REG1			
		R/W - 0h		R/W - 0h				
15	14	13	12	11	10	9	8	
			COMPA	RE_REG1				
			R/W	/ - 0h				
7	6	5	4	3	2	1	0	
		COMPARE_REG1		MUX_SEL_COMPIN				
		R/W - 0h			R/W - 0h			

### **Table 47. Register 13 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:19	RESERVED	R/W	0h	Always read or write 0h.
18:3	COMPARE_REG1	R/W	0h	Sequencer comparison threshold1 register
2:0	MUX_SEL_COMPIN	R/W	0h	Chooses the value used for comparator input register of sequencer. 0: AMP_OUT   1: DEALIAS_BIN   2: De-alias distance   3: PHASE_OUT   Other values: Not valid.

### 7.5.1.1.18 Register 14h (Address = 14h) [reset = 0h]

### Figure 46. Register 14h

23	22	21	20	19	18	17	16
	RESE	RVED		DIS_INTERRU PT	STATUS_IN_R EG	EN_PROCESS OR_VALUES	EN_SEQUENC ER
	R/W	- 0h		R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
	COMPARE_REG2						
			R/W	' - 0h			
7	6	5	4	3	2	1	0
	COMPARE_REG2						
	R/W - 0h						



#### **Table 48. Register 14 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:20	RESERVED	R/W	R/W 0h Always read or write 0h.	
19	DIS_INTERRUPT	R/W 0h Disables the interrupt that triggers sequencer. 0: Sequencer interrupt enabled   1: Sequencer interrupt		Disables the interrupt that triggers sequencer.  0: Sequencer interrupt enabled   1: Sequencer interrupt disabled
18	STATUS_IN_REG	R/W	0h	This register is used to control the program flow in the sequencer
17	EN_PROCESSOR_VALUE S	R/W	0h	Uses STATUS_OUT values instead of register values. STAUTS_OUT register mapping is described in Table 20
16	EN_SEQUENCER	R/W	0h	Enable the sequencer. 0: Sequencer enabled   1: Sequencer disabled
15:0	COMPARE_REG2	R/W	0h	Sequencer second comparison threshold register

#### 7.5.1.1.19 Register 15h (Address = 15h) [reset = 101063h]

#### Figure 47. Register 15h

23	22	21	20	19	18	17	16
			COMM	AND1			
			R/W -	10h			
15	14	13	12	11	10	9	8
	COMM	IAND1		COMMAND0			
	R/W	- 1h			R/W	- 0h	
7	6	5	4	3	2	1	0
COMMAND0							
	R/W - 63h						

### Table 49. Register 15 Field Descriptions

Bit	Field	Туре	Reset	Description
23:12	COMMAND1	R/W	101h	Sequencer command 1.
11:0	COMMAND0	R/W	63h	Sequencer command 0.

#### 7.5.1.1.20 Register 16h (Address = 16h) [reset = 400100h]

#### Figure 48. Register 16h

23	22	21	20	19	18	17	16	
			COMN	MAND3				
R/W - 40h								
15	14	13	12	11	10	9	8	
	COMN	MAND3		COMMAND2				
	R/W	- 0h			R/W	- 1h		
7	6	5	4	3	2	1	0	
	COMMAND2							
	R/W - 00h							

### Table 50. Register 16 Field Descriptions

Bit	Field	Type	Reset	Description
23:12	COMMAND3	R/W	400h	Sequencer command 3.
11:0	COMMAND2	R/W	100h	Sequencer command 2.

#### 7.5.1.1.21 Register 17h (Address = 17h) [reset = 0h]



# Figure 49. Register 17h

23	22	21	20	19	18	17	16	
COMMAND5								
R/W - 0h								
15	15 14 13 12			11	10	9	8	
	COMM	MAND5		COMMAND4				
	R/W	- 0h		R/W - 0h				
7	6	5	4	3	2	1	0	
COMMAND4								
	R/W - 0h							

#### Table 51. Register 17 Field Descriptions

Bit	Field	Type	Reset	Description
23:12	COMMAND5	R/W	0h	Sequencer command 5.
11:0	COMMAND4	R/W	0h	Sequencer command 4.

#### 7.5.1.1.22 Register 18h (Address = 18h) [reset = 0h]

### Figure 50. Register 18h

23	22	21	20	19	18	17	16		
	COMMAND7								
	R/W - 0h								
15	14	14 13 12			10	9	8		
	COMM	IAND7		COMMAND6					
	R/W	- 0h			R/W				
7	6	5	4	3	2	1	0		
COMMAND6									
R/W - 0h									

### **Table 52. Register 18 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:12	COMMAND7	R/W	0h	Sequencer command 7.
11:0	COMMAND6	R/W	0h	Sequencer command 6.

### 7.5.1.1.23 Register 19h (Address = 19h) [reset = 0h]

#### Figure 51. Register 19h

23	22	21	20	19	18	17	16	
COMMAND9								
R/W - 0h								
15	14	13	12	11	10	9	8	
	COMM	1AND9		COMMAND8				
	R/W	- 0h		R/W - 0h				
7	6	5	4	3	2	1	0	
COMMAND8								
R/W - 0h								

### Table 53. Register 19 Field Descriptions

Bit	Field	Туре	Reset	Description
23:12	COMMAND9	R/W	0h	Sequencer command 9.
11:0	COMMAND8	R/W	0h	Sequencer command 8.



#### 7.5.1.1.24 Register 1Ah (Address = 1Ah) [reset = 0h]

#### Figure 52. Register 1Ah

23	22	21	20	19	18	17	16
COMMAND11							
R/W - 0h							
15	14	13	12	11	10	9	8
	COMM	AND11		COMMAND10			
	R/W	- 0h		R/W - 0h			
7	7 6 5 4			3	2	1	0
COMMAND10							
R/W - 0h							

#### **Table 54. Register 1A Field Descriptions**

Bit	Field	Type	Reset	Description
23:12	COMMAND11	R/W	0h	Sequencer command 11.
11:0	COMMAND10	R/W	0h	Sequencer command 10.

# 7.5.1.1.25 Register 1Bh (Address = 1Bh) [reset = 0h]

#### Figure 53. Register 1Bh

23	22	21	21 20		18	17	16
COMMAND13							
R/W - 0h							
15	14	13	12	11	10	9	8
	COMM	AND13		COMMAND12			
	R/W	- 0h		R/W - 0h			
7	7 6 5 4			3	2	1	0
COMMAND12							
R/W - 0h							

### Table 55. Register 1B Field Descriptions

Bit	Field	Туре	Reset	Description
23:12	COMMAND13	R/W	0h	Sequencer command 13.
11:0	COMMAND12	R/W	0h	Sequencer command 12.

#### 7.5.1.1.26 Register 1Ch (Address = 1Ch) [reset = 0h]

### Figure 54. Register 1Ch

23	22	21	20	19	18	17	16	
COMMAND15								
R/W - 0h								
15	15 14 13 12			11	10	9	8	
	COMM	AND15		COMMAND14				
	R/W	- 0h		R/W - 0h				
7	7 6 5 4			3	2	1	0	
COMMAND14								
	R/W - 0h							



### Table 56. Register 1C Field Descriptions

Bit	Field	Type	Reset	Description
23:12	COMMAND15	R/W	0h	Sequencer command 15.
11:0	COMMAND14	R/W	0h	Sequencer command 14.

### 7.5.1.1.27 Register 1Dh (Address = 1Dh) [reset = 0h]

#### Figure 55. Register 1Dh

23	22	21	20	19	18	17	16			
COMMAND17										
R/W - 0h										
15	14	13	12	11	10	9	8			
	COMM	AND17		COMMAND16						
	R/W	- 0h		R/W - 0h						
7	6	5	4	3	2	1	0			
			COMMA	AND16						
R/W - 0h										

#### Table 57. Register 1D Field Descriptions

Bit	Field	Туре	Reset	Description
23:12	COMMAND17	R/W	0h	Sequencer command 17.
11:0	COMMAND16	R/W	0h	Sequencer command 16.

### 7.5.1.1.28 Register 1Eh (Address = 1Eh) [reset = 0h]

#### Figure 56. Register 1Eh

23	22	21	20	19	18	17	16			
COMMAND19										
R/W - 0h										
15	14	13	12	11	10	9	8			
	COMM	AND19		COMMAND18						
	R/W	- 0h		R/W - 0h						
7	6	5	4	3	2	1	0			
	COMMAND18									
R/W - 0h										

### Table 58. Register 1E Field Descriptions

Bit	Field	Туре	Reset	Description
23:12	COMMAND19	R/W	0h	Sequencer command 19.
11:0	COMMAND18	R/W	0h	Sequencer command 18.

# 7.5.1.1.29 Register 26h (Address = 26h) [reset = 4000Fh]

# Figure 57. Register 26h

23	22	21	20	19	18	17	16		
POWERUP_DELAY									
R/W - 04h									
15	14	13	12	11	10	9	8		
		POWERU	IP_DELAY			0	0		
	R/W - 00h								
7	6	5	4	3	2	1	0		



0	0	0	0	1	1	1	1
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 1h	R/W - 1h	R/W - 1h	R/W - 1h

#### **Table 59. Register 26 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:10	POWERUP_DELAY	R/W	100h	Register to program the delay from the monoshot trigger to start of frame (FRAME_VD). Delay = $(64 \times POWERUP\_DELAY + 2) \times t_{CLK}$ , $t_{CLK} = 25$ ns.
9:0	RESERVED	R/W	Fh	Always read or write Fh.

#### 7.5.1.1.30 Register 27h (Address = 27h) [reset = 26AC18h]

### Figure 58. Register 27h

23	22	21	20	19	18	17	16			
MONOSHOT_FZ_CLKCNT										
R/W - 26h										
15	14	13	12	11	10	9	8			
MONOSHOT_FZ_CLKCNT										
			R/W -	ACh						
7	6	5	4	3	2	1	0			
MONOSHOT	_NUMFRAME	MONOSHO <sup>-</sup>	T_NUMFRAME			MONOSHOT_MODE				
R/W - 6h						R/W	' - 0h			

### Table 60. Register 27 Field Descriptions

Bit	Field	Туре	Reset	Description
23:8	MONOSHOT_FZ_CLKCNT	R/W	26ACh	The CLK count at which a monoshot operation freezes.
7:2	MONOSHOT_NUMFRAME	R/W	6h	The number of samples to be captured on every monoshot trigger event.
1:0	MONOSHOT_MODE	R/W	0h	Select monoshot mode. 0: Continuous mode   3: Monoshot mode   Other values: Not valid

#### 7.5.1.1.31 Register 29h (Address = 29h) [reset = 3F0FC3h]

### Figure 59. Register 29h

23	22	21	20	19	18	17	16	
	ILLUM_DAC	_L_TX2[4:1]		ILLUM_DAC_H_TX1				
	R/W	- 3h		R/W - Fh				
15	14	13	12	11	10	9	8	
ILLUM_DAC_H _TX1	ILLUM_DAC_L_TX1 IL						AC_H_TX0	
R/W - 0h			R/W - 03h			R/W	- 3h	
7	6	5	4	3	2	1	0	
IL	LUM_DAC_H_TX	(0		ILLUM_DAC_L_TX0				
	R/W - 6h			R/W - 03h				

#### **Table 61. Register 29 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:20	ILLUM_DAC_L_TX2[4:1]	R/W	3h	Illumination driver current DAC register, ILLUM_DAC_L[4:1] of TX2 channel
19:15	ILLUM_DAC_H_TX1	R/W	1Eh	Illumination driver current DAC register, ILLUM_DAC_H of TX1 channel
14:10	ILLUM_DAC_L_TX1	R/W	3h	Illumination driver current DAC register, ILLUM_DAC_L of TX1 channel
9:5	ILLUM_DAC_H_TX0	R/W	1Eh	Illumination driver current DAC register, ILLUM_DAC_H of TX0 channel
4:0	ILLUM_DAC_L_TX0	R/W	3h	Illumination driver current DAC register, ILLUM_DAC_L of TX0 channel



#### 7.5.1.1.32 Register 2Ah (Address = 2Ah) [reset = 784920h]

### Figure 60. Register 2Ah

23	22	21	20	19	18	17	16		
ILLUM_DAC_L _TX2[0]		I		RESERVED	SEL_HDR_MO DE				
R/W - 0h		R/W - 1Eh R/W - 0h R/W							
15	14	13	12	11	10	9	8		
EN_ADAPTIVE _HDR		TX_SEQ_REG							
R/W - 0h				R/W - 49h					
7	6	5	4	3	2	1	0		
	TX_CH	EN_TX_SWITC H							
	·	R/W - 04h	R/W	′ - 0h	R/W - 0h				

### **Table 62. Register 2A Field Descriptions**

Bit	Field	Туре	Reset	Description
23	ILLUM_DAC_L_TX2[0]	R/W	1h	Illumination driver current DAC register, ILLUM_DAC_L[0] of TX2 channel
22:18	ILLUM_DAC_H_TX2	R/W	1Eh	Illumination driver current DAC register, ILLUM_DAC_H of TX2 channel
17	RESERVED	R/W	0h	Always read or write 0h.
16	SEL_HDR_MODE	R/W	0h	Selects which current to use when EN_ADAPTIVE_HDR = 0 0: ILLUM_DAC_L   1: ILLUM_DAC_H
15	EN_ADAPTIVE_HDR	R/W	0h	Enable adaptive HDR to switch between two illumination driver currents (ILLUM_DAC_L and ILLUM_DAC_H) depending on the amplitude of the received signal.  0: Disable adaptive HDR   1: Enable adaptive HDR
14:3	TX_SEQ_REG	R/W	924h	Switching sequence of illumination channels. Up to a sequence of 6 channel configurations.  For example, for register value: 2-1-0-2-1-0, the illumination channel sequence is 0-1-2-0-1-2
2:1	SEL_TX_CH	R/W	0h	Selects the illumination channel when channel switching is disabled. 0: TX0   1: TX1   2: TX2   3: Not valid
0	EN_TX_SWITCH	R/W	0h	Enable switching of illumination channels. 0: TX channel switching is disabled and the TX channel is determined by SEL_TX_CH 1: TX channel switching is enabled. The TX channel switching is programmed with TX_SEQ_REG.

#### 7.5.1.1.33 Register 2Bh (Address = 2Bh) [reset = 6000h]

### Figure 61. Register 2Bh

23	22	21	20	19	18	17	16	
RESE	RVED	ILI	LUM_SCALE_H_T	X0	ILI	LUM_SCALE_L_T	X0	
R/W	' - 0h		R/W - 0h			R/W - 0h		
15	14	13	12	11	10	9	8	
			HDR_TH	IR_HIGH				
			R/W	- 60h				
7	6	5	5 4 3 2 1 0					
	HDR_THR_HIGH							
	R/W - 00h							



### Table 63. Register 2B Field Descriptions

Bit	Field	Туре	Reset	Description
23:22	RESERVED	R/W	0h Always read or write 0h.	
21:19	ILLUM_SCALE_H_TX0	R/W	0h	Illumination driver current scale register of TX0 channel with DAC_H current. 0: 5.6 mA   1: 4.2mA   2: 2.8 mA   3: 1.4 mA   Other values: Not valid
18:16	ILLUM_SCALE_L_TX0	R/W	0h	Illumination driver current scale register of TX0 channel with DAC_L current. 0: 5.6 mA   1: 4.2mA   2: 2.8 mA   3: 1.4 mA   Other values: Not valid
15:0	HDR_THR_HIGH	R/W	6000h	High threshold for the HDR switching. Amplitude is compared against this threshold when the illumination driver current is high (ILLUM_DAC_H) and it switches to ILLUM_DAC_L if the amplitude exceeds this threshold value.

#### 7.5.1.1.34 Register 2Ch (Address = 2Ch) [reset = 800h]

### Figure 62. Register 2Ch

23	22	21	20	19	18	17	16		
RESE	RVED	IL	LUM_SCALE_H_T	TX1	ILLUM_SCALE_L_TX1				
R/W	' - 0h		R/W - 0h			R/W - 0h			
15	14	13	12	11	10	9	8		
			HDR_TH	HR_LOW					
			R/W	- 08h					
7	6	5	5 4 3 2 1 0						
	HDR_THR_LOW								
	R/W - 0h								

### Table 64. Register 2C Field Descriptions

Bit	Field	Туре	Reset	Description
23:22	RESERVED	R/W	0h	Always read or write 0h.
21:19	ILLUM_SCALE_H_TX0	R/W	0h	Illumination driver current scale register of TX1 channel with DAC_H current.  0: 5.6 mA   1: 4.2 mA   2: 2.8 mA   3: 1.4 mA   Other values: Not valid
18:16	ILLUM_SCALE_L_TX0	R/W	0h	Illumination driver current scale register of TX1 channel with DAC_L current. 0: 5.6 mA   1: 4.2 mA   2: 2.8 mA   3: 1.4 mA   Other values: Not valid
15:0	HDR_THR_LOW	R/W	800h	Low threshold for the HDR switching. Amplitude is compared against this threshold when the Illumination driver current is low (ILLUM_DAC_L) and it switches to ILLUM_DAC_H if the amplitude is lower than this threshold value.

#### 7.5.1.1.35 Register 2Dh (Address = 2Dh) [reset = 0h]

### Figure 63. Register 2Dh

23	22	21	20	19	18	17	16	
			TEMP_COEFF_M	AIN_HDR0_TX1				
			R/W	- 0h				
15	14	13	12	11	10	9	8	
	TEMP_COEFF_M	IAIN_HDR0_TX	1		TEMP_COEFF_M	AIN_HDR1_TX0		
	R/W	- 0h			R/W	- 0h		
7	6	5	4	3	2	1	0	
	TEMP_COEFF_MAIN_HDR1_TX0							
	R/W - 0h							



### Table 65. Register 2D Field Descriptions

Bit	Field	Туре	Reset	Description
23:12	TEMP_COEFF_MAIN_HD R0_TX1	R/W	0h	Phase temperature coefficient for sensor temperature for TX1 illumination channel with current of ILLUM_DAC_L_TX1
11:0	TEMP_COEFF_MAIN_HD R1_TX0	R/W	0h	Phase temperature coefficient for sensor temperature for TX0 illumination channel with current of ILLUM_DAC_H_TX0

#### 7.5.1.1.36 Register 2Eh (Address = 2Eh) [reset = 8001A0h]

### Figure 64. Register 2Eh

23	22	21	20	19	18	17	16
	XTALK_FILT_	TIME_CONST		ILLUM	1_XTALK_REG_SC	CALE	INT_XTALK_R EG_SCALE
	R/W	- 8h			R/W - 0h		R/W - 0h
15	14	13	12	11	10	9	8
INT_XTALK_	REG_SCALE	0	ILLUM_XTALK _CALIB	IQ	_READ_DATA_SE	L	USE_XTALK_R EG_ILLUM
R/W	- 0h	R/W - 0h	R/W - 0h		R/W - 0h		R/W - 1h
7	6	5	4	3	2	1	0
USE_XTALK_F ILT_ILLUM	USE_XTALK_R EG_INT	USE_XTALK_F ILT_INT	INT_XTALK_C ALIB	DIS_AUTO_SC ALE	FO	RCE_SCALE_\	/AL
R/W - 1h	R/W - 0h	R/W - 1h	R/W - 0h	R/W - 0h	·	R/W - 0h	·

# Table 66. Register 2E Field Descriptions

Bit	Field	Туре	Reset	Description
23:20	XTALK_FILT_TIME_CONS	R/W	8h	Time constant for crosstalk filtering. Time constant $\tau = 2^{\text{XTALK\_FILT\_TIME\_CONST}}$ frames. At least $5\tau$ should be allowed for settling the crosstalk measurement.
19:17	ILLUM_XTALK_REG_SCA LE	R/W	0h	Scale factor for illumination crosstalk register (IPHASE_XTALK_REG_HDR <i>&gt;_TX<j>, QPHASE_XTALK_REG_HDR<i>&gt;_TX<j>, i = 0, 1, j = 0, 1, 2). Scale = 2<sup>ILLUM_XTALK_REG_SCALE</sup></j></i></j></i>
16:14	INT_XTALK_REG_SCALE	R/W	0h	Scale factor for internal crosstalk register (IPHASE_XTALK_INT_REG, QPHASE_XTALK_INT_REG). Scale = 2 <sup>INT_XTALK_REG_SCALE</sup>
13	0	R/W	0h	Always read or write 0.
12	ILLUM_XTALK_CALIB	R/W	0h	The device initializes the illumination crosstalk measurement upon setting this bit. This measurement should be done with the photodiode masked such that no modulated light is received.  Use the following sequence:  ILLUM_XTALK_CALIB = 1  Delay (at least 5 × 2 <sup>XTALK_FILT_TIME_CONST</sup> frames)  ILLUM_XTALK_CALIB = 0
11:9	IQ_READ_DATA_SEL	R/W	0h	Mux selection for IPHASE_XTALK, QPHASE_XTALK registers 0: Internal crosstalk   1: Illumination crosstalk   2: Raw I, Q   3: 16-bit frame counter   Other values: Not valid
8	USE_XTALK_REG_ILLUM	R/W	1h	Select register value or internally calibrated value for illumination crosstalk 0: Calibration value   1: Register value
7	USE_XTALK_FILT_ILLUM	R/W	1h	Select filter or direct sampling for Illumination crosstalk measurement.  0: Direct sampling   1: Filter
6	USE_XTALK_REG_INT	R/W	0h	Select register value or internally calibrated value for internal crosstalk 0: Calibration value   1: Register value
5	USE_XTALK_FILT_INT	R/W	1h	Select filter or direct sampling for internal crosstalk measurement.  0: Direct sampling   1: Filter



#### Table 66. Register 2E Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
4	INT_XTALK_CALIB	R/W	0h	The device initializes the internal electrical crosstalk measurement upon setting this bit.  Use following sequence: INT_XTALK_CALIB = 1 Delay (at least 5 × 2 <sup>XTALK_FILT_TIME_CONST</sup> frames) INT_XTALK_CALIB = 0
3	DIS_AUTO_SCALE	R/W	0h	Disable digital auto scale in the signal path.  0: Auto scale enabled   1: Auto scale disabled.
2:0	FORCE_SCALE_VAL	R/W	0h	Digital scaling uses this register scale value if DIS_AUTO_SCALE = 1. This scale value is also used during any crosstalk calibration even if DIS_AUTO_SCALE = 0. Scale = 2 <sup>(6 - FORCE_SCALE_VAL)</sup>

#### 7.5.1.1.37 Register 2Fh (Address = 2Fh) [reset = 0h]

#### Figure 65. Register 2Fh

23	22	21	20	19	18	17	16	
		TI	EMP_COEFF_MA	IN_HDR1_TX1[11:	:4]			
			R/W	' - 0h				
15	14	13	12	11	10	9	8	
			IPHASE_XTALK_	REG_HDR0_TX0				
			R/W	' - 0h				
7	6	5	4	3	2	1	0	
	IPHASE_XTALK_REG_HDR0_TX0							
	R/W - 0h							

### Table 67. Register 2F Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	TEMP_COEFF_MAIN_HD R1_TX1[11:4]	R/W	0h	MSB of phase temperature coefficient for sensor temperature for TX1 illumination channel with current of ILLUM_DAC_H_TX1
15:0	IPHASE_XTALK_REG_HD R0_TX0	R/W	0h	Register for illumination crosstalk in-phase component for TX0 channel with ILLUM_DAC_L_TX0 current

### 7.5.1.1.38 Register 30h (Address = 30h) [reset = 0h]

### Figure 66. Register 30h

23	22	21	20	19	18	17	16		
	TEMP_COEFF_MA	IN_HDR1_TX1[3	3:0]		RESEF	RVED			
	R/W	- 0h		R/W - 0h					
15	14	13	12	11	10	9	8		
			QPHASE_XTALK_	REG_HDR0_TX0	)				
			R/W	- 0h					
7	6	5	4	3	2	1	0		
			QPHASE_XTALK_	REG_HDR0_TX	)				
	R/W - 0h								

### Table 68. Register 30 Field Descriptions

Bit	Field	Туре	Reset	Description
23:20	TEMP_COEFF_MAIN_HD R1_TX1[3:0]	R/W	0h	LSB of phase temperature coefficient for sensor temperature for TX1 illumination channel with current of ILLUM_DAC_H_TX1
19:16	RESERVED	R/W	0h	Always read or write 0h.



#### Table 68. Register 30 Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
15:0	QPHASE_XTALK_REG_H DR0_TX0	R/W	0h	Quadrature component of the crosstalk for ILLUM_DAC_L of TX0

#### 7.5.1.1.39 Register 31h (Address = 31h) [reset = 0h]

#### Figure 67. Register 31h

23	22	21	20	19	18	17	16				
	TEMP_COEFF_MAIN_HDR0_TX2[11:4]										
	R/W - 0h										
15	14	13	12	11	10	9	8				
			IPHASE_XTALK_	_REG_HDR1_TX0							
			R/W	/ - 0h							
7	6	5	4	3	2	1	0				
	IPHASE_XTALK_REG_HDR1_TX0										
	R/W - 0h										

### Table 69. Register 31 Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	TEMP_COEFF_MAIN_HD R0_TX2[11:4]	R/W	0h	MSB of phase temperature coefficient for sensor temperature for TX2 illumination channel with current of ILLUM_DAC_L_TX2
15:0	IPHASE_XTALK_REG_HD R1_TX0	R/W	0h	In-phase component of the crosstalk for ILLUM_DAC_H of TX0

#### 7.5.1.1.40 Register 32h (Address = 32h) [reset = 0h]

#### Figure 68. Register 32h

23	22	21	20	19	18	17	16				
٦	TEMP_COEFF_MAI	IN_HDR0_TX2[3	:0]		RESEF	RVED					
	R/W	- 0h		R/W - 0h							
15	14	13	12	11	10	9	8				
			QPHASE_XTALK	_REG_HDR1_TX0	)						
			R/W	- 0h							
7	6	5	4	3	2	1	0				
	QPHASE_XTALK_REG_HDR1_TX0										
		R/W - 0h									

### Table 70. Register 32 Field Descriptions

Bit	Field	Туре	Reset	Description
23:20	TEMP_COEFF_MAIN_HD R0_TX2[3:0]	R/W	0h	LSB of phase temperature coefficient for sensor temperature for TX2 illumination channel with current of ILLUM_DAC_L_TX2
19:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	QPHASE_XTALK_REG_H DR1_TX0	R/W	0h	Register for illumination crosstalk quad phase component for TX0 channel with ILLUM_DAC_H_TX0 current

# 7.5.1.1.41 Register 33h (Address = 33h) [reset = 0h]



### Figure 69. Register 33h

23	22	21	20	19	18	17	16				
	TEMP_COEFF_MAIN_HDR1_TX2[11:4]										
	R/W - 0h										
15	14	13	12	11	10	9	8				
			IPHASE_XTALK	_REG_HDR0_TX1							
			R/W	/ - 0h							
7	6	5	4	3	2	1	0				
IPHASE_XTALK_REG_HDR0_TX1											
	R/W - 0h										

### Table 71. Register 33 Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	TEMP_COEFF_MAIN_HD R1_TX2[11:4]	R/W	0h	MSB of phase temperature coefficient for sensor temperature for TX2 illumination channel with current of ILLUM_DAC_H_TX2
15:0	IPHASE_XTALK_REG_HD R0_TX1	R/W	0h	Register for illumination crosstalk in-phase component for TX1 channel with ILLUM_DAC_L_TX1 current

#### 7.5.1.1.42 Register 34h (Address = 34h) [reset = 0h]

#### Figure 70. Register 34h

23	22	21	20	19	18	17	16								
	TEMP_COEFF_MAI	N_HDR1_TX2[3	:0]	RESERVED											
	R/W	- 0h		R/W - 0h											
15	14	13	12	11	10	9	8								
			QPHASE_XTALK_	REG_HDR0_TX	1										
			R/W	- 0h											
7	6	5	4	3	2	1	0								
	QPHASE_XTALK_REG_HDR0_TX1														
			R/W	- 0h		R/W - 0h									

### **Table 72. Register 34 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:20	TEMP_COEFF_MAIN_HD R1_TX2[3:0]	R/W	0h	LSB of phase temperature coefficient for sensor temperature for TX2 illumination channel with current of ILLUM_DAC_H_TX2
19:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	QPHASE_XTALK_REG_H DR0_TX1	R/W	0h	Register for illumination crosstalk in quadrature-phase component for TX1 channel with ILLUM_DAC_L_TX1 current

#### 7.5.1.1.43 Register 35h (Address = 35h) [reset = 0h]

### Figure 71. Register 35h

23	22	21	20	19	18	17	16				
	RESERVED										
	R/W - 0h										
15	14	13	12	11	10	9	8				
			IPHASE_XTALK	_REG_HDR1_TX1							
			R/M	/ - 0h							
7	6	5	4	3	2	1	0				
	IPHASE_XTALK_REG_HDR1_TX1										
			R/W	/ - 0h							



### Table 73. Register 35 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	IPHASE_XTALK_REG_HD R1_TX1	R/W	0h	Register for illumination crosstalk in-phase component for TX1 channel with ILLUM_DAC_H_TX1 current

#### 7.5.1.1.44 Register 36h (Address = 36h) [reset = 0h]

#### Figure 72. Register 36h

23	22	21	20	19	18	17	16					
	TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR0_TX0											
	R/W - 0h											
15	14	13	12	11	10	9	8					
	QPHASE_XTALK_REG_HDR1_TX1											
			R/W	′ - 0h								
7	6	5	4	3	2	1	0					
	QPHASE_XTALK_REG_HDR1_TX1											
	R/W - 0h											

#### **Table 74. Register 36 Field Descriptions**

Bit	Field Type Reset		Reset	Description
23:16	TEMP_COEFF_ILLUM_XT ALK_IPHASE_HDR0_TX0	R/W	0h	Temperature coefficient of crosstalk in-phase component with TILLUM for TX0 channel with ILLUM_DAC_L_TX0 current.
15:0	QPHASE_XTALK_REG_H DR1_TX1	R/W	0h	Register for illumination crosstalk quadrature-phase component for TX1 channel with ILLUM_DAC_H_TX1 current

#### 7.5.1.1.45 Register 37h (Address = 37h) [reset = 0h]

### Figure 73. Register 37h

23	22	21	20	19	18	17	16				
	TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR0_TX0										
R/W - 0h											
15	15 14 13 12 11 10 9 8										
	IPHASE_XTALK_REG_HDR0_TX2										
			R/W	′ - 0h							
7	7 6 5 4 3 2 1 0										
	IPHASE_XTALK_REG_HDR0_TX2										
	R/W - 0h										

#### **Table 75. Register 37 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:16	TEMP_COEFF_ILLUM_XT ALK_QPHASE_HDR0_TX0	R/W	0h	Temperature coefficient of crosstalk quadrature-phase component with TILLUM for TX0 channel with ILLUM_DAC_L_TX0 current.
15:0	IPHASE_XTALK_REG_HD R0_TX2	R/W	0h	Register for illumination crosstalk in-phase component for TX2 channel with ILLUM_DAC_L_TX2 current

# 7.5.1.1.46 Register 38h (Address = 38h) [reset = 0h]



### Figure 74. Register 38h

23	22	21	20	19	18	17	16				
TEMP_COEFF_XTALK_IPHASE_HDR0_TX0											
R/W - 0h											
15	15 14 13 12 11 10 9 8										
	QPHASE_XTALK_REG_HDR0_TX2										
			R/W	/ - 0h							
7	7 6 5 4 3 2 1 0										
QPHASE_XTALK_REG_HDR0_TX2											
	R/W - 0h										

### **Table 76. Register 38 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:16	TEMP_COEFF_XTALK_IP HASE_HDR0_TX0	R/W	0h	Temperature coefficient of crosstalk in-phase component with TMAIN for TX0 channel with ILLUM_DAC_L_TX0 current
15:0	QPHASE_XTALK_REG_H DR0_TX2	R/W	0h	Register for illumination crosstalk quadrature-phase component for TX2 channel with ILLUM_DAC_L_TX2 current

#### 7.5.1.1.47 Register 39h (Address = 39h) [reset = 0h]

#### Figure 75. Register 39h

23	22	21	20	19	18	17	16					
	TEMP_COEFF_XTALK_QPHASE_HDR0_TX0											
	R/W - 0h											
15	14	13	12	11	10	9	8					
	IPHASE_XTALK_REG_HDR1_TX2											
			R/W	- 0h								
7	7 6 5 4 3 2 1 0											
	IPHASE_XTALK_REG_HDR1_TX2											
			R/W - 0h									

### **Table 77. Register 39 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:16	TEMP_COEFF_XTALK_QP HASE_HDR0_TX0	R/W	0h	Temperature coefficient of crosstalk quadrature-phase component with TMAIN for TX0 channel with ILLUM_DAC_L_TX0 current
15:0	IPHASE_XTALK_REG_HD R1_TX2	R/W	0h	Register for illumination crosstalk in-phase component for TX2 channel with ILLUM_DAC_H_TX2 current

### 7.5.1.1.48 Register 3Ah (Address = 3Ah) [reset = 0h]

# Figure 76. Register 3Ah

23	22	21	20	19	18	17	16			
RESERVED	SCALI	E_AMB_COEFF_	XTALK	SCALE	EN_TEMP_XT ALK_CORR					
R/W - 0h		R/W - 4h			R/W - 0h					
15	14	13	12	11	10	9	8			
			QPHASE_XTALK_	_REG_HDR1_TX2	2					
			R/W	- 0h						
7	7 6 5 4 3 2 1									
	QPHASE_XTALK_REG_HDR1_TX2									
	R/W - 0h									



### Table 78. Register 3A Field Descriptions

Bit	Field	Туре	Reset	Description		
23	RESERVED	R/W	0h	Always read or write 0h.		
22:20	SCALE_AMB_COEFF_XTA	R/W	Scaling factor for ambient coefficient of crosstalk (AMB_XTALK_IPHASE_COEFF, AMB_XTALK_QPHASE_COEFF)			
19:17	SCALE_TEMP_COEFF_XT ALK	R/W	5h	Scaling factor for temperature coefficient of crosstalk (TEMP_COEFF_XTALK_IPHASE_HDR <i>&gt;_TX<j>, TEMP_COEFF_XTALK_QPHASE_HDR<i>&gt;_TX<j>; i = 0, 1; j = 0, 1, 2).</j></i></j></i>		
16	EN_TEMP_XTALK_CORR	R/W	0h	Enable crosstalk correction with temperature.		
15:0	15:0 QPHASE_XTALK_REG_H R/W 0h		0h	Register for illumination crosstalk quadrature-phase component for TX2 channel with ILLUM_DAC_H_TX2 current		

#### 7.5.1.1.49 Register 3Bh (Address = 3Bh) [reset = 0h]

#### Figure 77. Register 3Bh

23	22	21	20	19	18	17	16				
	IPHASE_XTALK										
	R - 0h										
15	14	13	12	11	10	9	8				
	IPHASE_XTALK										
			R -	0h							
7	6	5	4	3	2	1	0				
	IPHASE_XTALK										
	R - 0h										

# Table 79. Register 3B Field Descriptions

Bit	Field	Туре	Reset	Description
23:0	IPHASE_XTALK	R		Read-only register. In-phase component. Different values can be selected to be read out with IQ_READ_DATA_SEL.

#### 7.5.1.1.50 Register 3Ch (Address = 3Ch) [reset = 0h]

#### Figure 78. Register 3Ch

23	22	21	20	19	18	17	16	
QPHASE_XTALK								
	R - 0h							
15 14 13 12 11 10 9 8					8			
	QPHASE_XTALK							
			R -	- 0h				
7	6	5	4	3	2	1	0	
	QPHASE_XTALK							
	R - 0h							

### Table 80. Register 3C Field Descriptions

Bit	Field	Туре	Reset	Description
23:0	QPHASE_XTALK	R		Read-only register. Quadrature-phase component. Different values can be selected to be read out with IQ_READ_DATA_SEL.

#### 7.5.1.1.51 Register 3Dh (Address = 3Dh) [reset = 0h]



# Figure 79. Register 3Dh

23	22	21	20	19	18	17	16		
RESERVED									
	R - 0h								
15	14	13	12	11	10	9	8		
			IPHASE_XTA	ALK_INT_REG					
			R/W	/ - 0h					
7	6	5	4	3	2	1	0		
	IPHASE_XTALK_INT_REG								
	R/W - 0h								

#### **Table 81. Register 3D Field Descriptions**

Bit	Field	Туре	Reset	Description
23:16	RESERVED	R	0h	
15:0	IPHASE_XTALK_INT_REG	R/W	0h	Register for in-phase component of internal crosstalk

#### 7.5.1.1.52 Register 3Eh (Address = 3Eh) [reset = 0h]

#### Figure 80. Register 3Eh

23	22	21	20	19	18	17	16		
	RESERVED								
	R - 0h								
15	14	13	12	11	10	9	8		
			QPHASE_XT/	ALK_INT_REG					
			R/W	' - 0h					
7	6	5	4	3	2	1	0		
	QPHASE_XTALK_INT_REG								
	R/W - 0h								

### **Table 82. Register 3E Field Descriptions**

Bit	Field	Туре	Reset	Description
23:16	RESERVED	R	0h	
15:0	QPHASE_XTALK_INT_RE G	R/W	0h	Register for quadrature-phase component of internal crosstalk

#### 7.5.1.1.53 Register 3Fh (Address = 3Fh) [reset = 0h]

### Figure 81. Register 3Fh

23	22	21	20	19	18	17	16	
TILLUM_CALIB_HDR0_TX2								
R/W -			- 0h					
15	14	13	12	11	10	9	8	
	TILLUM_CALI	B_HDR0_TX2		TMAIN_CALIB_HDR0_TX2				
	R/W	- 0h		R/W - 0h				
7	6	5	4	3	2	1	0	
TMAIN_CALIB_HDR0_TX2								
	R/W - 0h							

### Table 83. Register 3F Field Descriptions

Bit	Field	Туре	Reset	Description
23:12	TILLUM_CALIB_HDR0_TX 2	R/W	0h	Calibration temperature of external temperature sensor (TILLUM) for TX2 illumination channel with current of ILLUM_DAC_L_TX2



### Table 83. Register 3F Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
11:0	TMAIN_CALIB_HDR0_TX2	R/W	0h	Calibration temperature of on-chip temperature sensor (TMAIN) for TX2 illumination channel with current of ILLUM_DAC_L_TX2

#### 7.5.1.1.54 Register 40h (Address = 40h) [reset = 2021E0h]

### Figure 82. Register 40h

23	22	21	20	19	18	17	16
RESERVED	EN_MULTI_FR EQ_PHASE	NCR_CONFIG	BETA0_DEALIAS_S			LE	
R/W - 0h	R/W - 0h	R/W - 0h R/W - 1h R/W - 0h					
15	14 13 12 11 10 9					8	
BETA0_DEALI AS_SCALE							RESERVED
R/W - 0h			R/W	- 10h			R/W - 1h
7	6	5	4	3	2	1	0
	RESERVED						EN_DEALIAS_ MEAS
	R/W - 70h						R/W - 0h

### Table 84. Register 40 Field Descriptions

Bit	Field	Туре	Reset	Description
23	RESERVED	R/W	0h	Always read or write 0h.
22	EN_MULTI_FREQ_PHASE	R/W	0h	With this bit set to 1, along with EN_DEALIAS_MEAS = 1, the PHASE_OUT register gives the phase measurement with two frequencies. The frequency of the phase is indicated in MOD_FREQ status bit.  0: 10-MHz modulation   1: 10-MHz and 10 × (6 / 7)-MHz or 10 × (6 / 5)-MHz modulation.
21	NCR_CONFIG	R/W	1h	Select second frequency for de-alias operation. 0: 10 × (6 / 7) MHz   1: 10 × (6 / 5) MHz.
20:15	BETA0_DEALIAS_SCALE	R/W	0h	Internal crosstalk scaling for de-alias frequency. β = BETA0_DEALIAS_SCALE / 16.
14:9	ALPHA0_DEALIAS_SCALE	R/W	10h	Internal crosstalk scaling for de-alias frequency. $\alpha$ = ALPHA0_DEALIAS_SCALE / 16.
8:1	RESERVED	R/W	F0h	Always read or write F0h.
0	EN_DEALIAS_MEAS	R/W	0h	Enables de-alias measurement. 0: Default operating mode   1: De-alias operating mode

#### 7.5.1.1.55 Register 41h (Address = 41h) [reset = 10h]

### Figure 83. Register 41h

23	22	21	20	19	18	17	16		
			TMAIN_CALIE	B_HDR1_TX1					
			R/W	- 0h					
15	14	13	12	11	10	9	8		
	TMAIN_CALIB	_HDR1_TX1			BETA1_DEALIAS_SCALE				
	R/W -	· 0h		R/W - 0h					
7	6	5	4	3	2	1	0		
BETA1_DEALIAS_SCALE			ALPHA1_DE	ALIAS_SCALE					
R/V	V - 0h	' - 10h							



### Table 85. Register 41 Field Descriptions

Bit	Field	Туре	Reset	Description
23:12	TMAIN_CALIB_HDR1_TX1	R/W	0h	Calibration temperature of on-chip temperature sensor (TMAIN) for TX1 illumination channel with current of ILLUM_DAC_H_TX1
11:6	BETA1_DEALIAS_SCALE	R/W	0h	Illumination crosstalk scaling for de-alias frequency. $\beta$ = BETA1_DEALIAS_SCALE / 16
5:0	ALPHA1_DEALIAS_SCALE	R/W	10h	Illumination crosstalk scaling for de-alias frequency. $\alpha$ = ALPHA1_DEALIAS_SCALE / 16

#### 7.5.1.1.56 Register 42h (Address = 42h) [reset = 0h]

### Figure 84. Register 42h

23	22	21	20	19	18	17	16			
RESERVED										
	R/W - 0h									
15	14	13	12	11	10	9	8			
PHASE_OFFSET_HDR0_TX0										
			R/W	V - 0h						
7	6	5	4	3	2	1	0			
PHASE_OFFSET_HDR0_TX0										
	R/W - 0h									

#### **Table 86. Register 42 Field Descriptions**

Bit	Field	Туре	Reset	Description	
23:16	RESERVED	R/W	0h	Always read or write 0h.	
15:0	PHASE_OFFSET_HDR0_T X0	R/W	0h	Phase offset for TX0 illumination channel with current of ILLUM_DAC_L_TX0	

### 7.5.1.1.57 Register 43h (Address = 43h) [reset = 81h]

#### Figure 85. Register 43h

23	22	21	20	19	18	17	16				
	TILLUM_CALIB_HDR1_TX1										
			R/W	' - 0h							
15	14	13	12	11	10	9	8				
TILLUM_CALIB_HDR1_TX1 0						0	SCALE_PHAS E_TEMP_COE FF				
	R/W -	- 0h		R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h				
7	6	5	4	3	2	1	0				
SCALE_PHASE_TEMP_COEFF RESERVED						EN_TEMP_CO RR	EN_PHASE_C ORR				
RΛ	N - 2h	·	R/W	' - 0h		R/W - 0h	R/W - 1h				

### Table 87. Register 43 Field Descriptions

Bit	Field	Туре	Reset	Description
23:12	TILLUM_CALIB_HDR1_TX 1	R/W	0h	Calibration temperature of external temperature sensor (TILLUM) for TX1 illumination channel with current of ILLUM_DAC_H_TX1.
8:6	SCALE_PHASE_TEMP_C OEFF	R/W	2h	Scaling factor for phase temperature coefficient.
5:2	RESERVED	R/W	0h	Always read or write 0h.
1	EN_TEMP_CORR	R/W	0h	Enables temperature correction for phase.  0: Phase temperature correction disabled   0: Phase temperature correction enabled



#### Table 87. Register 43 Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
0	EN_PHASE_CORR	R/W	1h	Enables phase offset correction.  0: Phase offset correction disabled   0: Phase offset correction enabled

#### 7.5.1.1.58 Register 44h (Address = 44h) [reset = 0h]

#### Figure 86. Register 44h

23	22	21	20	19	18	17	16				
	RESERVED										
	R/W - 0h										
15	14	13	12	11	10	9	8				
PHASE2_OFFSET_HDR0_TX0											
			R/W	/ - 0h							
7	6	5	4	3	2	1	0				
PHASE2_OFFSET_HDR0_TX0											
	R/W - 0h										

#### **Table 88. Register 44 Field Descriptions**

В	it	Field	Туре	Reset	Description	
23:	:16	RESERVED	R/W	0h	Always read or write 0h.	
15	5:0	PHASE2_OFFSET_HDR0_ TX0	R/W	0h	De-alias frequency phase offset for TX0 illumination channel with current of ILLUM_DAC_L_TX0.	

#### 7.5.1.1.59 Register 45h (Address = 45h) [reset = 0h]

### Figure 87. Register 45h

23	22	21	20	19	18	17	16			
	TMAIN_CALIB_HDR1_TX2									
	R/W - 0h									
15	14	13	12	11	10	9	8			
TMAIN_CALIB_HDR1_TX2 TEMP_COEFF_MAIN_HDR0_TX0										
	R/W	- 0h			R/W	- 0h				
7	6	5	4	3	2	1	0			
	TEMP_COEFF_MAIN_HDR0_TX0									
	R/W - 0h									

#### Table 89. Register 45 Field Descriptions

Bit	Field	Туре	Reset	Description
23:12	TMAIN_CALIB_HDR1_TX2	R/W	0h	Calibration temperature of on-chip temperature sensor (TMAIN) for TX2 illumination channel with current of ILLUM_DAC_H_TX2
11:0	TEMP_COEFF_MAIN_HD R0_TX0	R/W	0h	Phase temperature coefficient of TX0 illumination channel with on-chip temperature sensor (TMAIN) for a current of ILLUM_DAC_L_TX0

#### 7.5.1.1.60 Register 46h (Address = 46h) [reset = 0h]

### Figure 88. Register 46h

23	22	21	20	19	18	17	16		
	TILLUM_CALIB_HDR1_TX2								
	R/W - 0h								
15	15 14 13 12 11 10 9 8								
	TILLUM_CALIB_HDR1_TX2 TEMP_COEFF_ILLUM_HDR0_TX0								



	R/W	' - 0h		R/W - 0h				
7 6 5 4			3	2	1	0		
	TEMP_COEFF_ILLUM_HDR0_TX0							
			R/W	′ - 0h				

#### **Table 90. Register 46 Field Descriptions**

Bit	Field	Type	Reset	Description
23:12	TILLUM_CALIB_HDR1_TX 2	R/W	0h	Calibration temperature of external temperature sensor (TILLUM) for TX2 illumination channel with current of ILLUM_DAC_H_TX2
11:0	TEMP_COEFF_ILLUM_HD R0_TX0	R/W	0h	Phase temperature coefficient of illumination source connected to TX0 pin with external temperature sensor (TILLUM) for a current of ILLUM_DAC_L_TX0.

#### 7.5.1.1.61 Register 47h (Address = 47h) [reset = 800800h]

### Figure 89. Register 47h

23	22	21	20	19	18	17	16	
	TILLUM_CALIB_HDR0_TX0							
R/W - 80h								
15	14	13	12	11	10	9	8	
	TILLUM_CALIE	B_HDR0_TX0			TMAIN_CALIE	_HDR0_TX0	8	
	R/W	- 0h			R/W	- 8h		
7	6	5	4	3	2	1	0	
TMAIN_CALIB_HDR0_TX0								
	R/W - 0h							

#### **Table 91. Register 47 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:12	TILLUM_CALIB_HDR0_TX 0	R/W	800h	Calibration temperature of external temperature sensor (TILLUM) for TX0 illumination channel with current of ILLUM_DAC_L_TX0
11:0	TMAIN_CALIB_HDR0_TX0	R/W	800h	Calibration temperature of on-chip temperature sensor (TMAIN) for TX0 illumination channel with current of ILLUM_DAC_L_TX0

#### 7.5.1.1.62 Register 48h (Address = 48h) [reset = 0h]

#### Figure 90. Register 48h

23	22	21	20	19	18	17	16	
	TILLUM_CALIB_HDR1_TX0							
R/W - 0h								
15	14	13	12	11	10	9	8	
	TILLUM_CALIE	B_HDR1_TX0			TMAIN_CALIE	B_HDR1_TX0	8 0	
	R/W	- 0h			R/W	- 0h		
7	6	5	4	3	2	1	0	
TMAIN_CALIB_HDR1_TX0								
	R/W - 0h							

#### **Table 92. Register 48 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:12	TILLUM_CALIB_HDR1_TX 0	R/W	0h	Calibration temperature of external temperature sensor (TILLUM) for TX0 illumination channel with current of ILLUM_DAC_H_TX0
11:0	TMAIN_CALIB_HDR1_TX0	R/W	0h	Calibration temperature of on-chip temperature sensor (TMAIN) for TX0 illumination channel with current of ILLUM_DAC_H_TX0



#### 7.5.1.1.63 Register 49h (Address = 49h) [reset = 0h]

#### Figure 91. Register 49h

23	22	21	20	19	18	17	16	
	TILLUM_CALIB_HDR0_TX1							
R/W - 0h								
15	14	13	12	11	10	9	8	
	TILLUM_CALII	B_HDR0_TX1			TMAIN_CALIE	B_HDR0_TX1		
	R/W	- 0h			R/W	- 0h		
7	6	5	4	3	2	1	0	
TMAIN_CALIB_HDR0_TX1								
	R/W - 0h							

#### **Table 93. Register 49 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:12	TILLUM_CALIB_HDR0_TX	R/W	0h	Calibration temperature of external temperature sensor (TILLUM) for TX1 illumination channel with current of ILLUM_DAC_L_TX1
11:0	TMAIN_CALIB_HDR0_TX1	R/W	0h	Calibration temperature of on-chip temperature sensor (TMAIN) for TX0 illumination channel with current of ILLUM_DAC_L_TX1

#### 7.5.1.1.64 Register 4Ah (Address = 4Ah) [reset = 0h]

### Figure 92. Register 4Ah

23	22	21	20	19	18	17	16	
	RESE	RVED		SCALE_NL_CORR_COEFF A0_COEFF_HDR0_TX0			_HDR0_TX0	
	R/W	- 0h		R/W	- 0h	R/W - 0h		
15	15 14 13 12			11	10	9	8	
	A0_COEFF_HDR0_TX0							
			R/W	′ - 0h				
7	6	5	4	3	2	1	0	
		RESERVED	EN_NL_CORR					
		R/W	/ - 0h			R/W - 0h	R/W - 0h	

#### **Table 94. Register 4A Field Descriptions**

Bit	Field	Туре	Reset	Description
23:20	RESERVED	R/W	0h	Always read or write 0h.
19:18	SCALE_NL_CORR_COEF F	R/W	0h	Scaling factor for nonlinearity correction coefficients $(A^*\_COEFF\_HDR< i>_TX< j>_, i = 0,1; j = 0, 1, 2)$
17:2	A0_COEFF_HDR0_TX0	R/W	0h	0th order coefficient for square wave nonlinearity correction
1	RESERVED	R/W	0h	Always read or write 0h.
0	EN_NL_CORR	R/W	0h	Enables square wave harmonic nonlinearity correction

#### 7.5.1.1.65 Register 4Bh (Address = 4Bh) [reset = 407h]

### Figure 93. Register 4Bh

23	22	21	20	19	18	17	16		
	RESERVED								
	R - 0h								
15	14	13	12	8					
	A1_COEFF_HDR0_TX0								
			R/W	- 04h					
7	6	5	4	3	2	1	0		
			A1_COEFF	_HDR0_TX0					



R/W - 07h

#### Table 95. Register 4B Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	RESERVED	R	0h	Always read or write 0h.
15:0	A1_COEFF_HDR0_TX0	R/W	407h	First-order coefficient for square wave nonlinearity correction for TX0 illumination channel with current of ILLUM_DAC_L_TX0.

#### 7.5.1.1.66 Register 4Ch (Address = 4Ch) [reset = F23Eh]

#### Figure 94. Register 4Ch

23	22	21	20	19	18	17	16		
RESERVED 0									
R - 0h									
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h		
15	14	13	13 12		10	9	8		
			A2_COEFF_	_HDR0_TX0					
			R/W	- F2h					
7	6	5	4	3	2	1	0		
A2_COEFF_HDR0_TX0									
	R/W - 3Eh								

### Table 96. Register 4C Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	RESERVED	R	0h	Always read or write 0h.
15:0	A2_COEFF_HDR0_TX0	R/W	F23Eh	Second-order coefficient for square wave nonlinearity correction for TX0 illumination channel with current of ILLUM_DAC_L_TX0.

#### 7.5.1.1.67 Register 4Dh (Address = 4Dh) [reset = 1144h]

#### Figure 95. Register 4Dh

23	22	21	20	19	18	17	16		
RESERVED									
R - 0h									
15	15 14 13 12 11 10 9 8						8		
A3_COEFF_HDR0_TX0									
			R/W	- 11h					
7	6	5	4	3	2	1	0		
A3_COEFF_HDR0_TX0									
R/W - 44h									

#### **Table 97. Register 4D Field Descriptions**

Bit	t	Field	Туре	Reset	Description
23:1	6	RESERVED	R	0h	
15:0	0	A3_COEFF_HDR0_TX0	R/W	1144h	Third-order coefficient for square wave nonlinearity correction for TX0 illumination channel with current of ILLUM_DAC_L_TX0.

#### 7.5.1.1.68 Register 4Eh (Address = 4Eh) [reset = F881h]



### Figure 96. Register 4Eh

23	22	21	20	19	18	17	16		
RESERVED									
R - 0h									
15	14	13	12	11	10	9	8		
A4_COEFF_HDR0_TX0									
			R/W	- F8h					
7	6	5	4	3	2	1	0		
A4_COEFF_HDR0_TX0									
	R/W - 81h								

#### Table 98. Register 4E Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	RESERVED	R	0h	
15:0	A4_COEFF_HDR0_TX0	R/W		Fourth-order coefficient for square wave nonlinearity correction for TX0 illumination channel with current of ILLUM_DAC_L_TX0

### 7.5.1.1.69 Register 50h (Address = 50h) [reset = 200100h]

### Figure 97. Register 50h

23	22	21	20	19	18	17	16
0	OVERRIDE_CL KGEN_REG	1	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 1h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	1
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 1h
7	6	5	4	3	2	1	0
0	0	0	0	CLIP_MODE_O FFSET	CLIP_MODE_T EMP	CLIP_MODE_N L	CLIP_MODE_F C
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h

#### Table 99. Register 50 Field Descriptions

Bit	Field	Type	Reset	Description
23	RESERVED	R/W	0h	Always read or write 0h.
22	OVERRIDE_CLKGEN_RE G	R/W	0h	Setting this register to 1 allows user to independently control DEALIAS_FREQ, DEALIAS_EN.
21:4	RESERVED	R/W 2 0010h		Always read or write 2 0010h.
3	CLIP_MODE_OFFSET	R/W	0h	Chooses either clipping or wrap around when applying offset correction for phase.  0: Wrap around   1: Clip
2	CLIP_MODE_TEMP	R/W	0h	Chooses either clipping or wrap around when applying temperature correction for phase.  0: Wrap around   1: Clip
1	CLIP_MODE_NL	R/W	0h	Chooses either clipping or wrap around when applying nonlinearity correction for phase.  0: Wrap around   1: Clip
0	CLIP_MODE_FC	R/W	0h	Chooses clipping or wrap around when applying freq-correction for phase.  0: Wrap around   1: Clip

# 7.5.1.1.70 Register 51h (Address = 51h) [reset = 0h]



### Figure 98. Register 51h

23	22	21	20	19	18	17	16		
TEMP_COEFF_ILLUM_HDR1_TX0[11:4]									
R/W - 0h									
15 14 13 12 11 10 9 8							8		
PHASE_OFFSET_HDR1_TX0									
			R/W	/ - 0h					
7	7 6 5 4 3 2 1 0								
PHASE_OFFSET_HDR1_TX0									
	R/W - 0h								

#### Table 100. Register 51 Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	TEMP_COEFF_ILLUM_HD R1_TX0[11:4]	R/W	0h	Phase temperature coefficient of illumination source connected to TX0 pin with external temperature sensor (TILLUM) for current of ILLUM_DAC_H_TX0.
15:0	PHASE_OFFSET_HDR1_T X0	R/W	0h	Phase offset for TX0 illumination channel with current of ILLUM_DAC_H_TX0

#### 7.5.1.1.71 Register 52h (Address = 52h) [reset = 0h]

#### Figure 99. Register 52h

23	22	21	21 20		18	17	16		
	TEMP_COEFF_ILLU	JM_HDR1_TX0[	[3:0]	RESERVED					
R/W - 0h					R/W	- 0h			
15 14 13 12			11	10	9	8			
	PHASE_OFFSET_HDR0_TX1								
			R/W	- 0h					
7	6	5	4	3	2	1	0		
	PHASE_OFFSET_HDR0_TX1								
	R/W - 0h								

#### **Table 101. Register 52 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:20	TEMP_COEFF_ILLUM_HD R1_TX0[3:0]	R/W	0h	Phase temperature coefficient of illumination source connected to TX0 pin with external temperature sensor (TILLUM) for current of ILLUM_DAC_H_TX0.
15:0	PHASE_OFFSET_HDR0_T X1	R/W	0h	Phase offset for TX1 illumination channel with current of ILLUM_DAC_L_TX1

### 7.5.1.1.72 Register 53h (Address = 53h) [reset = 0h]

### Figure 100. Register 53h

23	22	21	20	19	18	17	16		
TEMP_COEFF_ILLUM_HDR0_TX1[11:4]									
R/W - 0h									
15	15 14 13 12 11 10 9 8								
PHASE_OFFSET_HDR1_TX1									
R/W - 0h									
7	6	5	4	3	2	1	0		
PHASE_OFFSET_HDR1_TX1									
R/W - 0h									



### Table 102. Register 53 Field Descriptions

Bit	Field Type Res		Reset	Description
23:16	TEMP_COEFF_ILLUM_HD R0_TX1[11:4]	R/W	0h	Phase temperature coefficient of illumination source connected to TX1 pin with external temperature sensor (TILLUM) for current of ILLUM_DAC_L_TX1.
15:0	PHASE_OFFSET_HDR1_T X1	R/W	0h	Phase offset for TX1 illumination channel with current of ILLUM_DAC_H_TX1

#### 7.5.1.1.73 Register 54h (Address = 54h) [reset = 0h]

### Figure 101. Register 54h

23	22	21	20	19	18	17	16		
	TEMP_COEFF_ILLU	JM_HDR0_TX1[	[3:0]	RESERVED					
	R/W	- 0h		R/W - 0h					
15	15 14 13 12				10	9	8		
	PHASE_OFFSET_HDR0_TX2								
	R/W - 0h								
7	6	5	4	3	2	1	0		
PHASE_OFFSET_HDR0_TX2									
	R/W - 0h								

### Table 103. Register 54 Field Descriptions

Bit	Field	Туре	Reset	Description
23:20	TEMP_COEFF_ILLUM_HD R0_TX1[3:0]	R/W	0h	Phase temperature coefficient of illumination source connected to TX1 pin with external temperature sensor (TILLUM) for current of ILLUM_DAC_L_TX1.
19:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	PHASE_OFFSET_HDR0_T X2	R/W	0h	Phase offset for TX2 illumination channel with current of ILLUM_DAC_L_TX2

#### 7.5.1.1.74 Register 55h (Address = 55h) [reset = 0h]

### Figure 102. Register 55h

23	22	21	20	19	18	17	16		
TEMP_COEFF_ILLUM_HDR1_TX1[11:4]									
R/W - 0h									
15	15 14 13 12 11 10 9 8								
PHASE_OFFSET_HDR1_TX2									
R/W - 0h									
7	6	5	4	3	2	1	0		
PHASE_OFFSET_HDR1_TX2									
R/W - 0h									

### Table 104. Register 55 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_ILLUM_HD R1_TX1[11:4]	R/W	0h	Phase temperature coefficient of illumination source connected to TX1 pin with external temperature sensor (TILLUM) for current of ILLUM_DAC_H_TX1.
15:0	PHASE_OFFSET_HDR1_T X2	R/W	0h	Phase offset for TX2 illumination channel with current of ILLUM_DAC_H_TX2



### 7.5.1.1.75 Register 56h (Address = 56h) [reset = 0h]

### Figure 103. Register 56h

23	22	21	20	19	18	17	16	
-	TEMP_COEFF_ILLU	JM_HDR1_TX1	[3:0]	RESERVED				
				R/W - 0h				
15	14	13	12	11	10	9	8	
			PHASE2_OFFS	ET_HDR1_TX0				
			R/W	- 0h				
7	6	5	4	3	2	1	0	
	PHASE2_OFFSET_HDR1_TX0							
			R/W	- 0h	·			

### **Table 105. Register 56 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:20	TEMP_COEFF_ILLUM_HD R1_TX1[3:0]	R/W	0h	Phase temperature coefficient of illumination source connected to TX1 pin with external temperature sensor (TILLUM) for current of ILLUM_DAC_H_TX1.
19:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	PHASE2_OFFSET_HDR1_ TX0	R/W	0h	De-alias frequency phase offset for TX0 illumination channel with current of ILLUM_DAC_H_TX0

### 7.5.1.1.76 Register 57h (Address = 57h) [reset = 0h]

### Figure 104. Register 57h

23	22	21	20	19	18	17	16
		Т	EMP_COEFF_ILL	UM_HDR0_TX2[11	1:4]		
			R/W	/ - 0h			
15	14	13	12	11	10	9	8
			PHASE2_OFFS	SET_HDR0_TX1			
			R/W	/ - 0h			
7	6	5	4	3	2	1	0
PHASE2_OFFSET_HDR0_TX1							
			R/W	/ - 0h			

### Table 106. Register 57 Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	TEMP_COEFF_ILLUM_HD R0_TX2[11:4]	R/W	0h	Phase temperature coefficient of illumination source connected to TX2 pin with external temperature sensor (TILLUM) for current of ILLUM_DAC_L_TX2.
15:0	PHASE2_OFFSET_HDR0_ TX1	R/W	0h	De-alias frequency phase offset for TX1 illumination channel with current of ILLUM_DAC_L_TX1

# 7.5.1.1.77 Register 58h (Address = 58h) [reset = 0h]

# Figure 105. Register 58h

23	22	21	20	19	18	17	16
	TEMP_COEFF_ILLU	M_HDR0_TX2[	3:0]		RESE	RVED	
					R/W	- 0h	
15	14	13	12	11	10	9	8
			PHASE2_OFFS	ET_HDR1_TX1			
7	6	5	4	3	2	1	0
			PHASE2_OFFS	ET_HDR1_TX1			



### Table 107. Register 58 Field Descriptions

Bit	Field	Туре	Reset	Description
23:20	TEMP_COEFF_ILLUM_HD R0_TX2[3:0]	R/W	0h	Phase temperature coefficient of illumination source connected to TX2 pin with external temperature sensor (TILLUM) for current of ILLUM_DAC_L_TX2.
19:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	PHASE2_OFFSET_HDR1_ TX1	R/W	0h	De-alias frequency phase offset for TX1 illumination channel with current of ILLUM_DAC_H_TX1

### 7.5.1.1.78 Register 59h (Address = 59h) [reset = 0h]

### Figure 106. Register 59h

23	22	21	20	19	18	17	16
		Т	EMP_COEFF_ILLU	JM_HDR1_TX2[11	:4]		
			R/W	/ - 0h			
15	14	13	12	11	10	9	8
			PHASE2_OFFS	SET_HDR0_TX2			
			R/W	/ - 0h			
7	6	5	4	3	2	1	0
	PHASE2_OFFSET_HDR0_TX2						
			R/W	/ - 0h			

### Table 108. Register 59 Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	TEMP_COEFF_ILLUM_HD R1_TX2[11:4]	R/W	0h	Phase temperature coefficient of illumination source connected to TX2 pin with external temperature sensor (TILLUM) for current of ILLUM_DAC_H_TX2.
15:0	PHASE2_OFFSET_HDR0_ TX2	R/W	0h	De-alias frequency phase offset for TX2 illumination channel with current of ILLUM_DAC_L_TX2

### 7.5.1.1.79 Register 5Ah (Address = 5Ah) [reset = 0h]

## Figure 107. Register 5Ah

23	22	21	20	19	18	17	16	
	TEMP_COEFF_ILLU	JM_HDR1_TX2[	[3:0]	RESERVED				
					R/W	- 0h		
15	14	13	12	11	10	9	8	
			PHASE2_OFFS	ET_HDR1_TX2				
			R/W	- 0h				
7	6	5	4	3	2	1	0	
	PHASE2_OFFSET_HDR1_TX2							
			R/W	- 0h				

## Table 109. Register 5A Field Descriptions

Bit	Field	Type	Reset	Description
23:20	TEMP_COEFF_ILLUM_HD R1_TX2[3:0]	R/W	0h	Phase temperature coefficient of illumination source connected to TX2 pin with external temperature sensor (TILLUM) for current of ILLUM_DAC_H_TX2.
19:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	PHASE2_OFFSET_HDR1_ TX2	R/W	0h	De-alias frequency phase offset for TX2 illumination channel with current of ILLUM_DAC_H_TX2



### 7.5.1.1.80 Register 5Bh (Address = 5Bh) [reset = 0h]

### Figure 108. Register 5Bh

23	22	21	20	19	18	17	16
		TEMP_C	COEFF_ILLUM_X	TALK_IPHASE_HI	DR1_TX1		
			R/W	' - 0h			
15	14	13	12	11	10	9	8
		TEMP_C	COEFF_ILLUM_X	TALK_IPHASE_HI	DR0_TX1		
			R/W	' - 0h			
7	6	5	4	3	2	1	0
TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR1_TX0							
			R/W	' - 0h			

### Table 110. Register 5B Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	TEMP_COEFF_ILLUM_XT ALK_IPHASE_HDR1_TX1	R/W	0h	Temperature coefficient of crosstalk in-phase component with TILLUM for TX1 channel with ILLUM_DAC_H_TX1 current.
15:8	TEMP_COEFF_ILLUM_XT ALK_IPHASE_HDR0_TX1	R/W	0h	Temperature coefficient of crosstalk in-phase component with TILLUM for TX1 channel with ILLUM_DAC_L_TX1 current.
7:0	TEMP_COEFF_ILLUM_XT ALK_IPHASE_HDR1_TX0	R/W	0h	Temperature coefficient of crosstalk in-phase component with TILLUM for TX0 channel with ILLUM_DAC_H_TX0 current.

#### 7.5.1.1.81 Register 5Ch (Address = 5Ch) [reset = 0h]

### Figure 109. Register 5Ch

23	22	21	20	19	18	17	16	
		TEMP_C	OEFF_ILLUM_XT	ALK_QPHASE_H	DR1_TX0			
			R/W	' - 0h				
15	14	13	12	11	10	9	8	
		TEMP_C	OEFF_ILLUM_X1	TALK_IPHASE_HE	DR1_TX2			
			R/W	' - 0h				
7	6	5	4	3	2	1	0	
	TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR0_TX2							
			R/W	' - 0h				

### **Table 111. Register 5C Field Descriptions**

Bit	Field	Туре	Reset	Description
23:16	TEMP_COEFF_ILLUM_XT ALK_QPHASE_HDR1_TX0	R/W	0h	Temperature coefficient of crosstalk quadrature-phase component with TILLUM for TX0 channel with ILLUM_DAC_H_TX0 current.
15:8	TEMP_COEFF_ILLUM_XT ALK_IPHASE_HDR1_TX2	R/W	0h	Temperature coefficient of crosstalk in-phase component with TILLUM for TX2 channel with ILLUM_DAC_H_TX2 current.
7:0	TEMP_COEFF_ILLUM_XT ALK_IPHASE_HDR0_TX2	R/W	0h	Temperature coefficient of crosstalk in-phase component with TILLUM for TX2 channel with ILLUM_DAC_H_TX2 current.

## 7.5.1.1.82 Register 5Dh (Address = 5Dh) [reset = 0h]

### Figure 110. Register 5Dh

23	22	21	20	19	18	17	16	
	TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR0_TX2							
	R/W - 0h							
15	14	13	12	11	10	9	8	
	TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR1_TX1							
			R/W	- 0h				



7	6	5	4	3	2	1	0
		TEMP_C	OEFF_ILLUM_XT/	ALK_QPHASE_H	IDR0_TX1		
			R/W	- 0h			

### Table 112. Register 5D Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	TEMP_COEFF_ILLUM_XT ALK_QPHASE_HDR0_TX2	R/W	0h	Temperature coefficient of crosstalk quadrature-phase component with TILLUM for TX2 channel with ILLUM_DAC_L_TX2 current.
15:8	TEMP_COEFF_ILLUM_XT ALK_QPHASE_HDR1_TX1	R/W	0h	Temperature coefficient of crosstalk quadrature-phase component with TILLUM for TX1 channel with ILLUM_DAC_H_TX1 current.
7:0	TEMP_COEFF_ILLUM_XT ALK_QPHASE_HDR0_TX1	R/W	0h	Temperature coefficient of crosstalk quadrature-phase component with TILLUM for TX1 channel with ILLUM_DAC_L_TX1 current.

### 7.5.1.1.83 Register 5Eh (Address = 5Eh) [reset = 0h]

### Figure 111. Register 5Eh

23	22	21	20	19	18	17	16
		TEM	IP_COEFF_XTAL	K_IPHASE_HDR0	_TX1		
			R/W	' - 0h			
15	14	13	12	11	10	9	8
		TEM	IP_COEFF_XTAL	K_IPHASE_HDR1	_TX0		
			R/W	' - 0h			
7	6	5	4	3	2	1	0
	TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR1_TX2						
			R/W	' - 0h			

### Table 113. Register 5E Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	TEMP_COEFF_XTALK_IP HASE_HDR0_TX1	R/W	0h	Temperature coefficient of crosstalk in-phase component with TMAIN for TX1 channel with ILLUM_DAC_L_TX1 current
15:8	TEMP_COEFF_XTALK_IP HASE_HDR1_TX0	R/W	0h	Temperature coefficient of crosstalk in-phase component with TMAIN for TX0 channel with ILLUM_DAC_H_TX0 current
7:0	TEMP_COEFF_ILLUM_XT ALK_QPHASE_HDR1_TX2	R/W	0h	Temperature coefficient of crosstalk quadrature-phase component with TILLUM for TX2 channel with ILLUM_DAC_H_TX2 current.

## 7.5.1.1.84 Register 5Fh (Address = 5Fh) [reset = 0h]

### Figure 112. Register 5Fh

23	22	21	20	19	18	17	16	
	TEMP_COEFF_XTALK_IPHASE_HDR1_TX2							
			R/W	′ - 0h				
15	14	13	12	11	10	9	8	
		TEM	IP_COEFF_XTALI	K_IPHASE_HDR0	_TX2			
			R/W	′ - 0h				
7	6	5	4	3	2	1	0	
	TEMP_COEFF_XTALK_IPHASE_HDR1_TX1							
			R/W	′ - 0h				

### Table 114. Register 5F Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	TEMP_COEFF_XTALK_IP HASE_HDR1_TX2	R/W	0h	Temperature coefficient of crosstalk in-phase component with TMAIN for TX2 channel with ILLUM_DAC_H_TX2 current
15:8	TEMP_COEFF_XTALK_IP HASE_HDR0_TX2	R/W	0h	Temperature coefficient of crosstalk in-phase component with TMAIN for TX2 channel with ILLUM_DAC_L_TX2 current



### Table 114. Register 5F Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	TEMP_COEFF_XTALK_IP HASE_HDR1_TX1	R/W	0h	Temperature coefficient of crosstalk in-phase component with TMAIN for TX1 channel with ILLUM_DAC_H_TX1 current

### 7.5.1.1.85 Register 60h (Address = 60h) [reset = 0h]

### Figure 113. Register 60h

23	22	21	20	19	18	17	16		
	TEMP_COEFF_XTALK_QPHASE_HDR1_TX1								
			R/W	- 0h					
15	14	13	12	11	10	9	8		
		TEM	IP_COEFF_XTALK	_QPHASE_HDR(	)_TX1				
			R/W	- 0h					
7	6	5	4	3	2	1	0		
	TEMP_COEFF_XTALK_QPHASE_HDR1_TX0								
			R/W	- 0h					

### **Table 115. Register 60 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:16	TEMP_COEFF_XTALK_QP HASE_HDR1_TX1	R/W	0h	Temperature coefficient of crosstalk quadrature-phase component with TMAIN for TX1 channel with ILLUM_DAC_H_TX1 current
15:8	TEMP_COEFF_XTALK_QP HASE_HDR0_TX1	R/W	0h	Temperature coefficient of crosstalk quadrature-phase component with TMAIN for TX1 channel with ILLUM_DAC_L_TX1 current
7:0	TEMP_COEFF_XTALK_QP HASE_HDR1_TX0	R/W	0h	Temperature coefficient of crosstalk quadrature-phase component with TMAIN for TX0 channel with ILLUM_DAC_H_TX0 current

## 7.5.1.1.86 Register 61h (Address = 61h) [reset = 0h]

### Figure 114. Register 61h

23	22	21	20	19	18	17	16				
	RESERVED										
	R/W - 0h										
15	15 14 13 12 11 10 9 8										
	TEMP_COEFF_XTALK_QPHASE_HDR1_TX2										
			R/W	/ - 0h							
7	7 6 5 4 3 2 1 0										
	TEMP_COEFF_XTALK_QPHASE_HDR0_TX2										
	R/W - 0h										

## Table 116. Register 61 Field Descriptions

Bit	Field	Туре	Reset	Description	
23:16	RESERVED	R/W	0h	Always read or write 0h.	
15:8	TEMP_COEFF_XTALK_QP HASE_HDR1_TX2	R/W	0h	Temperature coefficient of crosstalk quadrature-phase component with TMAIN for TX2 channel with ILLUM_DAC_H_TX2 current	
7:0	TEMP_COEFF_XTALK_QP HASE_HDR0_TX2	R/W	0h	Temperature coefficient of crosstalk quadrature-phase component with TMAIN for TX2 channel with ILLUM_DAC_L_TX2 current	

## 7.5.1.1.87 Register 64h (Address = 64h) [reset = 280C00h]



### Figure 115. Register 64h

23	22	21	20	19	18	17	16		
PI	ROG_OVLDET_RE	FM	PF	PROG_OVLDET_REFP			RVED		
	R/W - 1h			R/W - 2h			R/W - 0h		
15	14	13	12 11 10 9						
	RESERVED								
			R/W	- 0Ch					
7	6	5	4	3	2	1	0		
	RESERVED								
	R/W - 0h								

### **Table 117. Register 64 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:21	PROG_OVLDET_REFM	R/W	1h	Program overload comparator threshold 0: Default   1: 100 mV   2: 200 mV   Other values: Not valid
20:18	PROG_OVLDET_REFP	R/W	2h	Program overload comparator threshold 0: Default   2: –100 mV   Other values: Not valid
17:0	RESERVED	R/W	0C00h	Always read or write 0C00h.

### 7.5.1.1.88 Register 65h (Address = 65h) [reset = 0h]

## Figure 116. Register 65h

23	22	21	20	19	18	17	16			
DIS_OVLDET		RESERVED								
R/W - 0h		R/W - 0h								
15	14	14 13 12 11 10 9 8								
			RESI	ERVED						
			R/V	V - 0h						
7	7 6 5 4 3 2 1 0									
	RESERVED									
	R/W - 0h									

### Table 118. Register 65 Field Descriptions

Bit	Field	Туре	Reset	Description
23	DIS_OVLDET	R/W	0h	Disables AFE overload detection. 0: AFE overload detection is enabled.   1: AFE overload detection is disabled.
22:0	RESERVED	R/W	0h	Always read or write 0h.

### 7.5.1.1.89 Register 6Eh (Address = 6Eh) [reset = 20000h]

### Figure 117. Register 6Eh

23	22	21	20	19	18	17	16			
	RESE	RVED		EN_TEMP_CO NV		RESERVED				
	R/W	- 0h		R/W - 0h		R/W - 2h				
15	14	13	12	11	10	9	8			
			RESE	RVED						
			R/W	- 0h						
7	6	5	4	3	2	1	0			
	RESERVED									
	R/W - 0h									



### Table 119. Register 6E Field Descriptions

Bit	Field	Туре	Reset	Description
23:20	RESERVED	R/W	0h	Always read or write 0h.
19	EN_TEMP_CONV	R/W	0h	Enable temperature sensor conversion 0: Temperature conversion is disabled.   1: Temperature conversion is enabled.
18:0	RESERVED	R/W	2 0000h	Always read or write 2 0000h.

### 7.5.1.1.90 Register 71h (Address = 71h) [reset = 0h]

### Figure 118. Register 71h

23	22	21	20	19	18	17	16
			UNMASK_ILLU MEN_INTXTAL K	EN_ILLUM_CL K_GPIO			
		R/V	V - 0h			R/W - 0h	R/W - 0h
15	14	14 13		11	10	9	8
ILLUM_CLK_G PIO_MODE	RESE	RVED	DIS_ILLUM_CL K_TX	INVERT_AFE_ CLK	RESERVED	INVERT_TG_C LK	SHUT_CLOCK S
R/W - 0h	R/W	- 0h	R/W - 0h		R/W - 0h	R/W - 0h	R/W - 0h
7	6	5	4	3	2	1	0
RESERVED		SHIFT_ILL	DEALIAS_FRE Q	DEALIAS_EN	RESERVED		
R/W - 0h		R/V	R/W - 0h	R/W - 0h	R/W - 0h		

## **Table 120. Register 71 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:18	RESERVED	R/W	0h	Always read or write 0h.
17	UNMASK_ILLUMEN_INTX TALK	R/W	0h	Mask or unmask ILLUM_EN_TX0 going to GPIO with internal crosstalk signal 0: ILLUM_EN_TX0 is masked with internal crosstalk correction signal 1: ILLUM_EN_TX0 is not masked with internal crosstalk correction signal
16	EN_ILLUM_CLK_GPIO	R/W	0h	Enable ILLUM CLK going to GPIO 0: Illumination clock to GPIO is disabled.   1: Illumination clock to GPIO is enabled.
15	ILLUM_CLK_GPIO_MODE	R/W	0h	Disable ILLUM_EN_TX0 gating ILLUM_CLK going to GPIO.  0: ILLUM_CLK comes on GPIO only when ILLUM_EN (TG signal) is high    1: ILLUM_CLK alive always
14:13	RESERVED	R/W	0h	Always read or write 0h.
12	DIS_ILLUM_CLK_TX	R/W	0h	Disable ILLUM_CLK going to transmitter 0: Clock to illumination driver is enabled.   1: Clock to illumination driver is disabled
11	INVERT_AFE_CLK	R/W	0h	Invert CLK input to AFE. 0: AFE CLK is not inverted   1: AFE CLK is inverted.
10	RESERVED	R/W	0h	Always read or write 0h.
9	INVERT_TG_CLK	R/W	0h	Invert CLK input to timing generation unit. 0: TG CLK is not inverted   1: TG CLK is inverted.
8	SHUT_CLOCKS	R/W	0h	Shut down all CLK signals at modulation frequency.  0: Modulation clocks is alive   1: Modulation clock is shut down.
7	RESERVED	R/W	0h	Always read or write 0h.
6:3	SHIFT_ILLUM_PHASE	R/W	0h	Shift the phase of ILLUM_CLK. PHASE = SHIFT_ILLUM_PHASE × 22.5°.
2	DEALIAS_FREQ	R/W	0h	Select modulation frequency when DEALIAS_EN = 1. This register works only when OVERRIDE_CLKGEN_REG = 1. 0: 10 × (6 / 7) MHz   1: 10 × (6 / 5) MHz
1	DEALIAS_EN	R/W	0h	Change the modulation frequency. This register works only when OVERRIDE_CLKGEN_REG = 1.



### Table 120. Register 71 Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
0	RESERVED	R/W	0h	Always read or write 0h.

### 7.5.1.1.91 Register 72h (Address = 72h) [reset = C0h]

### Figure 119. Register 72h

23	22	21	20	19	18	17	16			
	RESERVED									
	R/W - 0h									
15	14	13	12	11	10	9	8			
			RESE	RVED						
			R/W	- 0h						
7	6	5	4	3	2	1	0			
	IAMB_M	AX_SEL		RESERVED						
	R/W	- Ch			R/W	- 0h				

### **Table 121. Register 72 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:8	RESERVED	R/W	0h Always read or write 0h.	
7:4	IAMB_MAX_SEL	R/W	Ch	Selects the value of ambient cancellation DAC resistor 0: 20 $\mu$ A   5: 10 $\mu$ A   10: 33 $\mu$ A   11: 50 $\mu$ A   12: 100 $\mu$ A   14: 200 $\mu$ A   Other values: Not valid.
3:0	RESERVED	R/W	0h	Always read or write 0h.

### 7.5.1.1.92 Register 76h (Address = 76h) [reset = 0h]

### Figure 120. Register 76h

23	22	21	20	19	18	17	16
			RESE	RVED			
			R/W	- 0h			
15	14	13	12	11	10	9	8
	RESE	RVED		PDN_GLOBAL	RESERVED	DIS_GLB_PD_I 2CHOST	DIS_GLB_PD_ OSC
	R/W	- 0h		R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
7	6	5	4	3	2	1	0
RESERVED	DIS_GLB_PD_ AMB_ADC	DIS_GLB_PD_ AMB_DAC	DIS_GLB_PD_ AFE_DAC	DIS_GLB_PD_ AFE	DIS_GLB_PD_I LLUM_DRV	DIS_GLB_PD_ TEMP_SENS	DIS_GLB_PD_ REFSYS
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h

## **Table 122. Register 76 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:12	RESERVED	R/W	0h	Always read or write 0h.
11	PDN_GLOBAL	R/W	Oh Global power down of all the blocks. O: Acitve   1: Power down	
10	RESERVED	R/W	0h	Always read or write 0h.
9	DIS_GLB_PD_I2CHOST	R/W	0h	Disable global power down of I <sup>2</sup> C host.  0: Enable global power down   1: Disable global power down.
8	DIS_GLB_PD_OSC	R/W	0h	Disable global power down of main oscillator.  0: Enable global power down   1: Disable global power down.
7	RESERVED	R/W	0h	Always read or write 0h.
6	DIS_GLB_PD_AMB_ADC	R/W	0h	Disable global power down of ambient ADC.  0: Enable global power down   1: Disable global power down.



# Table 122. Register 76 Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
5	DIS_GLB_PD_AMB_DAC	R/W	0h	Disable global power down of ambient cancellation.  0: Enable global power down   1: Disable global power down.
4	DIS_GLB_PD_AFE_DAC	R/W	0h	Disable global power down of AFE DAC. 0: Enable global power down   1: Disable global power down.
3	DIS_GLB_PD_AFE	R/W	0h	Disable global power down of AFE. 0: Enable global power down   1: Disable global power down.
2	DIS_GLB_PD_ILLUM_DRV	R/W	0h	Disable global power down of illumination driver.  0: Enable global power down   1: Disable global power down.
1	DIS_GLB_PD_TEMP_SEN S	R/W	0h	Disable global power down of temperature sensor.  0: Enable global power down   1: Disable global power down.
0	DIS_GLB_PD_REFSYS	R/W	0h	Disable global power down of reference. 0: Enable global power down   1: Disable global power down.

### 7.5.1.1.93 Register 77h (Address = 77h) [reset = 0h]

### Figure 121. Register 77h

23	22	21	20	19	18	17	16
			RESE	RVED			
			R/W	- 0h			
15	14	13	12	11	10	9	8
		RESERVED         EN_DYN_PD_I         EN_DYN_PI           2CHOST_OSC         OSC					
		R/W	- 0h			R/W - 0h	R/W - 0h
7	6	5	4	3	2	1	0
RESERVED	EN_DYN_PD_ AMB_ADC	EN_DYN_PD_ AMB_DAC	EN_DYN_PD_ AFE_DAC	EN_DYN_PD_ AFE	EN_DYN_PD_I LLUM_DRV	EN_DYN_PD_ TEMP_SENS	EN_DYN_PD_ REFSYS
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h

## **Table 123. Register 77 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:10	RESERVED	R/W	0h	Always read or write 0h.
9	EN_DYN_PD_I2CHOST_O SC	R/W	0h	Enable dynamic power down of I <sup>2</sup> C host oscillator.  0: Disable dynamic power down   1: Enable dynamic power down.
8	EN_DYN_PD_OSC	R/W	0h	Enable dynamic power down of main oscillator.  0: Disable dynamic power down   1: Enable dynamic power down.
7	RESERVED	R/W	0h	Always read or write 0h.
6	EN_DYN_PD_AMB_ADC	R/W	0h	Enable dynamic power down of ambient ADC.  0: Disable dynamic power down   1: Enable dynamic power down.
5	EN_DYN_PD_AMB_DAC	R/W	0h	Enable dynamic power down of ambient cancellation.  0: Disable dynamic power down   1: Enable dynamic power down.
4	EN_DYN_PD_AFE_DAC	R/W	0h	Enable dynamic power down of AFE DAC.  0: Disable dynamic power down   1: Enable dynamic power down.
3	EN_DYN_PD_AFE	R/W	0h	Enable dynamic power down of AFE.  0: Disable dynamic power down   1: Enable dynamic power down.
2	EN_DYN_PD_ILLUM_DRV	R/W	0h	Enable dynamic power down of illumination driver.  0: Disable dynamic power down   1: Enable dynamic power down.
1	EN_DYN_PD_TEMP_SEN S	R/W	0h	Enable dynamic power down of temperature sensor.  0: Disable dynamic power down   1: Enable dynamic power down.
0	EN_DYN_PD_REFSYS	R/W	0h	Enable dynamic power down of reference.  0: Disable dynamic power down   1: Enable dynamic power down.



### 7.5.1.1.94 Register 78h (Address = 78h) [reset = 0h]

### Figure 122. Register 78h

23	22	21	20	19	18	17	16
RESERVED	SEL_GP3_ON_ SDAM			RESERVED			GPIO2_IBUF_E N
R/W - 0h	R/W - 0h			R/W - 0h			R/W - 0h
15	14	13	12	11	10	9	8
GPIO2_OBUF_ EN	RESE	RVED	GPIO1_OBUF_ EN		GPO2_MUX_SE	L	GPO1_MUX_S EL
R/W - 0h	R/W	- 0h	R/W - 0h		R/W - 0h		R/W - 0h
7	6	5	4	3	2	1	0
GPO1_M	IUX_SEL		RESERVED	GPO3_MUX_SEL	=		
R/W	- 0h		R/W - 0h R/W - 0				

### Table 124. Register 78 Field Descriptions

Bit	Field	Туре	Reset	Description
23	RESERVED	R/W	0h	Always read or write 0h.
22	SEL_GP3_ON_SDAM	R/W	0h	Select GP3 on SDA_M pin. This feature can be used when I <sup>2</sup> C host is not used in the system. Pull up need to be present on SDA_M pin. To save power the signal on this pin are inverted (active low).
21:17	RESERVED	R/W	0h	Always read or write 0h.
16	GPIO2_IBUF_EN	R/W	0h	Enable input buffer on GP2 pin. Used for reference CLK input.  0: Disable input buffer   1: Enable input buffer.
15	GPIO2_OBUF_EN	R/W	0h	Enable output buffer on GP2 pin. 0: Disable output buffer   1: Enable output buffer.
14:13	RESERVED	R/W	0h	Always read or write 0h.
12	GPIO1_OBUF_EN	R/W	0h	Enable output buffer on GP1 pin. 0: Disable output buffer   1: Enable output buffer.
11:9	GPO2_MUX_SEL	R/W	0h	Select signal for the GP2 output multiplexer. 0: DVSS   2: DIG_GPO_0   3: DIG_GPO_1   7: ILLUM_EN_TX0   Other values: Not valid.
8:6	GPO1_MUX_SEL	R/W	0h	Select signal for the GP1 output multiplexer. 0: DVSS   2: DIG_GPO_0   3: DIG_GPO_1   7: ILLUM_CLK   Other values: Not valid.
5:3	RESERVED	R/W	0h	Always read or write 0h.
2:0	GPO3_MUX_SEL	R/W	0h	Select signal for the GP3 output multiplexer. 0: DVSS   2: DIG_GPO_0   3: DIG_GPO_1   7: DIG_GPO_2   Other values: Not valid.

### 7.5.1.1.95 Register 79h (Address = 79h) [reset = 1h]

### Figure 123. Register 79h

23	22	21	20	19	18	17	16
	RESER	VED		PDN_ILLUM_D RV		RESERVED	
	R/W -	0h		R/W - 0h		R/W - 0h	
15	14	13	12	11	10	9	8
	RESERVED		PDN_ILLUM_D C_CURR		ILLUM_DC_	CURR_DAC	
	R/W - 0h		R/W - 0h		R/W	- 0h	
7	6	5	4	3	2	1	0
	RESERVED		EN_TX_DC_C URR_ALL	SEL_ILLUM_T X0_ON_TX1	EN_TX_CLKZ	RESERVED	EN_TX_CLKB
	R/W - 0h		R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 1h



### Table 125. Register 79 Field Descriptions

Bit	Field	Туре	Reset	Description
23:20	RESERVED	R/W	0h	Always read or write 0.
19	PDN_ILLUM_DRV	R/W	0h	Test-mode bit to power down the illumination driver.  0: Illumination driver is active   1: Illumination driver is powered down.
18:14	RESERVED	R/W	0h	Always read or write 0.
12	PDN_ILLUM_DC_CURR	R/W	Power down the dc bias current through the TX pins.  0: Illumination dc bias current is active   1: Illumination dc bias curpowered down.	
11:8	ILLUM_DC_CURR_DAC	R/W	0h	DC current through TX pin = 0.5 mA × ILLUM_DC_CURR_DAC
7:5	RESERVED	R/W	0h	Always read or write 0.
4	EN_TX_DC_CURR_ALL	R/W	0h	Enable dc current of all TX channels when TX0 is selected.
3	SEL_ILLUM_TX0_ON_TX1	R/W	0h	Use ILLUM_EN_TX0 for TX1. This mode is required to enable static current-drive mode.  0: TX1 is controlled by SEL_TX_CH   0: TX1 is selected when TX0 is active.
2	EN_TX_CLKZ	R/W	0h	Enable inverted modulation CLK. 0: Inverted modulation clock is disabled   1: Inverted modulation clock is enabled.
1	RESERVED	R/W	0h	Always read or write 0.
0	EN_TX_CLKB	R/W	1h	Enable modulation CLK. 0: Modulation clock is disabled   1: Modulation clock is enabled.

## 7.5.1.1.96 Register 7Ah (Address = 7Ah) [reset = 0h]

### Figure 124. Register 7Ah

23	22	21	20	19	18	17	16
			RESEI	RVED			
			R/W	- 0h			
15	14	13	12	11	10	9	8
			RESEI	RVED			
			R/W	- 0h			
7	6	5	4	3	2	1	0
RESE	RVED	TX0_PIN_CONFIG TX2_PIN_CONFIG TX1_PIN_CONFIG					
R/W	/ - 0h	R/W	/ - 0h	R/W	′ - 0h	R/W	' - 0h

### **Table 126. Register 7A Field Descriptions**

Bit	Field	Туре	Reset	Description
23:6	RESERVED	R/W	0h	Always read or write 0.
5:4	TX0_PIN_CONFIG	R/W	0h	Configure TX0 pin. 0: CLKB   2: CLKZ   3: 1   Other values: Not valid
3:2	TX2_PIN_CONFIG	R/W	0h	Configure TX2 pin. 0: CLKB   2: CLKZ   3: 1   Other values: Not valid
1:0	TX1_PIN_CONFIG	R/W	0h	Configure TX1 pin. 0: CLKB   2: CLKZ   3: 1   Other values: Not valid

### 7.5.1.1.97 Register 80h (Address = 80h) [reset = 4E1Eh]

### Figure 125. Register 80h

23	22	21	20	19	18	17	16			
DIS_TG_ACON F		RESERVED SUB_VD_CLK_ CNT								
R/W - 0h		R/W - 0h								
15	14	13	12	11	10	9	8			
SUB_VD_CLK_CNT										
R/W - 4Eh										



7	6	5	4	3	2	1	0		
SUB_VD_CLK_CNT									
	R/W - 0Fh								

#### **Table 127. Register 80 Field Descriptions**

Bit	Field	Туре	Reset	Description
23	DIS_TG_ACONF	R/W	0h	Disable automatic configuration of TG registers: TG_CAPTURE_MASK_*, TG_OVL_WINDOW_MSAK*, TG_ILLUMEN_MASK*, TG_CALC_MASK*, TG_DYNPDN_MASK*. If these TG signals must be configured by the user, DIS_TG_ACONF should be set 1 to override the default settings of the above mentioned TG signal registers.
22:17	RESERVED	R/W	0h	Always read or write 0h.
16:1	SUB_VD_CLK_CNT	R/W	270Fh	The number of TG clocks in a sub-frame.
0	TG_EN	R/W	0h	Enable the timing generation unit. 0: TG is disabled   1: TG is enabled.

### 7.5.1.1.98 Register 83h (Address = 83h) [reset = D0h]

### Figure 126. Register 83h

23	22	21	20	19	18	17	16			
RESERVED										
R/W - 0h										
15	14	13	12	11	10	9	8			
TG_AFE_RST_START										
			R/W	- 00h						
7	6	5	4	3	2	1	0			
	TG_AFE_RST_START									
	R/W - D0h									

### Table 128. Register 83 Field Descriptions

Bit	Field	Туре	Reset	Description	
23:16	23:16 RESERVED R/W 0h Always read or write 0h.				
15:0	TG_AFE_RST_START	R/W	D0h	This register defines the starting position of AFE data-path reset TG signal in the number of TG CLKs ( $t_{CLK}$ ) in a sub-frame. Pulse duration of this reset signal is (TG_AFE_RST_END – TG_AFE_RST_START) × $t_{CLK}$ .	

# 7.5.1.1.99 Register 84h (Address = 84h) [reset = D8h]

## Figure 127. Register 84h

23	22	21	20	19	18	17	16			
RESERVED										
R/W - 0h										
15	14	13	12	11	10	9	8			
TG_AFE_RST_END										
			R/W	- 00h						
7	6	5	4	3	2	1	0			
	TG_AFE_RST_END									
	R/W - D8h									



### **Table 129. Register 84 Field Descriptions**

Bit	Field	Type	Reset	Description
23:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	TG_AFE_RST_END	R/W	D8h	This register defines the ending position of the AFE data-path reset TG signal in the number of TG clocks ( $t_{CLK}$ ) in a sub-frame.

#### 7.5.1.1.100 Register 85h (Address = 85h) [reset = 20h]

### Figure 128. Register 85h

23	22	21	20	19	18	17	16			
RESERVED										
R/W - 0h										
15	14	13	12	11	10	9	8			
TG_SEQ_INT_START										
			R/W	- 00h						
7	6	5	4	3	2	1	0			
TG_SEQ_INT_START										
	R/W - 20h									

## Table 130. Register 85 Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	TG_SEQ_INT_START	R/W	20h	Starting position of the sequencer interrupt TG signal in the number of TG clocks (t <sub>CLK</sub> ) in a sub-frame.

### 7.5.1.1.101 Register 86h (Address = 86h) [reset = 28h]

### Figure 129. Register 86h

23	22	21	20	19	18	17	16				
RESERVED											
R/W - 0h											
15	14	13	12	11	10	9	8				
	TG_SEQ_INT_END										
			R/W	- 00h							
7	6	5	4	3	2	1	0				
	TG_SEQ_INT_END										
	R/W - 28h										

### **Table 131. Register 86 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	TG_SEQ_INT_END	R/W	28h	Ending position of the sequencer interrupt TG signal in the number of TG clocks (t <sub>CLK</sub> ) in a sub-frame.

### 7.5.1.1.102 Register 87h (Address = 87h) [reset = 2454h]

### Figure 130. Register 87h

23	22	21	20	19	18	17	16			
RESERVED										
R/W - 0h										
15 14 13 12 11 10 9 8										



			TG_CAPTU	JRE_START				
R/W - 24h								
7	7 6 5 4 3 2 1 0							
	TG_CAPTURE_START							
		R/W - 54h						

### Table 132. Register 87 Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	TG_CAPTURE_START	R/W		Starting position of the internal data capture TG signal in the number of TG clocks ( $t_{\rm CLK}$ ) in a sub-frame.

### 7.5.1.1.103 Register 88h (Address = 88h) [reset = 2648h]

### Figure 131. Register 88h

23	22	21	20	19	18	17	16
			RESE	RVED			
			R/W	/ - 0h			
15	14	13	12	11	10	9	8
			TG_CAPT	TURE_END			
			R/W	- 26h			
7	6	5	4	3	2	1	0
TG_CAPTURE_END							
	R/W - 48h						

### **Table 133. Register 88 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	TG_CAPTURE_END	R/W		Ending position of the internal data capture TG signal in the number of TG clocks (t <sub>CLK</sub> ) in a sub-frame.

### 7.5.1.1.104 Register 89h (Address = 89h) [reset = 3E8h]

### Figure 132. Register 89h

23	22	21	20	19	18	17	16
			RESE	RVED			
	R/W - 0h						
15	14	13	12	11	10	9	8
	TG_OVL_WINDOW_START						
			R/W	- 03h			
7	6	5	4	3	2	1	0
	TG_OVL_WINDOW_START						
	R/W - E8h						

### Table 134. Register 89 Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	TG_OVL_WINDOW_STAR	R/W	3E8h	Starting position of the AFE overload observation window TG signal in the number of TG clocks ( $t_{\rm CLK}$ ) in a sub-frame.



### 7.5.1.1.105 Register 8Ah (Address = 8Ah) [reset = 1F40h]

### Figure 133. Register 8Ah

23	22	21	20	19	18	17	16
			RESE	RVED			
	R/W - 0h						
15	14	13	12	11	10	9	8
	TG_OVL_WINDOW_END						
			R/W	- 1Fh			
7	6	5	4	3	2	1	0
	TG_OVL_WINDOW_END						
	R/W - 40h						

### Table 135. Register 8A Field Descriptions

	Bit	Field	Туре	Reset	Description
2	23:16	RESERVED	R/W	0h	Always read or write 0h.
,	15:0	TG_OVL_WINDOW_END	R/W	1F40h	Ending position of the AFE overload observation window TG signal in the number of TG clocks ( $t_{\rm CLK}$ ) in a sub-frame.

#### 7.5.1.1.106 Register 8Fh (Address = 8Fh) [reset = 0h]

### Figure 134. Register 8Fh

23	22	21	20	19	18	17	16
			RESE	RVED			
			R/W	/ - 0h			
15	14	13	12	11	10	9	8
			TG_ILLUM	IEN_START			
			R/W	/ - 0h			
7	6	5	4	3	2	1	0
	TG_ILLUMEN_START						
	R/W - 0h						

### Table 136. Register 8F Field Descriptions

Bit	Field	Type	Reset	Description
23:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	TG_ILLUMEN_START	R/W	0h	Starting position of the illumination enable TG signal in the number of TG clocks (t <sub>CLK</sub> ) in a sub-frame.

### 7.5.1.1.107 Register 90h (Address = 90h) [reset = 2134h]

## Figure 135. Register 90h

23	22	21	20	19	18	17	16
			RESE	RVED			
	R/W - 0h						
15	14	13	12	11	10	9	8
			TG_ILLUI	MEN_END			
			R/W	- 21h			
7	6	5	4	3	2	1	0
	TG_ILLUMEN_END						
	R/W - 34h						



### Table 137. Register 90 Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	TG_ILLUMEN_END	R/W	2134h	Ending position of the illumination enable TG signal in the number of TG clocks ( $t_{\text{CLK}}$ ) in a sub-frame.

#### 7.5.1.1.108 Register 91h (Address = 91h) [reset = 2134h]

### Figure 136. Register 91h

23	22	21	20	19	18	17	16				
RESERVED											
R/W - 0h											
15	14	13	12	11	10	9	8				
TG_CALC_START											
			R/W	- 21h							
7	6	5	4	3	2	1	0				
	TG_CALC_START										
		R/W - 34h									

### Table 138. Register 91 Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	TG_CALC_START	R/W	2134h	Starting position of the calculation TG signal in the number of TG clocks $(t_{\text{CLK}})$ in a sub-frame.

### 7.5.1.1.109 Register 92h (Address = 92h) [reset = 2EE0h]

### Figure 137. Register 92h

23	22	21	20	19	18	17	16			
RESERVED										
R/W - 0h										
15	14	13	12	11	10	9	8			
	TG_CALC_END									
			R/W	- 2Eh						
7	6	5	4	3	2	1	0			
	TG_CALC_END									
			R/W	- E0h						

## Table 139. Register 92 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	TG_CALC_END	R/W		Ending position of the calculation TG signal in the number of TG clocks $(t_{\text{CLK}})$ in a sub-frame.

# 7.5.1.1.110 Register 93h (Address = 93h) [reset = 0h]

### Figure 138. Register 93h

23	22	21	20	19	18	17	16			
RESERVED										
	R/W - 0h									
15	15 14 13 12 11 10 9 8									



	TG_DYNPDN_START									
R/W - 0h										
7	7 6 5 4 3 2 1 0									
	TG_DYNPDN_START									
	R/W - 0h									

### Table 140. Register 93 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	TG_DYNPDN_START	R/W	0h	Starting position of the dynamic power-down TG signal in the number of TG clocks ( $t_{CLK}$ ) in a sub-frame.

### 7.5.1.1.111 Register 94h (Address = 94h) [reset = FFFFh]

## Figure 139. Register 94h

23	22	21	20	19	18	17	16			
RESERVED										
R/W - 0h										
15	14	13	12	11	10	9	8			
TG_DYNPDN_END										
			R/W	- FFh						
7	6	5	4	3	2	1	0			
TG_DYNPDN_END										
	R/W - FFh									

### **Table 141. Register 94 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	TG_DYNPDN_END	R/W	FFFFh	Ending position of the dynamic power-down TG signal in the number of TG clocks (t <sub>CLK</sub> ) in a sub-frame.

### 7.5.1.1.112 Register 97h (Address = 97h) [reset = 0h]

### Figure 140. Register 97h

23	22	21	20	19	18	17	16			
TG_SEQ_INT_MASK_END										
R/W - 0h										
15	14	13	12	11	10	9	8			
	TG_SEQ_INT_	_MASK_END			TG_SEQ_INT_I	MASK_START	ART			
	R/W	- 0h			R/W	- 0h				
7	6	5	4	3	2	1	0			
TG_SEQ_INT_MASK_START										
	R/W - 0h									

### Table 142. Register 97 Field Descriptions

Bit	Field	Туре	Reset	Description
23:12	TG_SEQ_INT_MASK_END	R/W	0h	Ending position of the sequencer interrupt TG signal mask in the number of sub-frames in a frame.
11:0	TG_SEQ_INT_MASK_STA RT	R/W		Starting position of the sequencer interrupt TG signal mask in the number of sub-frames in a frame. The TG signal exists between the START and END sub-frames.



### 7.5.1.1.113 Register 98h (Address = 98h) [reset = 0h]

### Figure 141. Register 98h

23	22	21	20	19	18	17	16			
TG_CAPTURE_MASK_END										
R/W - 0h										
15	14	13	12	11	10	9	8			
	TG_CAPTURE	_MASK_END			TG_CAPTURE_MASK_START					
	R/W	- 0h			R/W	- 0h				
7	6	5	4	3	2	1	0			
TG_CAPTURE_MASK_START										
	R/W - 0h									

### **Table 143. Register 98 Field Descriptions**

Bit	Field	Type	Reset	Description
23:12	TG_CAPTURE_MASK_EN	R/W	0h	Ending position of the internal data-capture TG signal mask in the number of sub-frames in a frame. This register should be equal to NUM_AVG_SUB_FRAMES when DIS_TG_ACONF = 1.
11:0	TG_CAPTURE_MASK_ST ART	R/W	0h	Starting position of the internal data-capture TG signal mask in the number of sub-frames in a frame. This register should be equal to NUM_AVG_SUB_FRAMES when DIS_TG_ACONF = 1. The TG signal exists between the START and END sub-frames.

### 7.5.1.1.114 Register 99h (Address = 99h) [reset = 1h]

### Figure 142. Register 99h

23	22	21	20	19	18	17	16				
	TG_OVL_WINDOW_MASK_END										
R/W - 0h											
15	14	13	12	11	10	9	8				
	TG_OVL_WINDO	DW_MASK_END	)	TG_OVL_WINDOW_MASK_START							
	R/W	- 0h			R/W	- 0h					
7	6	5	4	3	2	1	0				
	TG_OVL_WINDOW_MASK_START										
	R/W - 0h										

### Table 144. Register 99 Field Descriptions

Bit	Field	Type	Reset	Description
23:12	TG_OVL_WINDOW_MASK _END	R/W	0h	Ending position of the AFE overload observation window TG signal mask in the number of sub-frames in a frame. This register should be equal to NUM_AVG_SUB_FRAMES when DIS_TG_ACONF = 1.
11:0	TG_OVL_WINDOW_MASK _START	R/W	1h	Starting position of AFE overload observation window TG signal mask in the number of sub-frames in a frame. The TG signal exists between the START and END sub-frames. Write 0 to this register when DIS_TG_ACONF = 1 and EN_ADAPTIVE_HDR = 0, or 1 when DIS_TG_ACONF = 1 and EN_ADAPTIVE_HDR = 1.

## 7.5.1.1.115 Register 9Ch (Address = 9Ch) [reset = FFF000h]

## Figure 143. Register 9Ch

23	22	21	20	19	18	17	16			
	TG_ILLUMEN_MASK_END									
	R/W - FFh									
15	15 14 13 12 11 10 9 8									
	TG_ILLUMEN_MASK_END TG_ILLUMEN_MASK_START									



R/W - Fh					R/W	- 0h			
7 6 5 4				3	2	1	0		
	TG_ILLUMEN_MASK_START								
			R/W	′ - 0h					

### Table 145. Register 9C Field Descriptions

Bit	Field	Туре	Reset	Description
23:12	TG_ILLUMEN_MASK_END	R/W	FFFh	Ending position of the illumination-enable TG signal mask in the number of sub-frames in a frame. This register should be equal to NUM_AVG_SUB_FRAMES when DIS_TG_ACONF = 1.
11:0	TG_ILLUMEN_MASK_STA RT	R/W	0h	Starting position of the illumination-enable TG signal mask in the number of sub-frames in a frame. The TG signal exists between the START and END sub-frames.

### 7.5.1.1.116 Register 9Dh (Address = 9Dh) [reset = 0h]

### Figure 144. Register 9Dh

23	22	21	20	19	18	17	16				
	TG_CALC_MASK_END										
	R/W - 0h										
15	14	13	12	11	10	9	8				
	TG_CALC_MASK_END TG_CALC_MASK_START										
	R/W	- 0h			R/W	- 0h					
7	6	5	4	3	2	1	0				
	TG_CALC_MASK_START										
_		·	R/W	- 0h	<u>-</u>						

### Table 146. Register 9D Field Descriptions

Bit	Field	Туре	Reset	Description
23:12	TG_CALC_MASK_END	R/W	0h	Ending position of the calculation TG signal mask in the number of sub- frames in a frame. This register should be equal to NUM_AVG_SUB_FRAMES when DIS_TG_ACONF = 1.
11:0	TG_CALC_MASK_START	R/W	0h	Starting position of the calculation TG signal mask in the number of sub- frames in a frame. The TG signal exists between the START and END sub- frames. This register should be equal to NUM_AVG_SUB_FRAMES when DIS_TG_ACONF = 1.

### 7.5.1.1.117 Register 9Eh (Address = 9Eh) [reset = 0h]

## Figure 145. Register 9Eh

23	22	21	20	19	18	17	16			
TG_DYNPDN_MASK_END										
R/W - 0h										
15	14	13	12	11	10	9	8			
	TG_DYNPDN_MASK_END TG_DYNPDN_MASK_START									
	R/W	- 0h			R/W	- 0h				
7	6	5	4	3	2	1	0			
	TG_DYNPDN_MASK_START									
			R/W	- 0h						

### Table 147. Register 9E Field Descriptions

Bit	Field	Туре	Reset	Description
23:12	TG_DYNPDN_MASK_END	R/W	0h	Ending position of the dynamic power-down TG signal mask in the number of sub-frames in a frame. This register should be equal to NUM_AVG_SUB_FRAMES when DIS_TG_ACONF = 1.



### Table 147. Register 9E Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	TG_DYNPDN_MASK_STA RT	R/W		Starting position of the dynamic power-down TG signal mask in the number of sub-frames in a frame. The TG signal exists outside the TG_DYNPDN_MASK_START and TG_DYNPDN_MASK_END sub-frames.

### 7.5.1.1.118 Register 9Fh (Address = 9Fh) [reset = 0h]

### Figure 146. Register 9Fh

23	22	21	20	19	18	17	16			
	NUM_AVG_SUB_FRAMES									
	R/W - 0h									
15	14	13	12	11	10	9	8			
NUM_AVG_SUB_FRAMES NUM_SUB_FRAMES										
	R/W	- 0h			R/W	- 0h				
7	6	5	4	3	2	1	0			
	NUM_SUB_FRAMES									
			R/W	- 0h						

### Table 148. Register 9F Field Descriptions

Bit	Field	Туре	Reset	Description
23:12	NUM_AVG_SUB_FRAMES	R/W	0h	Specifies the number of sub-frames to be averaged in a frame.  Averaging sub-frames = NUM_AVG_SUB_FRAMES + 1.
11:0	NUM_SUB_FRAMES	R/W	0h	Total number of sub-frames in a frame. Each sub-frame is approximately 0.25 ms (SUB_VD_CLK_CNT × 25 ns)  Number of sub-frames in a frame = NUM_SUB_FRAMES + 1.  This number must be equal to or greater than NUM_AVG_SUB_FRAMES.

### 7.5.1.1.119 Register A0h (Address = A0h) [reset = 2198h]

### Figure 147. Register A0h

23	22	21	20	19	18	17	16				
	RESERVED										
R/W - 0h											
15	14	13	12	11	10	9	8				
			CAPTURE	_CLK_CNT							
			R/W	- 21h							
7	6	5	4	3	2	1	0				
	CAPTURE_CLK_CNT										
		R/W - 98h									

### **Table 149. Register A0 Field Descriptions**

Bit	Field	Type	Reset	Description
23:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	CAPTURE_CLK_CNT	R/W	2198h	Internal data capture position (number of TG clocks, t <sub>CLK</sub> ) in a sub-frame.

# 7.5.1.1.120 Register A2h (Address = A2h) [reset = 0h]



### Figure 148. Register A2h

23	22	21	20	19	18	17	16				
A3_COEFF_HDR0_TX1[15:8]											
R/W - 0h											
15	14	13	12	11	10	9	8				
			A0_COEFF	_HDR1_TX0							
			R/W	/ - 0h							
7	6	5	4	3	2	1	0				
	A0_COEFF_HDR1_TX0										
		R/W - 0h									

### Table 150. Register A2 Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	A3_COEFF_HDR0_TX1[15 :8]	R/W	0h	MSB of third-order coefficient for square wave nonlinearity correction for TX1 illumination channel with current of ILLUM_DAC_L_TX1.
15:0	A0_COEFF_HDR1_TX0	R/W	0h	Constant offset for square wave nonlinearity correction for TX0 illumination channel with current of ILLUM_DAC_H_TX0.

### 7.5.1.1.121 Register A3h (Address = A3h) [reset = 0h]

### Figure 149. Register A3h

23	22	21	20	19	18	17	16								
	A3_COEFF_HDR0_TX1[7:0]														
	R/W - 0h														
15	14	13	12	11	10	9	8								
	A0_COEFF_HDR0_TX1														
			R/W	/ - 0h											
7	6	5	4	3	2	1	0								
	A0_COEFF_HDR0_TX1														
			R/W	′ - 0h		R/W - 0h									

### Table 151. Register A3 Field Descriptions

Bit Field Type Reset		Reset	Description	
23:16	A3_COEFF_HDR0_TX1[7: 0]	R/W	0h	LSB of third-order coefficient for square wave nonlinearity correction for TX1 illumination channel with current of ILLUM_DAC_L_TX1.
15:0	A0_COEFF_HDR0_TX1	R/W	0h	Constant offset for square wave nonlinearity correction for TX1 illumination channel with current of ILLUM_DAC_L_TX1.

### 7.5.1.1.122 Register A4h (Address = A4h) [reset = 0h]

### Figure 150. Register A4h

23	22	21	20	19	18	17	16			
A3_COEFF_HDR1_TX1[15:8]										
	R/W - 0h									
15	14	13	12	11	10	9	8			
			A0_COEFF	_HDR1_TX1						
			R/W	' - 0h						
7	6	5	4	3	2	1	0			
	A0_COEFF_HDR1_TX1									
	·	·	R/W	' - 0h	·	·	_			



### Table 152. Register A4 Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	A3_COEFF_HDR1_TX1[15 :8]	R/W	0h	MSB of third order coefficient for square wave nonlinearity correction for TX1 illumination channel with current of ILLUM_DAC_H_TX1.
15:0	A0_COEFF_HDR1_TX1	R/W	0h	Constant offset for square wave nonlinearity correction for TX1 illumination channel with current of ILLUM_DAC_H_TX1.

#### 7.5.1.1.123 Register A5h (Address = A5h) [reset = 0h]

### Figure 151. Register A5h

23	22	21	20	19	18	17	16			
A3_COEFF_HDR1_TX1[7:0]										
	R/W - 0h									
15	14	13	12	11	10	9	8			
			A0_COEFF	_HDR0_TX2						
			R/W	/ - 0h						
7	6	5	4	3	2	1	0			
	A0_COEFF_HDR0_TX2									
	R/W - 0h									

### **Table 153. Register A5 Field Descriptions**

Bit	Field	Туре	Reset	Description
23:16	A3_COEFF_HDR1_TX1[7: 0]	R/W	0h	LSB of third-order coefficient for square wave nonlinearity correction for TX1 illumination channel with current of ILLUM_DAC_H_TX1.
15:0	A0_COEFF_HDR0_TX2	R/W	0h	Constant offset for square wave nonlinearity correction for TX2 illumination channel with current of ILLUM_DAC_L_TX2.

### 7.5.1.1.124 Register A6h (Address = A6h) [reset = 0h]

### Figure 152. Register A6h

23	22	21	20	19	18	17	16			
A3_COEFF_HDR0_TX2[15:8]										
	R/W - 0h									
15	14	13	12	11	10	9	8			
			A0_COEFF	_HDR1_TX2						
			R/W	′ - 0h						
7	6	5	4	3	2	1	0			
	A0_COEFF_HDR1_TX2									
	R/W - 0h									

### Table 154. Register A6 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A3_COEFF_HDR0_TX2[15 :8]	R/W	0h	MSB of third-order coefficient for square wave nonlinearity correction for TX2 illumination channel with current of ILLUM_DAC_L_TX2.
15:0	A0_COEFF_HDR1_TX2	_TX2 R/W 0h		Constant offset for square wave nonlinearity correction for TX2 illumination channel with current of ILLUM_DAC_H_TX2.

# 7.5.1.1.125 Register A7h (Address = A7h) [reset = 0h]



### Figure 153. Register A7h

23	22	21	20	19	18	17	16			
A3_COEFF_HDR0_TX2[7:0]										
R/W - 0h										
15	14	13	12	11	10	9	8			
	A1_COEFF_HDR1_TX0									
			R/W	/ - 0h						
7	6	5	4	3	2	1	0			
	A1_COEFF_HDR1_TX0									
	R/W - 0h									

### **Table 155. Register A7 Field Descriptions**

Bit	it Field Type Reset		Reset	Description		
23:16	A3_COEFF_HDR0_TX2[7: 0]	R/W	0h	LSB of third-order coefficient for square wave nonlinearity correction for TX2 illumination channel with current of ILLUM_DAC_L_TX2.		
15:0	A1_COEFF_HDR1_TX0	R/W	0h	First-order coefficient for square wave nonlinearity correction for TX0 illumination channel with current of ILLUM_DAC_H_TX0.		

### 7.5.1.1.126 Register A8h (Address = A8h) [reset = 0h]

### Figure 154. Register A8h

23	22	21	20	19	18	17	16				
	A3_COEFF_HDR1_TX2[15:8]										
R/W - 0h											
15	14	13	12	11	10	9	8				
A1_COEFF_HDR0_TX1											
			R/W	/ - 0h							
7	6	5	4	3	2	1	0				
	A1_COEFF_HDR0_TX1										
		R/W - 0h									

### Table 156. Register A8 Field Descriptions

Bit Field		Туре	Reset	Description		
23:16	:16 A3_COEFF_HDR1_TX2[15 R/W 0h		0h	MSB of third-order coefficient for square wave nonlinearity correction for TX2 illumination channel with current of ILLUM_DAC_H_TX2.		
15:0	A1_COEFF_HDR0_TX1	DEFF_HDR0_TX1 R/W 0h		First-order coefficient for square wave nonlinearity correction for TX1 illumination channel with current of ILLUM_DAC_L_TX1.		

### 7.5.1.1.127 Register A9h (Address = A9h) [reset = 0h]

### Figure 155. Register A9h

23	22	21	20	19	18	17	16			
A3_COEFF_HDR1_TX2[7:0]										
R/W - 0h										
15	14	13	12	11	10	9	8			
	A1_COEFF_HDR1_TX1									
			R/W	/ - 0h						
7	6	5	4	3	2	1	0			
	A1_COEFF_HDR1_TX1									
			R/W	/ - 0h						



### Table 157. Register A9 Field Descriptions

Bit	Field	Type	Reset	Description		
23:16	A3_COEFF_HDR1_TX2[7: R/W 0h		0h	LSB of third-order coefficient for square wave nonlinearity correction for TX2 illumination channel with current of ILLUM_DAC_H_TX2.		
15:0	A1_COEFF_HDR1_TX1	R/W 0h		First-order coefficient for square wave nonlinearity correction for TX1 illumination channel with current of ILLUM_DAC_H_TX1.		

#### 7.5.1.1.128 Register AAh (Address = AAh) [reset = 0h]

### Figure 156. Register AAh

23	22	21	20	19	18	17	16			
A4_COEFF_HDR1_TX0[15:8]										
R/W - 0h										
15	14	13	12	11	10	9	8			
A1_COEFF_HDR0_TX2										
			R/W	/ - 0h						
7	6	5	4	3	2	1	0			
	A1_COEFF_HDR0_TX2									
	R/W - 0h									

### Table 158. Register AA Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	A4_COEFF_HDR1_TX0[15 :8]	R/W	0h	MSB of fourth-order coefficient for square wave nonlinearity correction for TX0 illumination channel with current of ILLUM_DAC_H_TX0.
15:0	A1_COEFF_HDR0_TX2	R/W	0h	First-order coefficient for square wave nonlinearity correction for TX2 illumination channel with current of ILLUM_DAC_L_TX2.

### 7.5.1.1.129 Register ABh (Address = ABh) [reset = 0h]

### Figure 157. Register ABh

23	22	21	20	19	18	17	16			
A4_COEFF_HDR1_TX0[7:0]										
	R/W - 0h									
15	14	13	12	11	10	9	8			
	A1_COEFF_HDR1_TX2									
			R/W	/ - 0h						
7	6	5	4	3	2	1	0			
	A1_COEFF_HDR1_TX2									
	R/W - 0h									

### Table 159. Register AB Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A4_COEFF_HDR1_TX0[7: 0]	R/W		LSB of fourth-order coefficient for square wave nonlinearity correction for TX0 illumination channel with current of ILLUM_DAC_H_TX0.
15:0	A1_COEFF_HDR1_TX2	HDR1_TX2 R/W 0h		First-order coefficient for square wave nonlinearity correction for TX2 illumination channel with current of ILLUM_DAC_H_TX2.

# 7.5.1.1.130 Register ACh (Address = ACh) [reset = 0h]



### Figure 158. Register ACh

23	22	21	20	19	18	17	16			
A4_COEFF_HDR0_TX1[15:8]										
R/W - 0h										
15	14	13	12	11	10	9	8			
	A2_COEFF_HDR1_TX0									
			R/W	/ - 0h						
7	6	5	4	3	2	1	0			
	A2_COEFF_HDR1_TX0									
	R/W - 0h									

### Table 160. Register AC Field Descriptions

Bit Field Type		Reset	Description	
23:16	A4_COEFF_HDR0_TX1[15 :8]	R/W	0h	MSB of fourth-order coefficient for square wave nonlinearity correction for TX1 illumination channel with current of ILLUM_DAC_L_TX1.
15:0	A2_COEFF_HDR1_TX0	R/W	0h	Second-order coefficient for square wave nonlinearity correction for TX0 illumination channel with current of ILLUM_DAC_H_TX0.

### 7.5.1.1.131 Register ADh (Address = ADh) [reset = 0h]

### Figure 159. Register ADh

23	22	21	20	19	18	17	16				
	A4_COEFF_HDR0_TX1[7:0]										
R/W - 0h											
15	14	13	12	11	10	9	8				
	A2_COEFF_HDR0_TX1										
			R/W	/ - 0h							
7	6	5	4	3	2	1	0				
	A2_COEFF_HDR0_TX1										
	R/W - 0h										

### Table 161. Register AD Field Descriptions

Bit Field		Туре	Reset	Description		
23:16	A4_COEFF_HDR0_TX1[7: 0]	R/W	0h	LSB of fourth-order coefficient for square wave nonlinearity correction for TX1 illumination channel with current of ILLUM_DAC_L_TX1.		
15:0	A2_COEFF_HDR0_TX1	R/W	0h	Second-order coefficient for square wave nonlinearity correction for TX1 illumination channel with current of ILLUM_DAC_L_TX1.		

### 7.5.1.1.132 Register AEh (Address = AEh) [reset = 0h]

## Figure 160. Register AEh

23	22	21	20	19	18	17	16			
A4_COEFF_HDR1_TX1[15:8]										
R/W - 0h										
15	14	13	12	11	10	9	8			
	A2_COEFF_HDR1_TX1									
			R/W	/ - 0h						
7	6	5	4	3	2	1	0			
	A2_COEFF_HDR1_TX1									
			R/W	/ - 0h						



### Table 162. Register AE Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	A4_COEFF_HDR1_TX1[15 :8]	R/W	0h	MSB of fourth-order coefficient for square wave nonlinearity correction for TX1 illumination channel with current of ILLUM_DAC_H_TX1.
15:0	A2_COEFF_HDR1_TX1	R/W	0h	Second-order coefficient for square wave nonlinearity correction for TX1 illumination channel with current of ILLUM_DAC_H_TX1.

#### 7.5.1.1.133 Register AFh (Address = AFh) [reset = 0h]

### Figure 161. Register AFh

23	22	21	20	19	18	17	16			
A4_COEFF_HDR1_TX1[7:0]										
R/W - 0h										
15	14	13	12	11	10	9	8			
	A2_COEFF_HDR0_TX2									
			R/W	/ - 0h						
7	6	5	4	3	2	1	0			
	A2_COEFF_HDR0_TX2									
	R/W - 0h									

### Table 163. Register AF Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A4_COEFF_HDR1_TX1[7: 0]	R/W	0h	LSB of fourth-order coefficient for square wave nonlinearity correction for TX1 illumination channel with current of ILLUM_DAC_H_TX1.
15:0	A2_COEFF_HDR0_TX2	R/W	0h	Second-order coefficient for square wave nonlinearity correction for TX2 illumination channel with current of ILLUM_DAC_L_TX2.

### 7.5.1.1.134 Register B0h (Address = B0h) [reset = 0h]

### Figure 162. Register B0h

23	22	21	20	19	18	17	16			
A4_COEFF_HDR0_TX2[15:8]										
R/W - 0h										
15 14 13 12 11 10 9 8										
	A2_COEFF_HDR1_TX2									
			R/W	' - 0h						
7	6	5	4	3	2	1	0			
	A2_COEFF_HDR1_TX2									
			R/W	′ - 0h						

### Table 164. Register B0 Field Descriptions

Bit	Field	Type	Reset	Description		
23:16	A4_COEFF_HDR0_TX2[15 :8]	[15 R/W 0h		MSB of fourth-order coefficient for square wave nonlinearity correction for TX2 illumination channel with current of ILLUM_DAC_L_TX2.		
15:0	A2_COEFF_HDR1_TX2	R/W	0h	Second-order coefficient for square wave nonlinearity correction for TX2 illumination channel with current of ILLUM_DAC_H_TX2.		

# 7.5.1.1.135 Register B1h (Address = B1h) [reset = 0h]



### Figure 163. Register B1h

23	22	21	20	19	18	17	16			
A4_COEFF_HDR0_TX2[7:0]										
R/W - 0h										
15 14 13 12 11 10 9 8										
	A3_COEFF_HDR1_TX0									
			R/W	/ - 0h						
7	6	5	4	3	2	1	0			
	A3_COEFF_HDR1_TX0									
			R/W	/ - 0h						

### Table 165. Register B1 Field Descriptions

Bit	Field	eld Type Reset		Description		
23:16	A4_COEFF_HDR0_TX2[7: R/W 0h			LSB byte of fourtt-order coefficient for square wave nonlinearity correction for TX2 illumination channel with current of ILLUM_DAC_L_TX2.		
15:0	A3_COEFF_HDR1_TX0	R/W	0h	Third-order coefficient for square wave nonlinearity correction for TX0 illumination channel with current of ILLUM_DAC_H_TX0.		

### 7.5.1.1.136 Register B2h (Address = B2h) [reset = 0h]

### Figure 164. Register B2h

23	22	21	20	19	18	17	16			
RESERVED										
R/W - 0h										
15	14	13	12	11	10	9	8			
	A4_COEFF_HDR1_TX2									
			R/W	/ - 0h						
7	6	5	4	3	2	1	0			
	A4_COEFF_HDR1_TX2									
	R/W - 0h									

### Table 166. Register B2 Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	RESERVED	R/W	0h	Always read or write 0h.
15:0	A4_COEFF_HDR1_TX2	R/W	0h	Fourth-order coefficient for square wave nonlinearity correction for TX2 illumination channel with current of ILLUM_DAC_H_TX2.

## 7.5.1.1.137 Register B4h (Address = B4h) [reset = 0h]

### Figure 165. Register B4h

23	22	21	20	19	18	17	16			
	AMB_PHASE_CORR_PWL_COEFF3									
R/W - 0h										
15	14	13	12	11	10	9	8			
			AMB_PHASE_CO	RR_PWL_COEFF	2					
	R/W - 0h									
7	6	5	4	3	2	1	0			
AMB_PHASE_CORR_PWL_COEFF1										
	R/W - 0h									



### Table 167. Register B4 Field Descriptions

Bit	Field	Туре	Reset	Description
23:16	AMB_PHASE_CORR_PWL _COEFF3	R/W	0h	Coefficient 3 for PWL phase correction with ambient.
15:8	AMB_PHASE_CORR_PWL _COEFF2	R/W	0h	Coefficient 2 for PWL phase correction with ambient.
7:0	AMB_PHASE_CORR_PWL _COEFF1	R/W	0h	Coefficient 1 for PWL phase correction with ambient.

### 7.5.1.1.138 Register B5h (Address = B5h) [reset = 0h]

### Figure 166. Register B5h

23	22	21	20	19	18	17	16		
			RESE	RVED					
	R/W - 0h								
15	14	13	12	11	10	9	8		
			RESE	RVED					
			R/W	′ - 0h					
7	6	5	4	3	2	1	0		
		RESERVED	SCALE_AN	//B_PHASE_COF	RR_COEFF				
		R/W - 0h		R/W - 0h					

### Table 168. Register B5 Field Descriptions

Bit	Field	Туре	Reset	Description
23:3	RESERVED	R/W	0h	Always read or write 0h.
2:0	SCALE_AMB_PHASE_CO RR_COEFF	R/W	0h	Scaling factor for ambient-based PWL phase correction.

### 7.5.1.1.139 Register B8h (Address = B8h) [reset = 7FDFFh]

### Figure 167. Register B8h

23	22	21	20	19	18	17	16		
	RESERVED GIVE_DEAL_D ATA				AMB_PHASE_CORR_PWL_X1				
	R/W - 0h		R/W - 0h		R/W	- 7h			
15	14	13	12	11	10	9	8		
		AMB_PHASE_0	CORR_PWL_X1			AMB_PHASE_C	CORR_PWL_X0		
		R/W	- 3Fh			R/W	- 1h		
7	6	5	4	3	2	1	0		
	AMB_PHASE_CORR_PWL_X0								
	R/W - FFh								

## Table 169. Register B8 Field Descriptions

Bit	Field	Type	Reset	et Description	
23:21	RESERVED	R/W	0h Always read or write 0h.		
20	GIVE_DEALIAS_DATA	R/W	0h	When this register is set to 1, de-aliased phase is given out on PHASE_OUT.	
19:10	AMB_PHASE_CORR_PWL _X1	R/W	1FFh	Second knee point of PWL phase correction with ambient.	
9:0	AMB_PHASE_CORR_PWL _X0	R/W	1FFh	First knee point of PWL phase correction with ambient.	



### 7.5.1.1.140 Register B8h (Address = B9h) [reset = 1FFh]

# Figure 168. Register B9h

23	22	21	20	19	18	17	16		
	ILLUM_SCALE_H_T	X2	IL	LUM_SCALE_L_T	X2	AMB_ADC_IN_TX2			
	R/W - 0h			R/W - 0h	R/W	/ - 0h			
15	14	13	12	11	10	9	8		
AN	AMB_ADC_IN_TX1 AMB_AD0			EN_TX2_ON_T X0	EN_TX1_ON_T X0	AMB_PHASE_0	CORR_PWL_X2		
	R/W - 0h R/W			/ - 0h R/W - 0h R/W - 0h			R/W - 1h		
7	6	5	4	3	2	1	0		
	AMB_PHASE_CORR_PWL_X2								
	R/W - FFh								

## Table 170. Register B9 Field Descriptions

Bit	Field	Туре	Reset	Description
23:21	ILLUM_SCALE_H_TX2	R/W	0h	Current-scaling register for the illumination driver TX2 channel with DAC_H current. 0: 5.6 mA   1: 4.2 mA   2: 2.8 mA   3: 1.4 mA   Other values: Not valid
20:18	ILLUM_SCALE_L_TX2	R/W	0h	Current scaling register for the illumination driver TX2 channel with DAC_L current.  0: 5.6 mA   1: 4.2 mA   2: 2.8 mA   3: 1.4 mA   Other values: Not valid
17:16	AMB_ADC_IN_TX2	R/W	0h	Select ambient ADC input when TX2 channel is selected. 0: DACP - DACM   1: DACP - REFP   2: DACM - DACP   3: DACM - REFM
15:14	AMB_ADC_IN_TX1	R/W	0h	Select ambient ADC input when TX1 channel is selected. 0: DACP - DACM   1: DACP - REFP   2: DACM - DACP   3: DACM - REFM
13:12	AMB_ADC_IN_TX0	R/W	0h	Select ambient ADC input when TX0 channel is selected. 0: DACP - DACM   1: DACP - REFP   2: DACM - DACP   3: DACM - REFM
11	EN_TX2_ON_TX0	R/W	0h	If this bit is 1 when TX2 is selected, the illumination driver current flows through TX0.
10	EN_TX1_ON_TX0	R/W	0h	If this bit is 1 when TX1 is selected, the illumination driver current flows through TX0.
9:0	AMB_PHASE_CORR_PWL _X2	R/W	1FFh	Third knee point of PWL phase correction with ambient



## 8 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

#### 8.1 Application Information

The OPT3101 AFE is a fully integrated analog front end with an integrated illumination driver for measuring distance. The device interfaces an external photodiode and LED, VCSEL, or LASER. The device has an I<sup>2</sup>C interface for the data output. An external MCU can read out the distance data from the device directly and no computation is required on the external MCU. All the computation and corrections for crosstalk, phase offset, temperature-dependent phase drift, and ambient-dependent phase drift are done on the chip. The device also provides temperature output from the on-chip temperature sensor. It can operate up to a speed of 4000 sps in non-HDR mode and 2000 sps in auto HDR mode.

#### 8.2 Typical Application

Obstacle avoidance for autonomous vehicle navigation is a typical application which can be implemented using this AFE. The system can be optimized to meet the application requirements by optimizing various parameters like illumination current, sub-frame averaging, and auto HDR mode, which are explained in the following sections. Figure 169 shows the interface between the OPT3101 device and an external MCU.

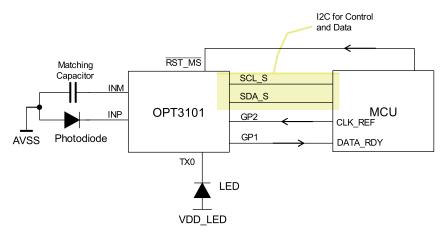


Figure 169. Typical Application Block Diagram

#### 8.2.1 Design Requirements

Table 171 lists the application requirements for obstacle avoidance system.

**Table 171. Application Specifications** 

SPECIFICATION	VALUE	UNITS	COMMENTS
Minimum distance	0.3	m	
Maximum distance	5	m	
Distance accuracy	2	%	For an object with 18% reflectivity.
Ambient light	130	klx	Sunlight condition
Field of view	±3	degrees	
Wavelength	850	nm	Infrared wavelength for illumination.
Sample rate	30	sps	
Supply	3.3	V	Single supply for the system



#### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Sample Rate

The sample rate can be adjusted by programming the number of sub-frames in a frame. To meet the application requirement of 30 sps, 128 sub-frame averaging can be used from Equation 1. Set the register NUM SUB FRAME = 127 and NUM AVG SUB FRAMES = 127, which gives a sample rate of 31.25 sps.

#### 8.2.2.2 Photodiode and LED

OSRAM SFH4550 LED meets the required field of view specification and has peak spectral emission at 860 nm. Even though LED is specified for a half-angle of ±3 degrees, a significant amount of the optical power will be outside the half-angle. Figure 170 shows the radiation characteristics of the LED. The photodiode should have a field of view greater than the field of view of the LED to effectively collect all the optical power emitted from the LED and reflected by the object. The photodiode should also have peak sensitivity matching the peak spectral emission of the LED. Most of the photodiodes come in two variants;

- With a daylight filter, which has a very broad spectrum; example: SFH213
- Narrow-band IR spectrum; example: SFH213FA.

A photiode with a narrow-band IR filter should be selected as it collects a lower ambient signal. Photodiode SFH213FA meets these requirements. This photodiode has a capacitance of 5.8 pF at 1-V reverse bias, which is within the supported capacitance range of the AFE. Photodiode characterisits are shown in Figure 171 and Figure 172

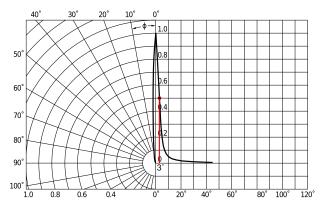
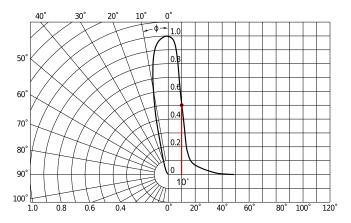
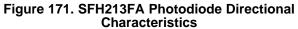


Figure 170. SFH4550 LED Radiation Characteristics





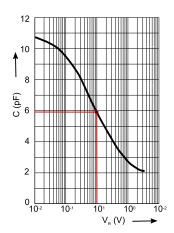


Figure 172. SFH213FA Photodiode Reverse Bias Capacitance



#### 8.2.2.3 Ambient Support

The photodiode has an IR filter centered at 900 nm as shown in Figure 173. The sunlight spectral irradiance within the spectral bandwidth of the photodiode is also shown in the same figure. The total sunlight power with in the spectral bandwidth of photodiode is 176 watts/ $m^2$ . The ambient sunlight power received by the photodiode can be calculated using Equation 9. Total ambient current for this photodiode is 49.2  $\mu$ A. Accounting for variations in reflectivity, the IAMB\_MAX\_SEL = 12 setting should be selected, which corresponds to 100- $\mu$ A ambient current support.

$$P_{r,amb}\!=\!P_{AMB}\times A_{scene}\times \frac{\Omega_{lens}}{\Omega_{semi-sphere}} \;\; in\; Watts$$

#### where

- P<sub>AMB</sub> = Total ambient light power in the photodiode spectral bandwidth in W/m<sup>2</sup>
- A<sub>scene</sub> = Area covered by photodiode FoV
- $\Omega_{lens}$  = Solid angle from a point on target object to the photodiode lens

• 
$$\Omega_{\text{semi-sphere}} = 2\pi$$
 (9)  
 $P_{\text{r,amb}} \sim \frac{P_{\text{AMB}} \times \left[ \tan(\phi_{\text{PD}}) \right]^2}{2}$  in Watts/m<sup>2</sup>

where

• 
$$\varphi_{PD}$$
 = Photodiode half-angle = 10° for SFH213FA (10)

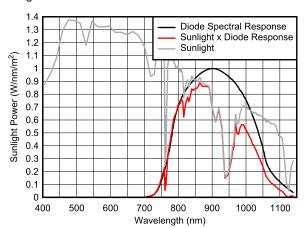


Figure 173. SFH213FA Photodiode Spectral Response and Sunlight Power Within Photodiode Spectral Bandwidth

#### Table 172. Photodiode Specifications

PARAMETER	VALUE	UNIT	COMMENTS
Photodiode current with 1 mW/cm <sup>2</sup>	90	μA	Photodiode specification
Half-angle	±10	Degrees	Photodiode specification
Total sunlight power in photodiode spectral bandwidth falling on the object	175	W/m <sup>2</sup>	Calculated from sunlight spectra (see Figure 173)
Total power received at the photodiode	0.2736	mW/cm <sup>2</sup>	Calculated using Equation 10
Ambient current	49.2	μА	Calculated from 0.2736 mW/cm <sup>2</sup> × 90 µA/ (1 mW/cm <sup>2</sup> ). An additional factor of 2 should be added to account for the photodiode response outside the specified half angle of ±10 degrees.
Reverse bias capacitance at $V_R = 1 \text{ V}$	5.8	pF	AFE supports a maximum capacitance of 6 pF.



#### 8.2.2.4 Distance Accuracy

For 30 sps operation, 128 sub-frames can be averaged to improve the noise performance by setting NUM\_SUB\_FRAMES = 127 and NUM\_AVG\_SUB\_FRAMES = 127. AFE noise with a 6-pF photodiode capacitance and 100- $\mu$ A ambient current support can be extracted from Figure 2 as 2.25 pA/ $\sqrt{Hz}$ . Total noise at 31.25 sps operation with the above settings is 12.6 pA. The minimum SNR required to meet the distance accuracy of 2%, (10 cm at 5 m) can be calculated using Equation 6 as 23.8. So the minimum signal current required is 12.6 pA × 23.8 = 300 pA. The photodiode current required to get a signal current of 300pA can be calculated from Equation 11 as 720 pA. With a diode responsivity of 0.5 A/W, the optical power required is 720 pA / (0.5 A/W) = 1.44 nW. Illumination power required with an 18% reflective target can be calculated from Equation 12 as 64 mW. The SFH4550 produces 70 mW of optical power for a current of 100 mA. From this, the required illumination current can be calculated as 91.5 mA

$$I_{SIG\_AFE} = \frac{I_{PD}}{2} \times \frac{30}{(30 + C_{PD})}$$

where

- I<sub>PD</sub> = Photodiode signal current.
- I<sub>SIG AFE</sub> = Signal current entering the AFE.

• 
$$C_{PD}$$
 = Photodiode capacitance at a reverse bias voltage of 1 V (11)

$$P_{r,sig} = P_{LED} \times \frac{\Omega_{lens}}{\Omega_{semi-sphere}} \times R \text{ in Watts}$$

where

- P<sub>r,sig</sub> = Signal power received by the photodiode
- P<sub>LED</sub> = LED output power
- R = Object reflectivity
- $\Omega_{lens}$  = Solid angle from a point on a target object to the photodiode lens

• 
$$\Omega_{\text{semi-sphere}} = 2\pi$$
 (12)

$$\Omega_{\text{lens}} = 4\pi \sin^2 \left( \frac{1}{2} \tan^{-1} \left( \frac{D_{\text{lens}}}{2d} \right) \right) \sim \pi \frac{D_{\text{lens}}^2}{4d^2}$$

where

• D<sub>lens</sub> = Diameter of the lens over the photodiode = 5 mm for SFH213FA

Choose 100 mA as the illumination current for meeting the SNR requirement for the 18% reflective target at a 5-m distance. With this illumination current, a 90% reflective object gives a signal current of 1.5 nA for an object at 5 m, and the AFE saturates for an object at a distance of 5 m /  $\sqrt{(200 \text{ nA} / 1.5 \text{nA})} = 0.43$  m. Because the required minimum distance is lower than this, on-chip adaptive HDR should be used by setting ENABLE\_ADAPTIVE\_HDR = 1, ILLUM\_DAC\_L\_TX0 = 2 and ILLUM\_DAC\_H\_TX0 = 20. HDR switching thresholds can be set at HDR\_THR\_HIGH = 27 000 and HDR\_THR\_LOW = 27 000 / 10 / 1.2 = 2250.

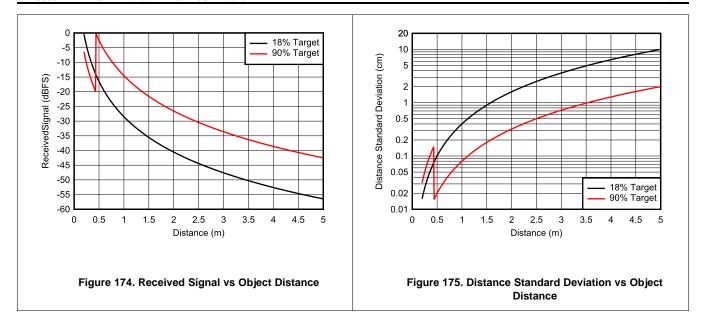
#### 8.2.2.5 Supply Voltage

Because the system must operate with a single supply, the OPT3101 device can be used in LDO mode, where the required 1.8-V supplies AVDD and DVDD are generated by the device itself using an internal LDO. To operate in this mode, connect the REG\_MODE pin to the IOVDD supply (3.3 V).

#### 8.2.3 Application Curves

Figure 174 and Figure 175 shows simulated received signal and distance standard deviation with object distance





### 8.3 Initialization Set Up

After device power up, apply device reset by applying an active-low pulse of duration  $> 30 \mu s$ .

Write the following registers to set the device running in required condition.

- Write the NUM\_SUB\_FRAMES and NUM\_AVG\_SUB\_FRAMES registers to set the device to operate at the required sample rate.
- Select the maximum ambient current to be supported by writing IAMB\_MAX\_SEL.
- Enable adaptive HDR mode if required: EN ADAPTIVE HDR.
- Write illumination DAC currents ILLUM\_DAC\_L\_TX0 and ILLUM\_DAC\_H\_TX0.
- Program the adaptive HDR thresholds: HDR THR LOW and HDR THR HIGH.
- Load all the calibration settings: illumination crosstalk, phase offset, phase temperature coefficient, and phase ambient coefficient.
- Enable frequency calibration if an external reference CLK is connected to GP2: EN\_AUTO\_FREQ\_COUNT = 1, EN\_FLOOP = 1, EN\_FREQ\_CORR = 1, SYS\_CLK\_DIVIDER = round(log<sub>2</sub>(40×10<sup>6</sup> /  $f_{EXT}$ )), REF\_COUNT\_LIMIT =  $2^{14}$  × (40×10<sup>6</sup> /  $2^{SYS_CLK_DIV}$ ) /  $f_{EXT}$ , EN\_CONT\_FCALIB = 1
- Enable on-chip temperature conversion: EN\_TEMP\_CONV = 1
- Write I<sup>2</sup>C host settings to read the external temperature sensor if it is present in the system. Register settings are listed in Table 26.
- Enable the timing generator by setting TG\_EN = 1
- Perform internal crosstalk correction by making INT\_XTALK\_CALIB = 1, followed by INT\_XTALK\_CALIB = 0.



### 9 Power Supply Recommendations

The OPT3101 device requires 1.8-V and 3.3-V supplies. There are two 1.8-V supplies (AVDD and DVDD) and two 3.3-V supplies (AVDD3 and IOVDD). AVDD and AVDD3 are analog supplies, DVDD and IOVDD are digital and I/O supplies. VDD\_LED is not a device pin, but the supply connecting to the anode of the LED (Illumination source). The inimum voltage of the VDD\_LED supply is 0.7 V ( $V_{DRV}$ ) + forward voltage drop of the LED at the maximum illumination driver current (1.8-V typical for 850-nm LED with 100 mA) + IR drop across the series elements (beads, PCB routing) in the supply (VDD\_LED) – ground (VSSL) path. The transmitter and receiver of the OPT3101 device operate at the same modulation frequency (10 MHz). Any coupling from the transmitter switching to the AFE results in a crosstalk signal which affects the performance of the distance measurement. Achieving the lowest possible crosstalk is critical for an accurate distance measurement system. Care should be taken to isolate all analog and switching supplies. VDD\_LED has the highest switching current at the modulation frequency,  $f_{MOD}$ . DVDD and IOVDD also have switching current at the modulation frequency,  $f_{MOD}$ , but much lower than VDD\_LED. Use ferrite beads with the highest impedance at 10 MHz (> 500  $\Omega$ ) in the series path of the supplies and decoupling capacitors with low impedance at  $f_{MOD}$  on the supplies very close to the device.

#### 9.1 System With Off-Chip 1.8-V Regulator

Figure 176 shows the supply network with 1.8 V generated using an off-chip regulator. The REG\_MODE pin of the OPT3101 device should be connected to IOVSS in this mode. One external regulator can be used to generate the 1.8-V supply and use beads to isolate AVDD and DVDD. The external regulator mode is useful only when the on-chip regulator mode cannot meet the power-down-state current requirement. For example, in systems where the sample rate is very low that are kept in the power-down state most of the time.

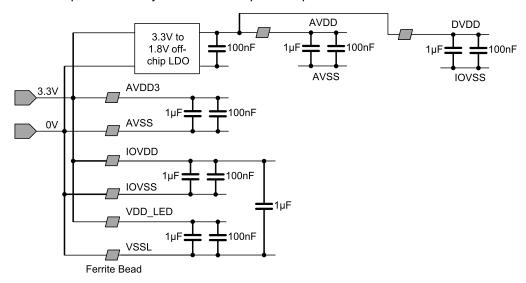


Figure 176. Power Supply Network in a System With External 1.8-V Regulator

#### 9.2 System With On-Chip 1.8-V Regulator

Figure 177 shows the supply network with 1.8 V generated using the on-chip regulators. There are two regulators, one each for AVDD and DVDD, with the input supply as AVDD3. Only decoupling capacitors need to be placed on AVDD and DVDD supplies. All other supplies should have beads in the series path. The REG\_MODE pin of the OPT3101 device should be connected to IOVDD in this mode.



### System With On-Chip 1.8-V Regulator (continued)

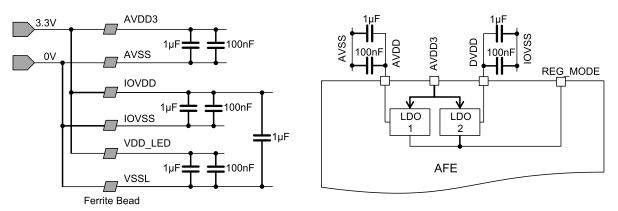


Figure 177. Power Supply Network With On-Chip 1.8-V Regulator

## 10 Layout

#### 10.1 Layout Guidelines

Reducing coupling between transmitter and receiver is very critical to achieve good system performance. The area of the transmitter current-carrying loop through the LED supply decoupling capacitor, LED, and the AFE pins TX\* and VSSL should be minimized. Similarly, the receiver loop involving the photodiode, matching capacitor, and the AFE pins INP and INM should be minimized. Figure 178 shows the transmitter and receiver loops.

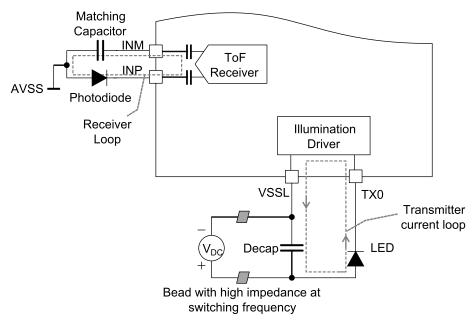


Figure 178. AFE Interface With Photodiode and LED

#### 10.2 Layout Example

Layout of a system involving a 5-mm radial through-hole photodiode and LED is shown in Figure 179. The following guidelines should be followed to keep the crosstalk between transmitter and receiver low.

- Use a four-layer board, so that all the analog and digital supplies can be well isolated from each other.
- Place the photodiode and LED oriented orthogonal to each other.



## **Layout Example (continued)**

- Minimize the area of the transmitter current-carrying loop involving LED, VDD\_LED-to-VSSL decoupling capacitor, and AFE.
- Minimize the area of the receiver loop involving the photodiode, matching capacitor, and AFE.
- Shield the receiver loop using AVSS ground in the top and bottom PCB layers. Also place a shielding ring around the photodiode and connect the shielding ring to AVSS. This shielding ring helps in reducing the electrical and optical crosstalk.
- Shield the transmitter loop using IOVSS ground in all the PCB layers. Also place a shielding ring around the LED and connect the shielding ring to IOVSS.
- LED terminals should not see the photodiode terminals directly. Any small amount of capacitive coupling between photodiode and LED terminals results in huge crosstalk. Grounded metal rings around photodiode and LED help in shielding.
- Use vias around the transmitter and receiver loops in their respective ground planes to improve the shielding.
- Connect the device thermal pad to AVSS.
- Do not overlap different ground planes, keep them well isolated.

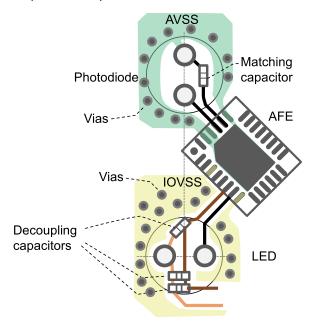


Figure 179. PCB Layout example

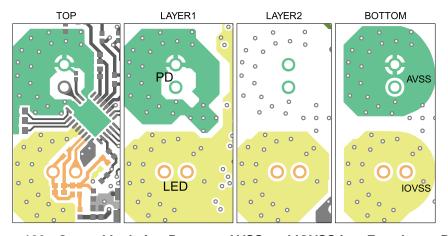


Figure 180. Ground Isolation Between AVSS and IOVSS in a Four-Layer PCB

Product Folder Links: OPT3101



# **Layout Example (continued)**

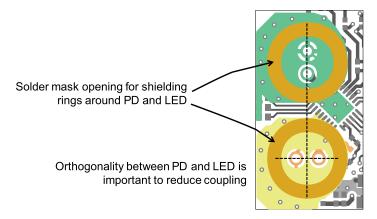


Figure 181. Photodiode and LED Placement on PCB

Submit Documentation Feedback

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## 11 Device and Documentation Support

## 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- OPT3101 Distance Sensor System Calibration
- Introduction to Time-of-Flight Optical Proximity Sensor System Design
- OPT3101 Evaluation Module User's Guide

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 11.4 Trademarks

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#### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.6 Glossary

SLYZ022 — TI Glossarv.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

Product Folder Links: OPT3101

www.ti.com 10-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
OPT3101RHFR	Active	Production	VQFN (RHF)   28	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPT 3101
OPT3101RHFR.A	Active	Production	VQFN (RHF)   28	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPT 3101
OPT3101RHFRG4	Active	Production	VQFN (RHF)   28	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPT 3101
OPT3101RHFRG4.A	Active	Production	VQFN (RHF)   28	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPT 3101
OPT3101RHFT	Obsolete	Production	VQFN (RHF)   28	-	-	Call TI	Call TI	-40 to 85	OPT 3101

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

# **PACKAGE OPTION ADDENDUM**

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

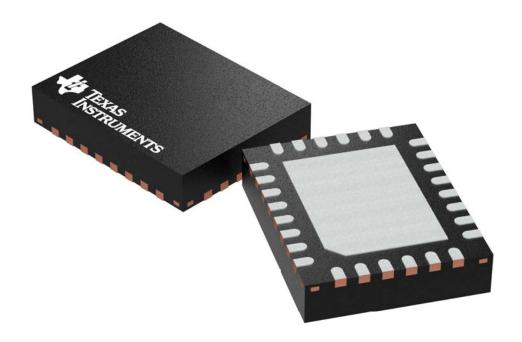
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPT3101RHFR	VQFN	RHF	28	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
OPT3101RHFRG4	VQFN	RHF	28	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

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### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPT3101RHFR	VQFN	RHF	28	3000	367.0	367.0	35.0
OPT3101RHFRG4	VQFN	RHF	28	3000	367.0	367.0	35.0



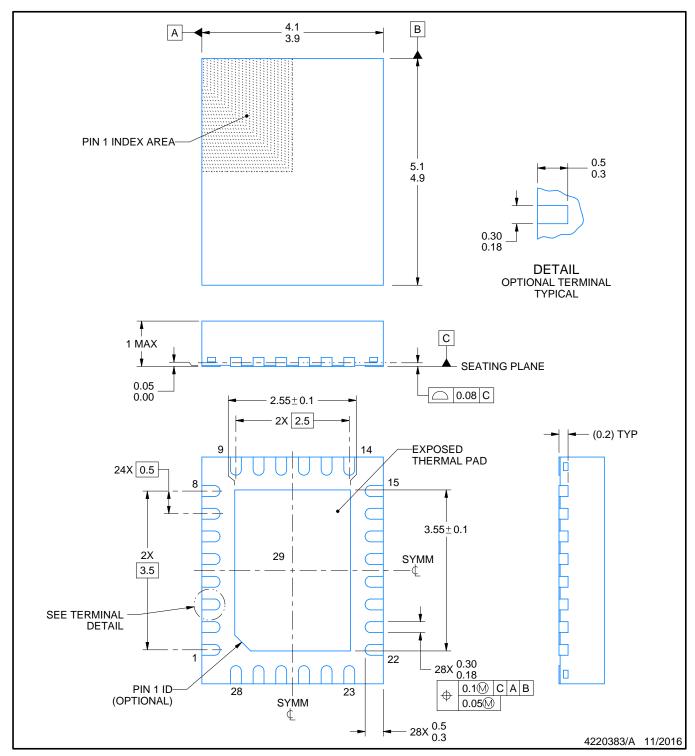
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4204845/J





PLASTIC QUAD FLATPACK - NO LEAD



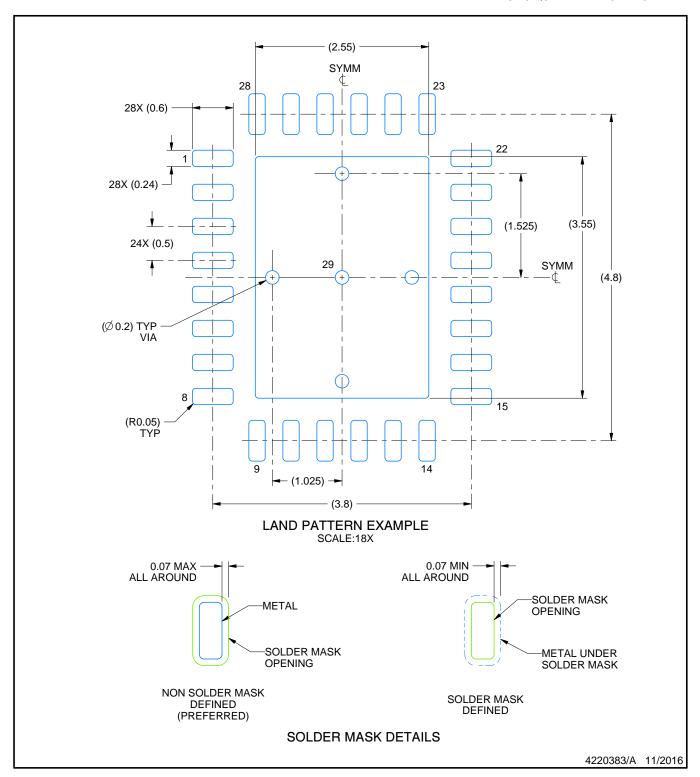
### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD

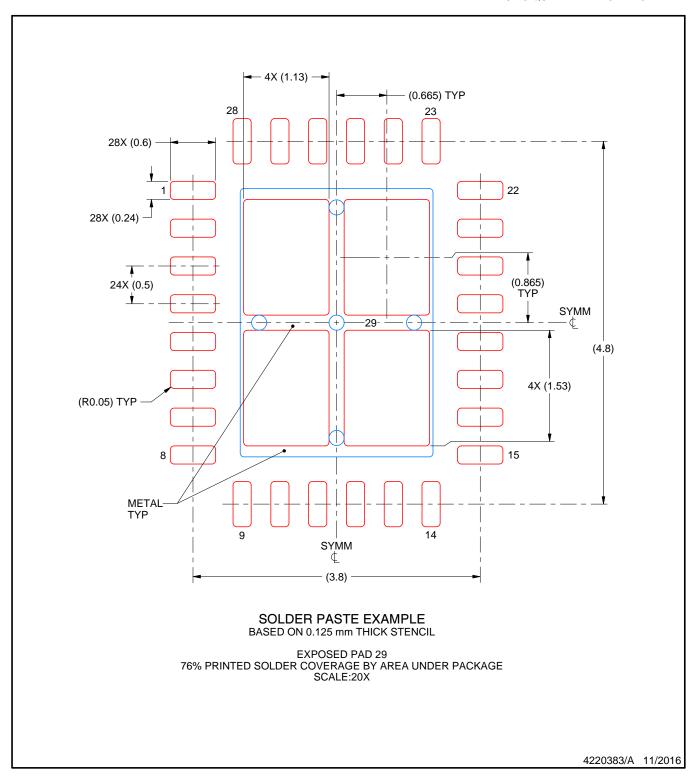


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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