











SBOS630D - DECEMBER 2013-REVISED AUGUST 2016

**OPA857** 

# OPA857 Ultralow-Noise, Wideband, Selectable-Feedback Resistance Transimpedance Amplifier

#### 1 Features

- Internal Midscale Reference Voltage
- · Pseudo-Differential Output Voltage
- Wide Dynamic Range
- Closed-Loop Transimpedance Bandwidth:
  - 125 MHz (5-kΩ Transimpedance Gain,
     1.5-pF External Parasitic Capacitance)
  - 105 MHz (20-kΩ Transimpedance Gain,
     1.5-pF External Parasitic Capacitance)
- Ultralow Input-Referred Current Noise (Brickwall Filter BW = 135 MHz): 15 nA<sub>RMS</sub> (20-kΩ Transimpedance)
- Very Fast Overload Recovery Time: < 25 ns</li>
- Internal Input Protection Diode
- Power Supply:

Voltage: 2.7 V to 3.6 V

Current: 23.4 mA

• Extended Temperature Range: -40°C to +85°C

# 2 Applications

- · Photodiode Monitoring
- High-Speed I/V Conversion
- Optical Amplifiers
- CAT-Scanner Front-Ends

# 3 Description

The OPA857 is a wideband, fast overdrive recovery, fast-settling, ultralow-noise transimpedance amplifier targeted at photodiode monitoring applications. With selectable feedback resistance, the **OPA857** simplifies the design of high-performance optical systems. Very fast overload recovery time and internal input protection provide the best combination to protect the remainder of the signal chain from overdrive while minimizing recovery time. The two selectable transimpedance gain configurations allow high dynamic range and flexibility required in modern transimpedance amplifier applications. The OPA857 is available in a 3-mm × 3-mm VQFN package.

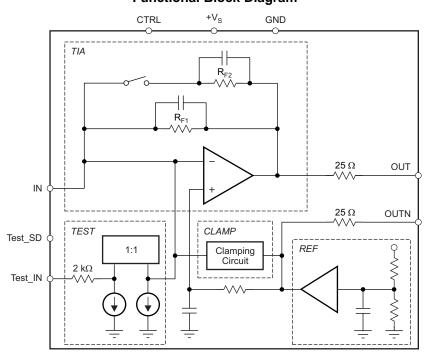
The device is characterized for operation over the full industrial temperature range from -40°C to +85°C.

#### **Device Information**(1)

DEVICE NAME	PACKAGE	BODY SIZE
OPA857	VQFN (16)	3 mm × 3 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

# **Functional Block Diagram**





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# 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

CI	hanges from Revision C (April 2014) to Revision D	Page
•	Changed Features bullets	1
•	Changed "Precision" to "High-Speed" in 2nd Applications bullet	1
•	Changed pin configuration drawing and pin functions table	4
•	Changed Handling Ratings table to ESD Ratings and moved storage temperature to Absolute Maximum Ratings	5
•	Changed Supply Input Voltage min value from 3.0 to 2.7 in Recommended Operating Conditions	5
•	Changed VOUT unit from V <sub>P</sub> to V <sub>PP</sub> in Electrical Charateristics condition line	6
•	Changed all AC Performance values except Closed-Loop Output Impedance	6
•	Changed test conditions for Equivalent Input-Referred Current Noise parameter in Electrical Characteristics	6
•	Deleted Operating Voltage from Electrical Characteristics; already in Recommended Operating Conditions	<mark>7</mark>
•	Deleted Temperature Range from Electrical Characteristics; already in Recommended Operating Conditions	<mark>7</mark>
•	Changed all plots in Typical Characteristics section except figures 17, 35, and 36	8
•	Changed 4.5 k $\Omega$ and 18.2 k $\Omega$ to 5 k $\Omega$ and 20 k $\Omega$ , respectively, in first paragrpah of <i>Overview</i> section	14
•	Changed text in Transimpedance Amplifier (TIA) Block section	15
•	Changed text in Reference Voltage (REF) Block section	15
•	Changed text in Integrated Test Structure (TEST) Block section	15
•	Changed Table 2 values	17
•	Added Test Mode section	17
•	Changed Application Information section	18
•	Changed Figure 50; updated pin names	24

Changed document format to meet new data sheet standards; added Handling Ratings and Device and 

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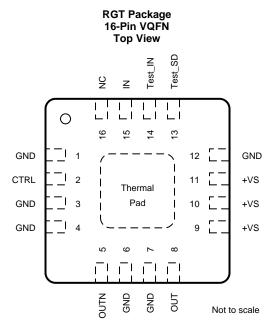
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Changes from Revision A (December 2013) to Revision B	Page
Changed document status to Production Data	1
Changed transimpedance value in both sub-bullets of Bandwidth Features bullet	1
• Changed Extended Temperature Range Features bullet to a range of -40°C to +85°C	1
• Changed first sentence of <i>Description</i> section: added "targeted at photodiode monitoring applications"	1
• Changed temperature range to -40°C to +85°C in last sentence of <i>Description</i> section	1
Changed front-page graphic	1
Added pages 2 through end of document	4
Changes from Original (December 2013) to Revision A	Page
Changed document status to Product Preview	1
Deleted all pages past page 1	
Deleted fourth Applications bullet	1
Changed first sentence of Description section	1



# 5 Pin Configuration and Functions



**Pin Functions** 

	PIN I/O		DESCRIPTION	
NAME	NO.	1/0	DESCRIPTION	
CTRL	2	Į	Control pin for transimpedance gain. GND, logic $0 = 5-k\Omega$ internal resistance; $+V_S$ , logic $1 = 20-k\Omega$ internal resistance.	
GND	1, 3, 4, 6, 7, 12	I	Ground	
IN	15	I	Input	
NC	16	_	Not connected	
OUT	8	0	Signal output	
OUTN	5	0	Common-mode voltage output reference	
Test_IN	14	I	Test mode input. Connect to +V <sub>S</sub> during normal operation.	
Test_SD	13	I	Test mode enable. Connect to GND for normal operation, and connect to +V <sub>S</sub> to enable test mode.	
+V <sub>S</sub>	9, 10, 11	I	Supply voltage	



# 6 Specifications

# 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
	Supply voltage, V <sub>S-</sub> to V <sub>S+</sub>		3.8		
Voltage	Input and output voltage, V <sub>IN</sub> , V <sub>OUT</sub> pins	(V <sub>S-</sub> ) - 0.7	$(V_{S+}) + 0.7$	V	
	Differential input voltage		1		
•	Output current		50	A	
Current	Input current, V <sub>IN</sub> pin		10	mA	
Continuous power dissip	ation	See	Thermal Information	table	
	Maximum junction, T <sub>J</sub>		150		
Temperature	Maximum junction, T <sub>J</sub> (continuous operation, long-term reliability)		140	80	
	Operating free-air, T <sub>A</sub>	-40	85	°C	
	Storage, T <sub>stg</sub>	<b>–</b> 65	150		

<sup>(1)</sup> Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V	Flootroototic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	\/
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

# 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{SS}$	Supply input voltage	2.7	3.3	3.6	V
$T_J$	Operating junction temperature	-40		85	°C

#### 6.4 Thermal Information

	THERMAL METRIC <sup>(1)</sup>	RGT (VQFN)	UNIT
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	91.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.6	°C/W
ΨЈТ	Junction-to-top characterization parameter	7.1	°C/W
ΨЈВ	Junction-to-board characterization parameter	41.7	°C/W
R <sub>0</sub> JC(bot)	Junction-to-case(bottom) thermal resistance	23.1	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report (SPRA953).

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



# 6.5 Electrical Characteristics

at  $T_A = 25^{\circ}C^{(1)}$ ,  $V_S = 3.3$  V,  $V_{S+} - V_{S-} = 3.3$  V,  $C_{Source} = 1.5$  pF,  $V_{OUT} = 0.5$  V<sub>PP</sub> (differential),  $R_L = 500 - \Omega$  differential, single-ended input, pseudo-differential output, and input and output referenced to midsupply (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP M.	AX UNIT	TEST LEVEL <sup>(2)</sup>
AC PERFO	DRMANCE					
	Concil pianal handwidth	CTRL = 1, T <sub>A</sub> = -40°C to +85°C		105	MHz	С
	Small-signal bandwidth	CTRL = 0, $T_A = -40^{\circ}\text{C}$ to +85°C		125	MHz	С
SR	Slew rate (differential)	V <sub>OUT</sub> = 1-V step		215	V/μs	С
	Cottling time to 10/	$V_{OUT} = 0.5$ -V step, CTRL = 0, $T_A = 25$ °C		8	ns	В
	Settling time to 1%	V <sub>OUT</sub> = 0.5-V step, CTRL = 1, T <sub>A</sub> = 25°C		8	ns	В
t <sub>S</sub>	Cattling time to 0.0049/	V <sub>OUT</sub> = 0.5-V step, CTRL = 0		600	ns	С
	Settling time to 0.001%	V <sub>OUT</sub> = 0.5-V step, CTRL = 1		700	ns	С
LIDO	0 11 11 11 11	$V_{OUT} = 0.5 V_{PP}, f = 10 MHz, R_F = 5 k\Omega, T_A = 25^{\circ}C$		-80	dBc	С
HD2	Second-harmonic distortion	$V_{OUT} = 0.5 V_{PP}, f = 10 MHz, R_F = 20 k\Omega, T_A = 25^{\circ}C$		-83	dBc	С
LIDO	TILL III	$V_{OUT} = 0.5 V_{PP}, f = 10 MHz, R_F = 5 k\Omega, T_A = 25^{\circ}C$		-88	dBc	С
HD3	Third-harmonic distortion	$V_{OUT} = 0.5 V_{PP}, f = 10 MHz, R_F = 20 k\Omega, T_A = 25^{\circ}C$		-83	dBc	С
	Equivalent input-referred	CTRL = 0, using 135-MHz brickwall filter		25	nA <sub>RMS</sub>	С
	current noise	CTRL = 1, using 135-MHz brickwall filter		15	nA <sub>RMS</sub>	С
	Overdrive recovery time	I <sub>IN</sub> = 2x overload, CTRL = 1, settling to 1% of final value		25	ns	В
	Closed-loop output impedance	f = 1 MHz (differential)		50	Ω	С
DC PERFO	DRMANCE				*	*
	Tanadana dan sa sala	CTRL = 1 into 500 $\Omega^{(3)(4)}$		18.2	kΩ	С
	Transimpedance gain	CTRL = 0 into 500 $\Omega^{(3)(4)}$		4.5	kΩ	С
	Transimpedance gain error	$T_A = 25^{\circ}\text{C}$ , $R_F = 20 \text{ k}\Omega$ and $R_F = 5 \text{ k}\Omega$		±1% ±15	5%	Α
	0	T <sub>A</sub> = +25°C		±1	±5 mV	Α
$V_{00}$	Output offset voltage	$T_A = -40$ °C to +85°C <sup>(5)</sup>			±6 mV	В
	Output offset voltage drift	$T_A = -40$ °C to +85°C <sup>(5)</sup>		4	:15 μV/°C	С
V <sub>ICR</sub>	Common-mode voltage range	T <sub>A</sub> = 25°C, OUTN	1.78	1.83 1.	.88 V	А
INPUT					<u> </u>	
	Input pin capacitance			2	pF	С
OUTPUT						•
	O	OUT, T <sub>A</sub> = 25°C	0.6		1.9 V	Α
	Output voltage swing	$T_A = -40$ °C to +85°C <sup>(5)</sup>			1.9 V	В
	Output current drive	OUT I'' I I SO O L L OUT LOUTU		+5	mA	С
	(for linear operation)	OUT, differential 50-Ω between OUT and OUTN		-20	mA	С

<sup>(1)</sup> Junction temperature = ambient for 70°C specifications.

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<sup>(2)</sup> Test levels: (A) 100% tested at 25°C. Overtemperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

<sup>(3)</sup> See the Application and Implementation section for details on loading and effective transimpedance gain.

<sup>(4)</sup> Note that the effective transimpedance gain is reduced to 18.2 k $\Omega$  and 4.5 k $\Omega$ , respectively, with a 500- $\Omega$  load resulting from the internal series resistance on OUT and OUTN.

<sup>(5)</sup> Junction temperature = ambient at low temperature; junction temperature = ambient + 3.5°C for overtemperature specifications.



# **Electrical Characteristics (continued)**

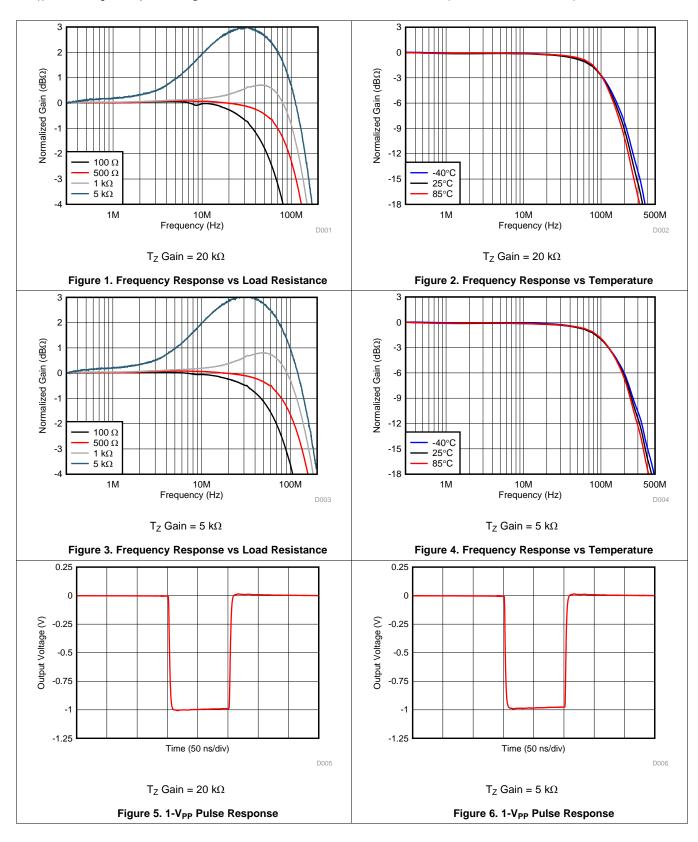
at  $T_A = 25^{\circ}C^{(1)}$ ,  $V_S = 3.3$  V,  $V_{S+} - V_{S-} = 3.3$  V,  $C_{Source} = 1.5$  pF,  $V_{OUT} = 0.5$  V<sub>PP</sub> (differential),  $R_L = 500 - \Omega$  differential, single-ended input, pseudo-differential output, and input and output referenced to midsupply (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL <sup>(2)</sup>
POWER	SUPPLY						
		CTRL = 0, T <sub>A</sub> = 25°C	20.5	23.4	26.3	mA	Α
	Outcoant enerating aurent	CTRL = 0, $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}^{(5)}$	20.0		26.8	mA	В
	Quiescent operating current	CTRL = 1, T <sub>A</sub> = 25°C	20.5	23.4	26.3	mA	Α
		CTRL = 1, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}^{(5)}$	20.0		26.8	mA	В
DCDD		At dc, T <sub>A</sub> = 25°C	70	80		dB	Α
PSRR	Power-supply rejection ratio	$f = 10 \text{ MHz}, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}^{(5)}$	15	18		dB	В
LOGIC L	EVEL (CTRL)		<u>.</u>				
V <sub>IH</sub>	High-level input voltage		2			V	А
V <sub>IL</sub>	Low-level input voltage				0.8	V	Α
	High-level control pin input bias current				1	μΑ	Α
	Low-level control pin input bias current				1	μA	Α

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# 6.6 Typical Characteristics

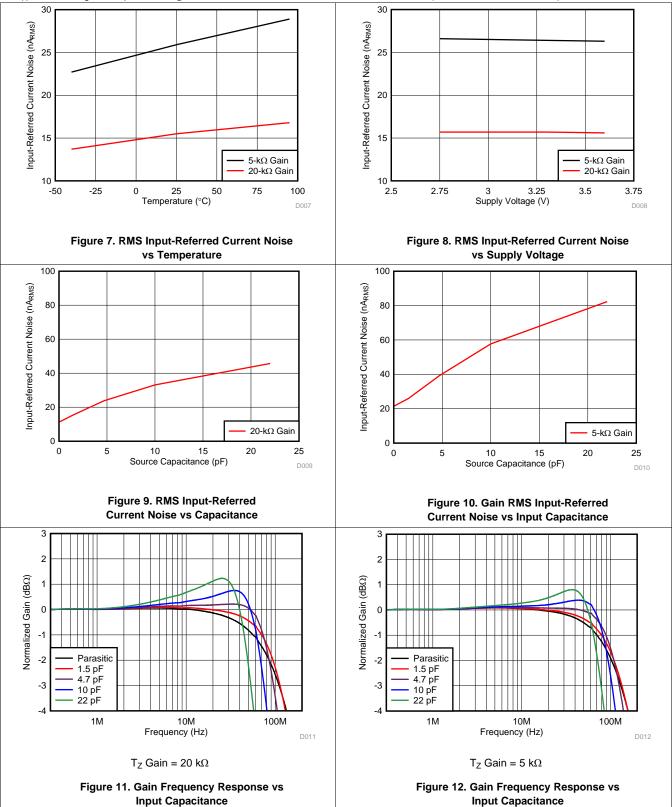
At  $T_A$  = 25°C,  $C_S$  = 1.5 pF, and  $R_L$  = 500- $\Omega$  differential between OUT and OUTN (unless otherwise noted).





# **Typical Characteristics (continued)**

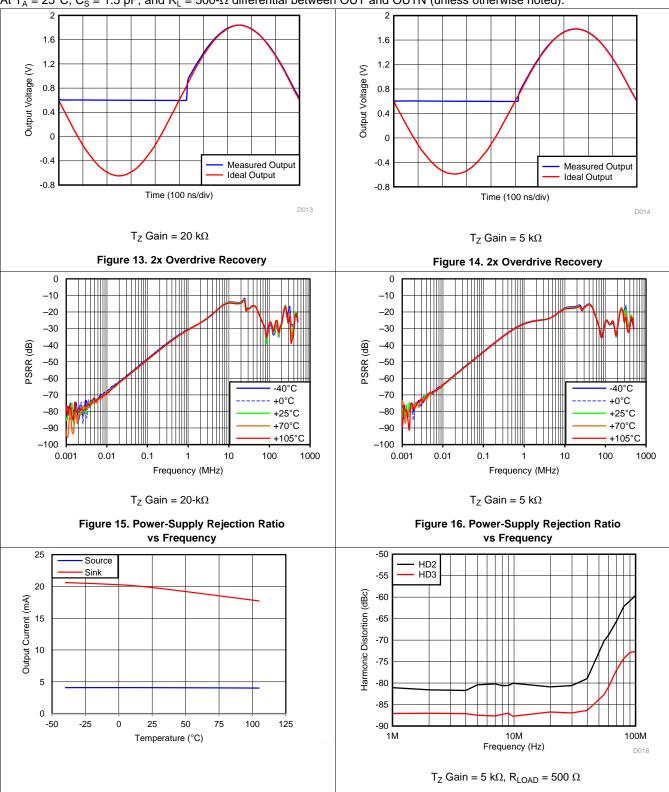
At  $T_A$  = 25°C,  $C_S$  = 1.5 pF, and  $R_L$  = 500- $\Omega$  differential between OUT and OUTN (unless otherwise noted).



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# **Typical Characteristics (continued)**

At  $T_A$  = 25°C,  $C_S$  = 1.5 pF, and  $R_L$  = 500- $\Omega$  differential between OUT and OUTN (unless otherwise noted).



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Figure 17. Output Current vs Temperature

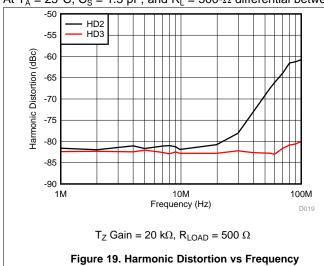
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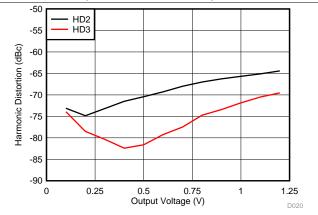
Figure 18. Harmonic Distortion vs Frequency



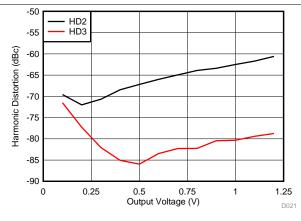
# **Typical Characteristics (continued)**

At  $T_A = 25$ °C,  $C_S = 1.5$  pF, and  $R_L = 500$ - $\Omega$  differential between OUT and OUTN (unless otherwise noted).





 $T_Z$  Gain = 5 k $\Omega,~R_{LOAD}$  = 500  $\Omega,~f$  = 50 MHz

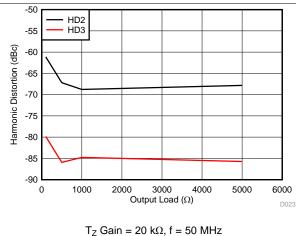


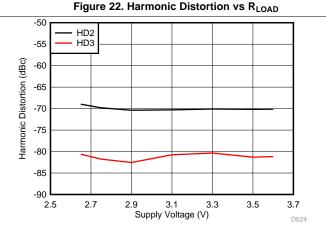
 $T_Z$  Gain = 20 k $\Omega$ ,  $R_{LOAD}$  = 500  $\Omega$ , f = 50 MHz

Figure 20. Harmonic Distortion vs Output Voltage HD2 -55 HD3 Harmonic Distortion (dBc) -60 -65 -75 -80 -85 -90 0 1000 2000 3000 4000 5000 6000 Output Load ( $\Omega$ ) D022

 $T_Z$  Gain = 5 k $\Omega$ , f = 50 MHz

Figure 21. Harmonic Distortion vs Output Voltage





 $T_Z$  Gain = 5 k $\Omega$ ,  $T_A$  = 25°C,  $R_{LOAD}$  = 500  $\Omega$ , f = 50 MHz

Figure 23. Harmonic Distortion vs R<sub>LOAD</sub>

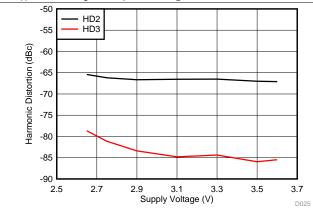
Figure 24. Harmonic Distortion vs Supply Voltage

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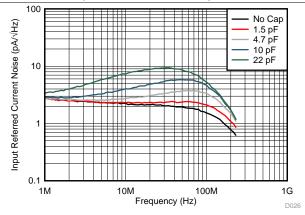
# **Typical Characteristics (continued)**

At  $T_A$  = 25°C,  $C_S$  = 1.5 pF, and  $R_L$  = 500- $\Omega$  differential between OUT and OUTN (unless otherwise noted).



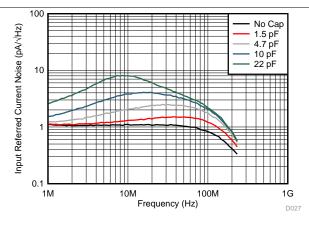
 $T_Z$  Gain = 20 k $\Omega$ ,  $T_A$  = 25°C,  $R_{LOAD}$  = 500  $\Omega$ , f = 50 MHz

Figure 25. Harmonic Distortion vs Supply Voltage



 $T_Z$  Gain = 5 k $\Omega$ 

Figure 26. Input-Referred Current Noise Density vs Frequency



 $T_Z$  Gain = 20 k $\Omega$ 

Figure 27. Input-Referred Current Noise Density vs Frequency

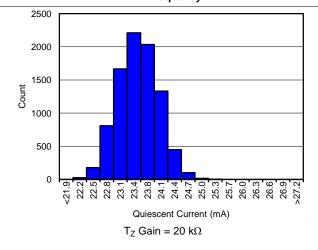
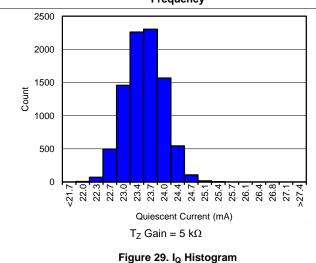


Figure 28. I<sub>Q</sub> Histogram



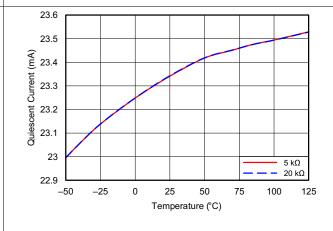
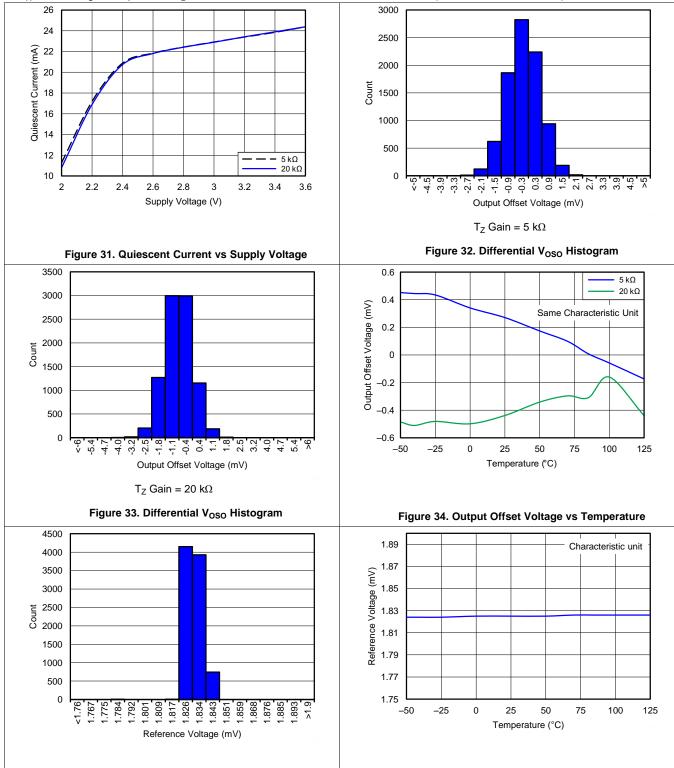


Figure 30. Quiescent Current vs Temperature



# **Typical Characteristics (continued)**

At  $T_A$  = 25°C,  $C_S$  = 1.5 pF, and  $R_L$  = 500- $\Omega$  differential between OUT and OUTN (unless otherwise noted).



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Figure 35. Reference Voltage (V<sub>OUTN</sub>) Distribution Histogram

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Figure 36. Reference Voltage (V<sub>OUTN</sub>) vs Temperature



# 7 Detailed Description

#### 7.1 Overview

The OPA857 provides a unique combination of low-noise, high-bandwidth, and high-transimpedance gain. The amplifier is optimized to achieve greater than 100-MHz bandwidth on either the  $5\text{-k}\Omega$  or  $20\text{-k}\Omega$  transimpedance gain for the lowest possible RMS noise on the output for a targeted low input capacitance of 1.5 pF. Note that this 1.5-pF capacitance includes the board parasitic; thus, great attention must be placed on minimizing stray capacitance in the layout. This value is selected because the device is expected to be driven by a photodiode with biasing high enough to include the photodiode capacitance contribution between approximately 0.5 pF and 0.7 pF, leaving between 0.8 pF to 1 pF for the external parasitic.

The OPA857 is a dedicated transimpedance amplifier with a pseudo-differential output. A block diagram is provided in the Functional Block Diagram section.

There are four distinct blocks in this diagram: a transimpedance amplifier (TIA), a reference voltage (REF), a test structure (TEST), and an internal clamping circuit (CLAMP).

The TIA block of the Functional Block Diagram includes two selectable gain configurations:  $R_{F1}$  and  $R_{F2}$ . For a 500- $\Omega$  load, including the GND alternatives resulting from the internal 25- $\Omega$  series resistor on each output, the resulting gain is 4.5 k $\Omega$  or 18.2 k $\Omega$ . The TIA block is designed to provide excellent bandwidth (> 100 MHz) in both gain configurations with the lowest possible RMS noise over the entire bandwidth. This level of performance is achieved by minimizing the noise gain peaking at higher frequencies. The noise gain peaking resulting from feedback and source capacitance is the main noise contributor in high-speed transimpedance amplifiers.

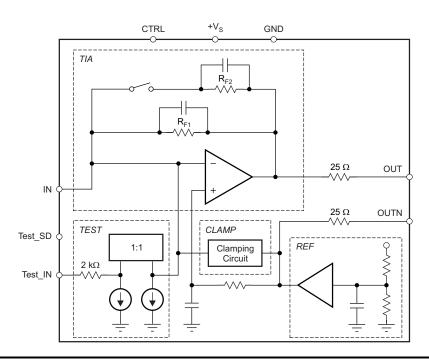
The reference voltage block of the Functional Block Diagram has several purposes: this block provides an adequate dc reference voltage to the input, and provides a dc reference at the output (thus allowing the dc-coupled solution to interface to a fully-differential signal chain). The CMRR provided by the fully-differential signal chain reduces any feedthrough from the OPA857 power supply, thereby increasing the PSRR of the amplifier.

The test structure block is available on the pinout, but the main purpose of this structure is to allow the device characterization to proceed as smoothly as possible.

The internal clamping circuit block and ESD diodes on the IN pin are used for internal protection and to make sure that the amplifier can recover quickly after saturation.

These blocks are each described in further detail in the Feature Description section.

### 7.2 Functional Block Diagram



Product Folder Links: *OPA857* 

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#### 7.3 Feature Description

## 7.3.1 Transimpedance Amplifier (TIA) Block

The amplifier of the TIA block has a class-A output stage, which limits its usable swing from the common-mode voltage of 1.83 V to the negative rail. Because the internal protection allows excellent overdrive recovery, the negative swing cannot go closer than 0.6 V to the rail. The resulting output dynamic range of the OPA857 on a 3.3-V supply is 1.2 V. This 1.2-V swing corresponds to a maximum input current of 60  $\mu$ A in the high-gain configuration, and 240  $\mu$ A in the low-gain configuration. A 25- $\Omega$  series resistor between the internal output of the TIA block and OUT (pin 8) limits the amplifier load during short-circuit conditions. A similar 25- $\Omega$  series resistor also exists between the output of the reference voltage amplifier and OUTN (pin 5). The internal resistors on OUT and OUTN reduce the overall gain of the OPA857. With a 500- $\Omega$  differential load, the attenuation resulting from the load is 0.83 dB, which affects the overall transimpedance gain. Because of the load attenuation, the 20-k $\Omega$  transimpedance gain is reduced to an effective 18.2 k $\Omega$ , while the 5-k $\Omega$  internal resistor gain is reduced to an effective 4.5-k $\Omega$  internal resistor.

#### 7.3.2 Reference Voltage (REF) Block

The reference output voltage is set to be 5/9th of the power supply. Thus, for a single 3.3-V supply, the reference voltage is 1.83 V. A wideband amplifier with low output impedance to high frequencies is used in the reference voltage block. The amplifier output drives two paths: the first path drives the output (OUTN) through a  $25-\Omega$  series resistor, while the second path drives the noninverting input of the TIA block. The output from the second path is filtered through an RC filter in order to reduce the noise contribution from the reference block.

# 7.3.3 Integrated Test Structure (TEST) Block

In order to evaluate the low input capacitance condition on the input of the OPA857, simply evaluate the OPA857 performance without the photodiode. An integrated voltage-to-current conversion is implemented and can be accessed with the use of Test\_SD (pin 13) and Test\_IN (pin 14). This V-to-I converter structure is represented in Figure 37. If required, a capacitor can be added to IN (pin 15) to match the target input capacitance during normal operation with an external photodiode. The test structure in Figure 37 allows for the evaluation of the OPA857 as a TIA using standard lab equipment, such as function generators and network analyzers.

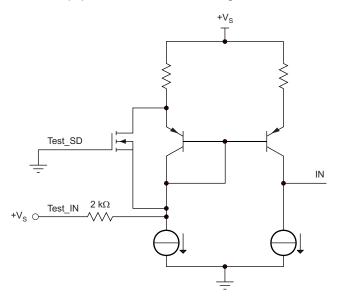


Figure 37. Internal V-to-I Converter

When using a photodiode, make sure that this source is turned off completely. This test structure is not intended to be used as a output dc-control voltage.



### **Feature Description (continued)**

#### 7.3.4 Internal Clamping Circuit (CLAMP) Block

The OPA857 is built using a very high-speed, complementary, BICMOS process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings<sup>(1)</sup> table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 38.

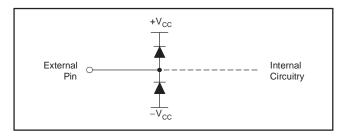


Figure 38. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30-mA continuous current. Use additional external low-capacitance protection where higher currents are possible.

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



#### 7.4 Device Functional Modes

#### 7.4.1 Gain Control

The device transimpedance gain is controlled with the CTRL pin. Setting the CTRL pin high results in selecting the high-gain configuration. Setting the CTRL pin low results in selecting the low-gain configuration, as described in Table 1

**Table 1. Gain Control Logic Table** 

GAIN	CTRL (Pin 2)
5 kΩ	Logic 0 (GND)
20 kΩ	Logic 1 (+V <sub>S</sub> )

#### 7.4.2 Test Mode

The OPA857 operates in normal mode when the input is driven by a photodiode. In test mode, the test structure described in the *Integrated Test Structure (TEST) Block* section is used to emulate a photodiode using a voltage input. Table 2 describes how to configure the OPA857 in each mode.

**Table 2. Mode Configuration** 

MODE	Test_IN PIN CONNECTED TO	Test_SD PIN CONNECTED TO			
Normal mode	+V <sub>S</sub>	GND			
Test mode	AC-coupled input using a series cap or dc-coupled signal on a 2.1-V (approx) offset voltage	+V <sub>S</sub>			

Set an adequate dc voltage at the input to make sure that the output is operating within normal operation. At minimum, the output of the TIA block must be set to 5/9th of the supply voltage in preparation for a pulse configuration. For sine-wave operation, as required when measuring a frequency response, set the dc voltage on the OUT pin to allow the full sine-wave amplitude and avoid clipping. In such a case, the OUT pin voltage is set lower than 5/9th of the supply voltage.

Note that the  $2-k\Omega$  internal resistance used for the V-to-I conversion is not trimmed and can vary  $\pm 15\%$  with process. Therefore, the source must be capable of sourcing both dc and ac voltages to make sure that the output voltage swing is compliant with the class-A output stage of the TIA block. Any change in the test circuit configuration (such as gain change) requires a new calibration of the internal V-to-I converter.

Again if a photodiode is used, the internal V-to-I converter must be shut off completely. Failure to do so results in degraded performance and higher than normal quiescent current.



# 8 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

# 8.1 Application Information

The OPA857 is a transimpedance amplifier offering two selectable gains. This device is used in conjunction with a photodiode at its input. The output is pseudo differential and may or may not require the use of a fully differential amplifier, depending on the analog-to-digital converter (ADC) used for implementation.

The OPA857 requires a photodiode to be connected to the positive bias voltage because the output voltage can only swing down from the reference voltage (1.85 V for a 3.3-V supply) to ground.

# 8.2 Typical Application

### 8.2.1 TIA With Associated Signal Chain

Figure 39 presents a complete end-to-end receive signal chain for an optical input. It includes a high-speed photodiode, the OPA857, a THS4541 fully-differential amplifier, and a 16-bit, 160-MSPS, high-speed ADC. For the complete wide-bandwidth, optical front-end reference design, go to http://www.ti.com/tool/TIDA-00725.

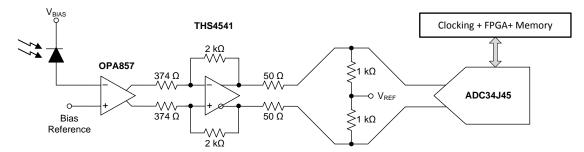


Figure 39. TIA With Associated Signal Chain



### Typical Application (continued)

#### 8.2.1.1 Design Requirements

For this example, use the values listed in Table 3 for the input parameters.

**Table 3. Design Parameters** 

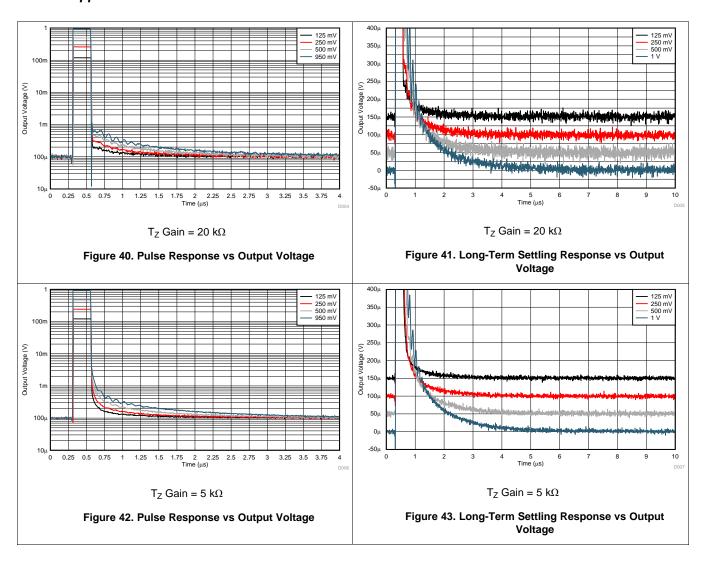
DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage	5-V external supply
Analog bandwidth	120 MHz
ADC sampling rate	160 MSPS
Maximum system gain	100 kΩ
Programmable transimpedance gain	5 kΩ / 20 kΩ
Maximum signal swing	1 V <sub>PP</sub>
Noise performance	≥ 60-dB SNR
Averaged noise performance	< 10-μV <sub>RMS</sub>

#### 8.2.1.2 Detailed Design Procedure

- 1. Use a high-speed, low input capacitance photodiode, such as the NR7500 or NR8300, as the front-end optical sensor. Take care during layout to minimize parasitic capacitance added because of the PCB.
- 2. Bias the photodiode with the cathode connected to a positive supply, and the anode connected to IN pin of the OPA857. These connections make sure that the photodiode sources an output current that results in the OPA857 output swinging down below the reference voltage =  $(5/9) \times 3.3 \text{ V} = 1.83 \text{ V}$ .
- 3. Disable the OPA857 test mode by setting Test\_IN =  $+V_S$  and Test\_SD = GND. The transimpedance gain is selected by setting CTRL =  $+V_S$  (gain = 20 k $\Omega$ ) or CTRL = GND (gain = 5 k $\Omega$ ).
- 4. The THS4541 is configured in a gain of 5 V/V in order to achieve a maximum signal transimpedance gain of 100 k $\Omega$ . It is important to carefully select the value of the RG gain resistors for the THS4541.
- Setting RG very low increases the resistive loading on the previous OPA857 output stage, and reduces the bandwidth of the OPA857.
- 6. Setting  $R_G$  very high results in a large value of feedback resistance,  $R_F$ , on the THS4541 in order to achieve the desired 5V/V gain.  $R_F$  interacts with the input capacitance of the THS4541 to create a zero in the noise-gain response of the amplifier, and if not properly compensated, results in reduced phase-margin and potential instability.
- 7. A value of  $R_G$  = 374  $\Omega$  was selected that results in a total differential load of 798  $\Omega$  on the OPA857. The resultant  $R_F$  = 2 k $\Omega$ .
- 8. The response to an optical pulsed input is shown in Figure 40 to Figure 43. To prevent signal reflections between the THS4541 output and the ADC34J45 input, the signal is doubly terminated through 50-Ω resistors. If the THS4541 and ADC34J45 are physically close together on the PCB, then the double-termination is eliminated, which increases the overall gain of the signal chain without affecting the transient response of the system. These results were verified, and the complete data is available in reference design TIDA-00725.
- 9. An optional antialiasing filter can be added between the THS4541 and the ADC34J45 to reduce system noise caused by aliasing.



### 8.2.1.3 Application Curves





#### 8.2.2 Extending Transimpedance Bandwidth

At the core of the OPA857 is an ultrawide bandwidth op amp. One of the highlights of the OPA857 is the relatively small change in the transimpedance bandwidth as a function of the internal gain selected; 130 MHz (gain =  $5 \text{ k}\Omega$ ) and 105 MHz (gain =  $20 \text{ k}\Omega$ ). Theoretically, for a four times increase in gain, the bandwidth should reduce by two times; however, as observed in the case of the OPA857, the results do not follow theory. For more information on the various factors that contribute to an amplifier frequency-response performance when configured as a TIA, see What You Need To Know About Transimpedance Amplifiers – Part 1 on the TI E2E Community website at e2e.ti.com. This blog also contains a reference to an excel calculator to simplify TIA designs when using discrete opamps. The OPA857 is unique in displaying this type of behavior because the CTRL logic controls an internal switch in the amplifier core that recompensates the amplifier open-loop gain characteristic depending upon the logic level. In this application, it it shown how the closed-loop transimpedance bandwidth can be increased to greater than 250 MHz. The circuit used for this test is shown in Figure 44. An external feedback resistor,  $R_F$ , is added in parallel to the internal transimpedance gain resistors of the OPA857. This resistor has the effect of reducing the overall transimpedance gain, but with increased bandwidth.

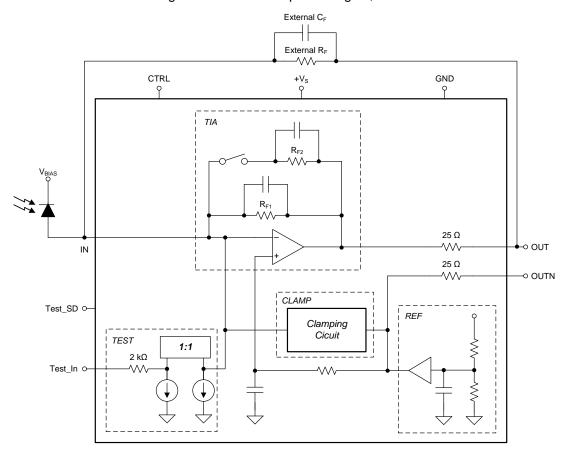


Figure 44. Extending Transimpedance Bandwidth

#### 8.2.2.1 Design Requirements

For this example, use the values listed in Table 4 for the input parameters.

**Table 4. Design Parameters** 

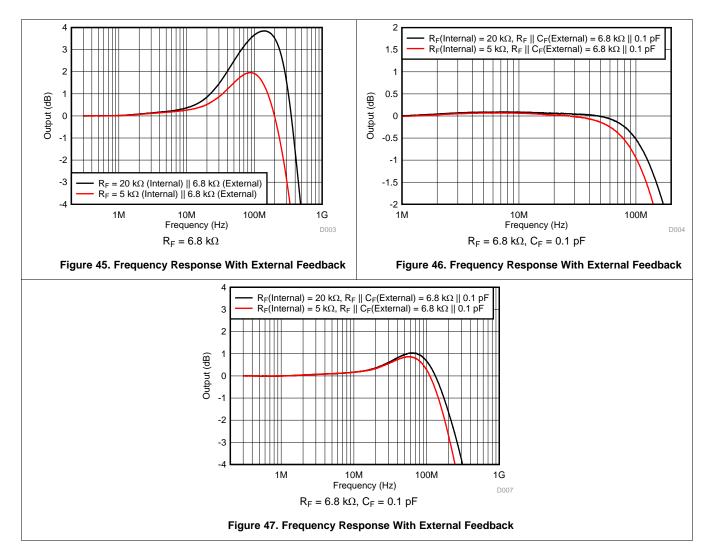
DESIGN PARAMETER	EXAMPLE VALUE		
Supply voltage	3.3 V		
Output swing	500 mV <sub>PP</sub>		
Differential output load	500 k $\Omega$ and 1 k $\Omega$		
Target bandwidth	250 MHz		
Effective transimpedance gain	5 kΩ		

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#### 8.2.2.2 Application Curves

Figure 45 shows the frequency response with a feedback resistance of 6.8 k $\Omega$  and an output load of 500  $\Omega$ . The large amount of peaking indicates a low phase-margin and potential instability. Next, a 0.1-pF feedback capacitor,  $C_F$ , is added in parallel to the 6.8-k $\Omega$   $R_F$ . Both  $R_F$  and  $C_F$  interact to create pole in the noise gain curve that counteracts the effect of the zero caused by  $R_F$ , and the total input capacitance at pin IN of the OPA857. The input capacitance is caused by the opamps inherent input capacitance, the photodiode capacitance, and the parasitic input capacitance from the PCB. The pole zero cancellation increases the phase margin, as is evident in the reduced peaking shown in Figure 46. In Figure 47, an output load of 1 k $\Omega$  was used, along with an  $R_F$  = 6.8 k $\Omega$  and  $C_F$  = 0.1 pF. The reduced load helps to increase the op amp open-loop gain, which in turn increases the closed-loop bandwidth of the OPA857 circuit.





# 9 Power-Supply Recommendations

Use a linear power supply with good PSRR. For a good, high-frequency, power-supply bypass, use a ceramic capacitor connected as close as possible to the  $+V_S$  pin.

### 10 Layout

### 10.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the OPA857 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

- a. Minimize parasitic capacitance to any ac ground for all signal I/O pins. Parasitic capacitance on the inverting input pin can cause instability. To reduce unwanted capacitance, open a window around the signal I/O pins in all ground and power planes around those pins. Otherwise, make sure that ground and power planes are unbroken elsewhere on the board.
- b. **Minimize the distance** (< 0.25") from the power-supply pins to high-frequency 0.1- $\mu$ F decoupling capacitors, as shown in Figure 48. At the device pins, make sure that the ground and power-plane layout are not in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and decoupling capacitors. Always decouple the power-supply connections with these capacitors. An optional supply decoupling capacitor (0.1  $\mu$ F) across the two power supplies (for bipolar operation) improves second-harmonic distortion performance. Use larger (2.2  $\mu$ F to 6.8  $\mu$ F) decoupling capacitors, effective at lower frequencies, on the main supply pins. These capacitors can be placed somewhat farther from the device and can be shared among several devices in the same area of the PC board.
- c. Careful selection and placement of external components preserves the high-frequency performance of the OPA857. Use very low reactance type resistors. Surface-mount resistors function best and allow a tighter overall layout. Metal-film or carbon composition, axially-leaded resistors also provide good highfrequency performance. Again, keep the leads and PC board traces as short as possible. Never use wirewound type resistors in a high-frequency application.
- d. Connections to other wideband devices on the board can be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Use relatively wide traces (50 mils to 100 mils), preferably with ground and power planes opened up around them.
- e. **Do not socket a high-speed part such as the OPA857.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that makes achieving a smooth, stable frequency response almost impossible. Best results are obtained by soldering the OPA857 onto the board.



# 10.2 Layout Example

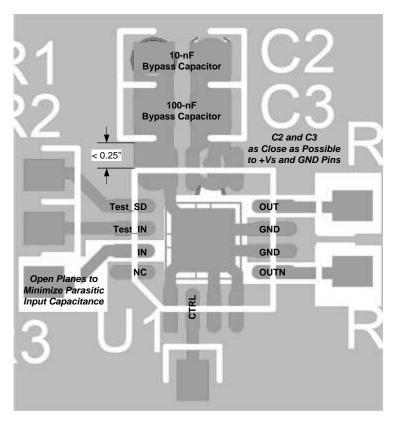


Figure 48. Layout Example



# 11 Device and Documentation Support

#### 11.1 Device Support

#### 11.1.1 Development Support

#### 11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the OPA857. The summary information for this fixture is shown in Table 5.

**Table 5. EVM Ordering Information** 

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER		
OPA857IRGT	RGT	OPA857EVM	SBOU138		

The EVM can be requested at the Texas Instruments web site (www.ti.com) through the OPA857 product folder.

#### 11.1.1.2 Spice Model

Computer simulation of circuit performance using spice is often useful when analyzing the performance of analog circuits and systems. The previous statement is particularly true for transimpedance applications where parasitic capacitance and inductance can have a major effect on circuit performance. A spice model for the OPA857 is available through the OPA857 product folder under simulation models. These models do a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. These models, however, do not do as well in predicting harmonic distortion.

#### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation, see the following:

- OPA857EVM Evaluation Module (SBOU138)
- Transimpedance Considerations for High-speed Amplifiers (SBOA122)
- Wide Bandwidth Optical Front-end Reference Design (TIDUAZ1)
- Reference Design for Extending the OPA857 Transimpedance Bandwidth (TIDUBX7)
- Learn how to compensate transimpedance amplifiers intuitively in:
   What You Need To Know About Transimpedance Amplifiers Part 1 (Cherian 2016)

#### 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 11.5 Trademarks

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### 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# 11.7 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 10-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
OPA857IRGTR	Active	Production	VQFN (RGT)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA857
OPA857IRGTR.B	Active	Production	VQFN (RGT)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA857
OPA857IRGTT	Active	Production	VQFN (RGT)   16	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA857
OPA857IRGTT.B	Active	Production	VQFN (RGT)   16	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA857

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 20-Apr-2023

# TAPE AND REEL INFORMATION



# TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

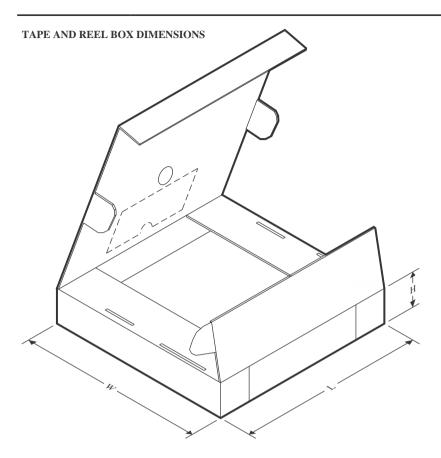
#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA857IRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA857IRGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

www.ti.com 20-Apr-2023



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA857IRGTR	VQFN	RGT	16	3000	346.0	346.0	33.0
OPA857IRGTT	VQFN	RGT	16	250	210.0	185.0	35.0



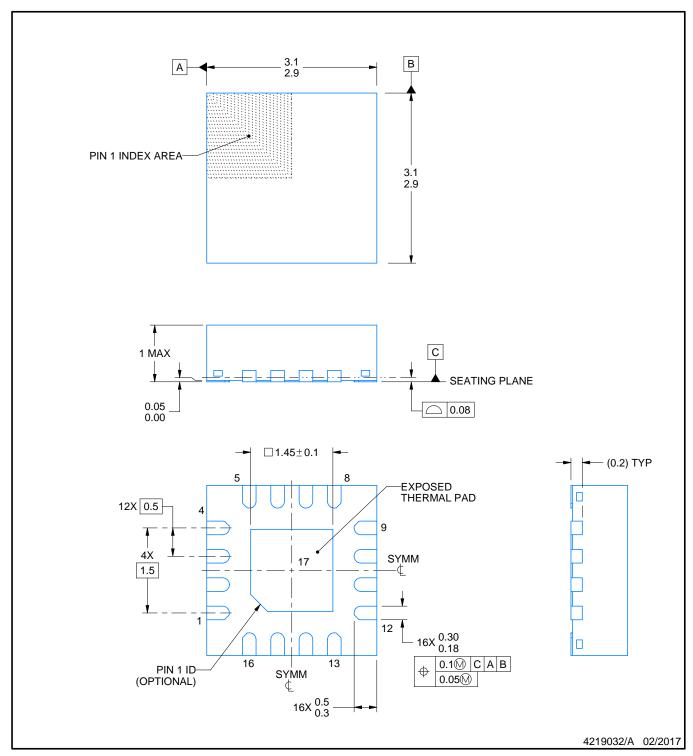
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.







PLASTIC QUAD FLATPACK - NO LEAD

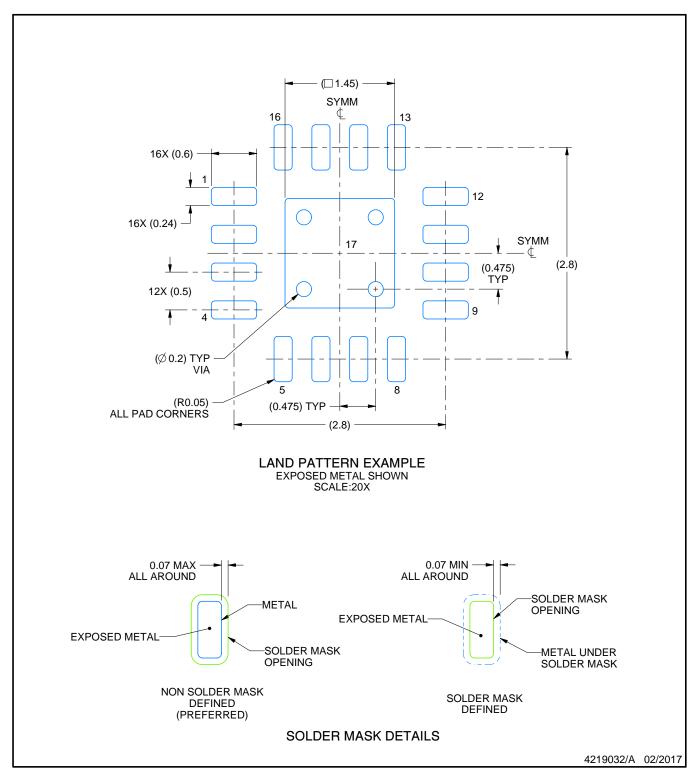


#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
- The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
   Reference JEDEC registration MO-220



PLASTIC QUAD FLATPACK - NO LEAD

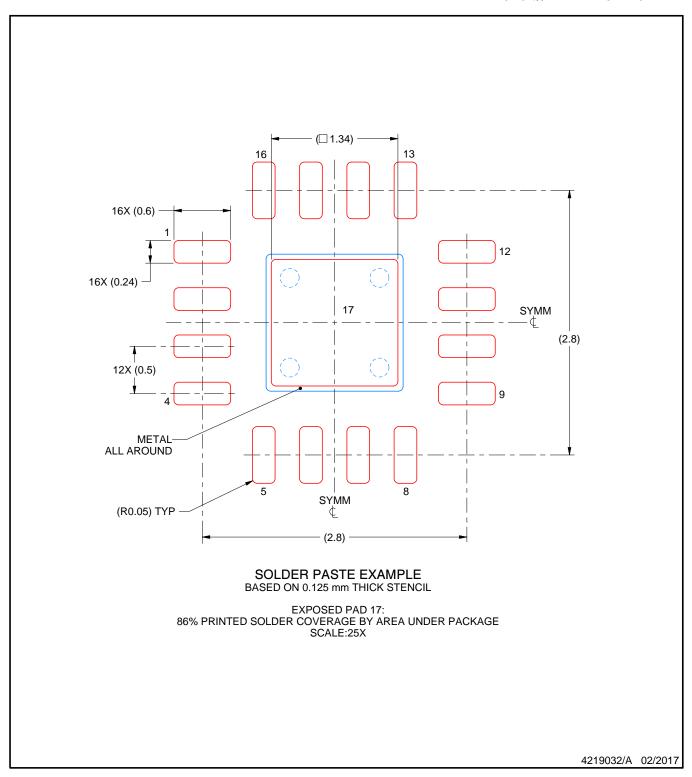


NOTES: (continued)

- 5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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