







OPA992, OPA2992, OPA4992

SBOSA10F - JUNE 2021 - REVISED MARCH 2024

OPAx992 40V Rail-to-Rail Input/Output, Low Offset Voltage, Low Noise Op Amp

1 Features

Low offset voltage: ±210µV

Low offset voltage drift: ±0.25µV/°C

Low noise: $7nV/\sqrt{Hz}$ at 1kHz. $4.4nV/\sqrt{Hz}$ broadband

High common-mode rejection: 115dB

Low bias current: ±10pA

Rail-to-rail input and output

MUX-friendly/comparator inputs

 Amplifier operates with differential inputs up to supply rail

- Amplifier can be used in open-loop or as comparator

Wide bandwidth: 10.6MHz GBW, unity-gain stable

High slew rate: 32V/µs

Low quiescent current: 2.4mA per amplifier

Wide supply: ±1.35V to ±20V, 2.7V to 40V

Robust EMIRR performance

2 Applications

Multiplexed data-acquisition systems

Test and measurement equipment

Motor drive: power stage and control modules

Power delivery: UPS, server, and merchant network power

ADC driver and reference buffer amplifier

Programmable logic controllers

Analog input and output modules

High-side and low-side current sensing

High precision comparator

3 Description

The OPAx992 family (OPA992, OPA2992, and OPA4992) is a family of high voltage (40V) general purpose operational amplifiers. These devices offer excellent DC precision and AC performance, including rail-to-rail input/output, low offset (±210µV, typical), low offset drift (±0.25µV/°C, typical) and low noise $(7nV/\sqrt{Hz})$ at 1kHz, 4.4nV/ \sqrt{Hz} at 10kHz).

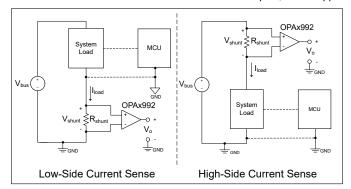
Features such as differential and common-mode input voltage ranges to the supply rails, high short-circuit current (±65mA), and high slew rate (32V/µs) make the OPAx992 a flexible, robust, and high-performance op amp for high-voltage industrial applications.

The OPAx992 family of op amps is available in smallsize packages (such as X2QFN and WSON), as well as standard packages (such as SOT-23, SOIC, and TSSOP), and is specified from -40°C to 125°C.

Device Information

PART NUMBER ⁽¹⁾	CHANNEL COUNT	PACKAGE	PACKAGE SIZE(2)	
OPA992	Single	DCK (SC70, 5)	2mm × 2.1mm	
OFA992	Sirigle	DBV (SOT-23, 5)	2.9mm × 2.8mm	
OPA992S	Single, Shutdown	DBV (SOT-23, 6)	2.9mm × 2.8mm	
		D (SOIC, 8)	4.9mm × 6mm	
	Dual	DDF (SOT-23, 8)	2.9mm × 2.8mm	
OPA2992		PW (TSSOP, 8)	3mm × 6.4mm	
		DGK (VSSOP, 8)	3mm × 4.9mm	
		DSG (WSON, 8)	2mm × 2mm	
OPA2992S	Dual, Shutdown	RUG (X2QFN, 10)	1.5mm × 2mm	
004 4000	Quad	D (SOIC, 14)	8.65mm × 6mm	
OPA4992	Quau	PW (TSSOP, 14)	5mm × 6.4mm	

- For more information, see Section 10. (1)
- The package size (length × width) is a nominal value and (2)includes pins, where applicable.



OPAx992 in Current-Sensing Applications



Table of Contents

1 Features1	6.4 Device Functional Modes	.28
2 Applications1	7 Application and Implementation	. 29
3 Description1	7.1 Application Information	. 29
4 Pin Configuration and Functions3	7.2 Typical Applications	
5 Specifications7	7.3 Power Supply Recommendations	.31
5.1 Absolute Maximum Ratings7	7.4 Layout	. 31
5.2 ESD Ratings7	8 Device and Documentation Support	.33
5.3 Recommended Operating Conditions7	8.1 Device Support	33
5.4 Thermal Information for Single Channel8	8.2 Documentation Support	
5.5 Thermal Information for Dual Channel8	8.3 Receiving Notification of Documentation Updates	.33
5.6 Thermal Information for Quad Channel	8.4 Support Resources	. 33
5.7 Electrical Characteristics9	8.5 Trademarks	.33
5.8 Typical Characteristics11	8.6 Electrostatic Discharge Caution	.33
6 Detailed Description19	8.7 Glossary	.34
6.1 Overview19	9 Revision History	. 34
6.2 Functional Block Diagram19	10 Mechanical, Packaging, and Orderable	
6.3 Feature Description20	Information	. 35



4 Pin Configuration and Functions

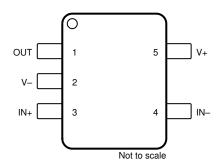


Figure 4-1. OPA992 DBV Package 5-Pin SOT-23 (Top View)

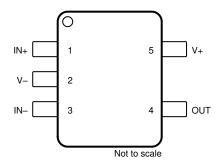


Figure 4-2. OPA992 DCK Package 5-Pin SC70 (Top View)

Table 4-1. Pin Functions: OPA992

	PIN		- I/O	DESCRIPTION		
NAME	SOT-23	SC70	1/0	DESCRIPTION		
IN+	3	1	I	Noninverting input		
IN-	4	3	I	Inverting input		
OUT	1	4	0	Output		
V+	5	5	_	Positive (highest) power supply		
V-	2	2	_	Negative (lowest) power supply		

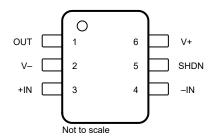


Figure 4-3. OPA992S DBV Package 6-Pin SOT-23 (Top View)

Table 4-2. Pin Functions: OPA992S

F	PIN	I/O	DESCRIPTION
NAME	NO.	1/0	DESCRIPTION
+IN	3	I	Noninverting input
-IN	4	I	Inverting input
OUT	1	0	Output
SHDN	5	I	Shutdown: low = amplifier enabled, high = amplifier disabled
V+	6	_	Positive (highest) power supply
V-	2	_	Negative (lowest) power supply



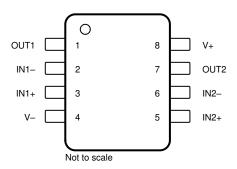
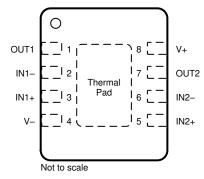


Figure 4-4. OPA2992 D, DDF, PW, and DGK
Package
8-Pin SOIC, SOT-23, TSSOP, and VSSOP
(Top View)



A. Connect thermal pad to V–. See Section 6.3.10 for more information.

Figure 4-5. OPA2992 DSG Package^(A) 8-Pin WSON With Exposed Thermal Pad (Top View)

Table 4-3. Pin Functions: OPA2992

	Table 4 of 1 in 1 another of 7 table						
PIN		I/O	DESCRIPTION				
NAME	NO.	1 1/0	DESCRIPTION				
IN1+	3	I	Noninverting input, channel 1				
IN1-	2	I	Inverting input, channel 1				
IN2+	5	I	Noninverting input, channel 2				
IN2-	6	I	Inverting input, channel 2				
OUT1	1	0	Output, channel 1				
OUT2	7	0	Output, channel 2				
V+	8	_	Positive (highest) power supply				
V-	4	_	Negative (lowest) power supply				



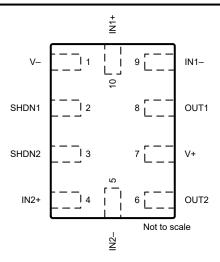


Figure 4-6. OPA2992S RUG Package 10-Pin X2QFN (Top View)

Table 4-4. Pin Functions: OPA2992S

1	PIN	1/0	DESCRIPTION
NAME	NO.	1/0	DESCRIPTION
IN1+	10	I	Noninverting input, channel 1
IN1-	9	I	Inverting input, channel 1
IN2+	4	I	Noninverting input, channel 2
IN2-	5	I	Inverting input, channel 2
OUT1	8	0	Output, channel 1
OUT2	6	0	Output, channel 2
SHDN1	2	I	Shutdown, channel 1: low = amplifier enabled, high = amplifier disabled. See <i>Shutdown</i> section for more information.
SHDN2	3	1	Shutdown, channel 2: low = amplifier enabled, high = amplifier disabled. See <i>Shutdown</i> section for more information.
V+	7	_	Positive (highest) power supply
V-	1	_	Negative (lowest) power supply



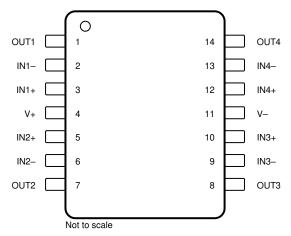


Figure 4-7. OPA4992 D and PW Package 14-Pin SOIC and TSSOP (Top View)

Table 4-5. Pin Functions: OPA4992

	PIN	I/O	DESCRIPTION
NAME	NO.		DESCRIPTION
IN1+	3	I	Noninverting input, channel 1
IN1-	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2-	6	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3-	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4-	13	I	Inverting input, channel 4
OUT1	1	0	Output, channel 1
OUT2	7	0	Output, channel 2
OUT3	8	0	Output, channel 3
OUT4	14	0	Output, channel 4
V+	4	_	Positive (highest) power supply
V-	11	_	Negative (lowest) power supply



5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	<u> </u>		MIN	MAX	UNIT
			IVIIIN	IVIAA	UNII
Supply voltage, $V_S = (V+)$			0	42	V
	Common-mode voltage ⁽³⁾		(V-) - 0.5	(V+) + 0.5	V
Signal input pins	Differential voltage ⁽³⁾			V _S + 0.2	V
	Current ⁽³⁾		-10	10	mA
Shutdown pin voltage ⁽⁴⁾			V–	(V-) + 20	V
Output short-circuit ⁽²⁾			Continuous		
Operating ambient temper	rature, T _A		- 55	150	°C
Junction temperature, T _J				150	°C
Storage temperature, T _{stg}			-65	150	°C

- (1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* will cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.
- (2) Short-circuit to ground, one amplifier per package. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction.
- (3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
- (4) Cannot exceed V+.

5.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500	\/
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Vs	Supply voltage, (V+) – (V–)	2.7	40	V
V _I	Common mode voltage range	(V-)	(V+)	V
V _{IH}	High level input voltage at shutdown pin (amplifier disabled)	1.1	(V-) + 20 ⁽¹⁾	V
V _{IL}	Low level input voltage at shutdown pin (amplifier enabled)	(V-)	0.2	V
T _A	Specified temperature	-40	125	°C

Cannot exceed V+.



5.4 Thermal Information for Single Channel

			OPA992, OPA992S	}	
THERMAL METRIC ⁽¹⁾		_	BV T-23)	DCK (SC70)	UNIT
			6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.4	166.9	198.1	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	83.9	83.9	94.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.5	47.1	45.3	°C/W
ΨЈТ	Junction-to-top characterization parameter	25.4	25.9	16.9	°C/W
ΨЈВ	Junction-to-board characterization parameter	52.1	47.0	45.0	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Thermal Information for Dual Channel

		OPA2992, OPA2992S						
THERMAL METRIC(1)		D (SOIC)	DDF (SOT-23)	DGK (VSSOP)	DSG (WSON)	PW (TSSOP)	RUG (X2QFN)	Unit
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	131.0	149.6	174.2	74.8	183.4	131.7	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	73.0	85.3	65.9	93.6	72.4	52.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	74.5	68.6	95.9	42.1	114.0	62.0	°C/W
ΨЈТ	Junction-to-top characterization parameter	25.0	7.9	11.0	3.8	12.1	1.1	°C/W
ΨЈВ	Junction-to-board characterization parameter	73.8	68.4	94.4	41.9	112.3	61.8	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	17.0	N/A	N/A	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.6 Thermal Information for Quad Channel

		OPA	OPA4992			
	THERMAL METRIC ⁽¹⁾	D (SOIC)	PW (TSSOP)	UNIT		
		14 PINS	14 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.0	118.8	°C/W		
R _{0JC(top)}	Junction-to-case (top) thermal resistance	55.1	47.0	°C/W		
$R_{\theta JB}$	Junction-to-board thermal resistance	54.8	61.9	°C/W		
ΨЈТ	Junction-to-top characterization parameter	16.7	5.5	°C/W		
ΨЈВ	Junction-to-board characterization parameter	54.4	61.3	°C/W		
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W		

⁽¹⁾ For more information about traditional and new thermal metrics, see the <u>Semiconductor and IC Package Thermal Metrics</u> application note.



5.7 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at T_A = 25°C, R_L = 10 k Ω connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

DLTAGE						
				±0.21	±1	
Input offset voltage	V _{CM} = V-	T _A = -40°C to 125°C			±1.2	mV
Input offset voltage drift	V _{CM} = V-	**		±0.25		μV/°C
	OPA992, OPA2992, V _{CM} =	<i>A</i>		±0.2	±1.3	•
Input offset voltage versus power supply	OPA2992SIRUGR, V _{CM} = V-,			±0.2	±3.7	μV/V
	OPA4992, V _{CM} = V-, V _S = 5 V to 40 V	$T_A = -40^{\circ}\text{C to } 125^{\circ}\text{C}$		±0.4	±1.8	
	OPA992, OPA2992, OPA4992, V _{CM} = V-, V _S = 2.7 V to 40 V ⁽¹⁾			±0.8	±7	
DC channel separation		,		0.4		μV/V
CURRENT						
Input bias current				±10		pA
Input offset current				±10		pA
			1			
				2.77		μV _{PP}
Input voltage noise	f = 0.1 Hz to 10 Hz			0.49		μV _{RMS}
	f = 1 kHz		7			
Input voltage noise density	f = 10 kHz	4.4			nV/√Hz	
Input current noise density	f = 1 kHz			60		fA/√Hz
TAGE RANGE						
Common-mode voltage range			(V-)		(V+)	V
Common-mode rejection ratio	V (PMOS pair) ⁽¹⁾		100	100 115		
			75	98		
	$V_S = 2.7 \text{ V, V-} < V_{CM} < (V+) - 2 \text{ V (PMOS pair)}$			90		dB
	V _S = 2.7 – 40 V, (V+) – 1 V < V _{CM} < V+ (NMOS pair)			79		
	(V+) - 2 V < V _{CM} < (V+) - 1 V		See Offset Voltage vs Common-Mode Voltage (Transition Region)			
EDANCE						
Differential				100 9		MΩ pF
Common-mode				6 1		TΩ pF
P GAIN						
Open-loop voltage gain	$V_S = 40 \text{ V}, V_{CM} = V_S / 2,$ $(V-) + 0.1 \text{ V} < V_O < (V+) -$ 0.1 V		120	142		
	V _S = 40 V, V _{CM} = V _S / 2, (V–) + 0.12 V < V _O < (V+) – 0.12 V	T _A = -40°C to 125°C		142		al D
	V _S = 5 V, V _{CM} = V _S / 2,		104	125		dB
	$(V-) + 0.1 V < V_O < (V+) - 0.1 V(1)$	T _A = -40°C to 125°C		125		
	1 U. I V ^{1.7}					
	$V_S = 2.7 \text{ V}, V_{CM} = V_S / 2,$	~	90	105		
	DC channel separation S CURRENT Input bias current Input offset current Input voltage noise Input voltage noise density Input current noise density TAGE RANGE Common-mode voltage range Common-mode rejection ratio EDANCE Differential Common-mode P GAIN	Input offset voltage versus power supply OPA992, OPA2992, $V_{CM} = V_{-}$, $V_{S} = 5 \text{ V to } 40 \text{ V}$ OPA2992SIRUGR, $V_{CM} = V_{-}$, $V_{S} = 5 \text{ V to } 40 \text{ V}$ OPA4992, $V_{CM} = V_{-}$, $V_{S} = 5 \text{ V to } 40 \text{ V}$ OPA4992, $V_{CM} = V_{-}$, $V_{S} = 5 \text{ V to } 40 \text{ V}$ OPA4992, $V_{CM} = V_{-}$, $V_{S} = 5 \text{ V to } 40 \text{ V}$ OPA4992, $V_{CM} = V_{-}$, $V_{S} = 5 \text{ V to } 40 \text{ V}$ Input bias current Input offset current Input voltage noise $V_{CM} = V_{-}$, V_{CM}	Input offset voltage versus power supply	OPA992, OPA2992, V _{CM} = V ₋ V _s = 5 V to 40 V	Input offset voltage versus power supply	DPA992_OPA2992_VCM



5.7 Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at T_A = 25°C, R_L = 10 k Ω connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

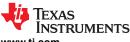
	PARAMETER	TEST CO	NDITIONS	MIN TYP	MAX	UNIT	
FREQUEN	CY RESPONSE						
GBW	Gain-bandwidth product			10.6		MHz	
SR	Slew rate	V _S = 40 V, G = +1, V _{STEP} = 10	32		V/µs		
		To 0.1%, V _S = 40 V, V _{STEP} = 1	0.65				
	0 - 441: 4:	To 0.1%, V _S = 40 V, V _{STEP} = 2	V, G = +1, C _L = 20 pF	0.3			
t _S	Settling time	To 0.01%, V _S = 40 V, V _{STEP} =	0.86		μs		
		To 0.01%, V _S = 40 V, V _{STEP} =	2 V, G = +1, C _L = 20 pF	0.44			
	Phase margin	$G = +1$, $R_L = 10$ kΩ, $C_L = 20$ pF		64		٥	
	Overload recovery time	V _{IN} × gain > V _S		170		ns	
		V _S = 40 V, V _O = 3 V _{RMS} , G = 1	0.00005%				
		$V_S = 40 \text{ V}, V_O = 3 \text{ V}_{RMS}, G = 1$, I = I KHZ, KL = 10 KΩ	126		dB	
THD+N	Total harmonic distortion +	V = 40 V V = 2 V C = 4					
I HD+N	noise	$V_S = 10 \text{ V}, V_O = 3 \text{ V}_{RMS}, G = 1, f = 1 \text{ kHz}, R_L = 128 \Omega$		90		dB	
		V _S = 10 V, V _O = 0.4 V _{RMS} , G =	4 f = 4 kH= D = 22 O	0.00032%			
		$V_S = 10 \text{ V}, V_O = 0.4 \text{ V}_{RMS}, G =$	$11, 1 = 1 \text{ KHZ}, R_L = 32 \Omega$	110		dB	
OUTPUT							
			V _S = 40 V, R _L = no load	7			
			V _S = 40 V, R _L = 10 kΩ	48	60		
	Voltage output swing from	Positive and negative	$V_S = 40 \text{ V}, R_L = 2 \text{ k}\Omega$	220	300	ma\ /	
	rail	rail headroom	V _S = 2.7 V, R _L = no load	0.5		mV	
			$V_S = 2.7 \text{ V}, R_L = 10 \text{ k}\Omega$	5	20		
			$V_S = 2.7 \text{ V}, R_L = 2 \text{ k}\Omega$	20	50		
I _{SC}	Short-circuit current			±65 ⁽³⁾		mA	
C _{LOAD}	Capacitive load drive			See Phase Margin vs Cap	acitive Load	pF	
Z _O	Open-loop output impedance	I _O = 0 A	See Open-Loop Output Im Frequency	Ω			
POWER SU	JPPLY			I	1		
		0040000 0044000 4 04		2.4	2.8		
	Quiescent current per	OPA2992, OPA4992, I _O = 0 A	T _A = -40°C to 125°C		2.84		
IQ	amplifier			2.48	2.92	mA	
		OPA992, I _O = 0 A	T _A = -40°C to 125°C		2.98		
SHUTDOW	'N				I		
I _{QSD}	Quiescent current per amplifier	V_S = 2.7 V to 40 V, all amplifie	rs disabled, SHDN = V- + 2 V	40	45	μА	
Z _{SHDN}	Output impedance during shutdown	$V_S = 2.7 \text{ V to } 40 \text{ V, amplifier di}$	10 2		GΩ pF		
V _{IH}	Logic high threshold voltage (amplifier disabled)	For valid input high, the SHDN than the maximum threshold b (V–) + 20 V, whichever is less	I pin voltage should be greater out less than or equal to V+ or		(V–) + 1.1 V	V	
V _{IL}	Logic low threshold voltage (amplifier enabled)	For valid input low, the SHDN the minimum threshold but gre	(V–) + 0.2 V		V		
t _{ON}	Amplifier enable time (from shutdown) (2)	V-	5		μs		
t _{OFF}	Amplifier disable time (2)	V _S = ±20 V, G = +1, V _{CM} = V _S V-	/ 2, R_L = 10 k Ω connected to	3		μs	
	SHDN pin input bias	V _S = 2.7 V to 40 V, (V–) + 20 V	/ ⁽⁴⁾ ≥ SHDN ≥ (V–) + 0.9 V	500			
	current (per pin)	V _S = 2.7 V to 40 V, (V–) ≤ SHE	400	nA			

⁽¹⁾ Specified by characterization only.

Submit Document Feedback

Copyright © 2024 Texas Instruments Incorporated

⁽²⁾ Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the SHDN pin and the point at which the output voltage reaches 10% (disable) or 90% (enable) of its final value.

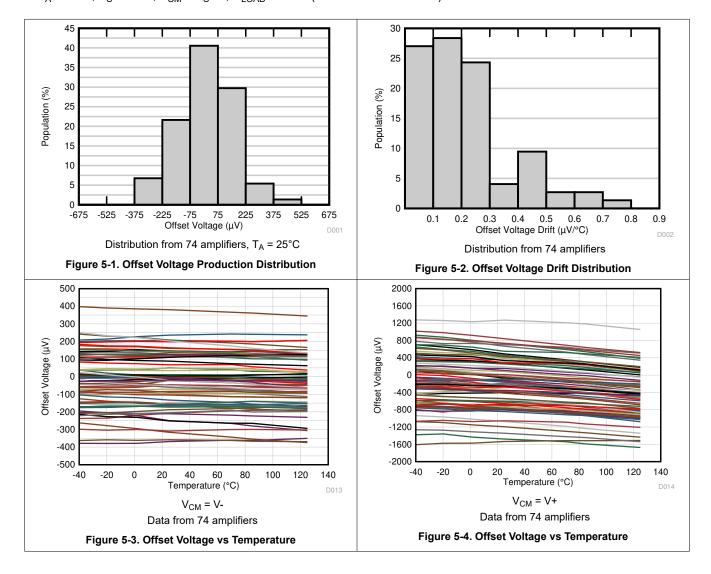


www.ti.com

- At high supply voltage, placing the OPAx992 in a sudden short to mid-supply or ground will lead to rapid thermal shutdown. Output current greater than I_{SC} can be achieved if rapid thermal shutdown is avoided as per Output Voltage Swing vs Output Current.
- SHDN pin should not exceed V+ or (V-) + 20 V, whichever is less.
- (5) See Slew Rate vs Input Step Voltage for more information.

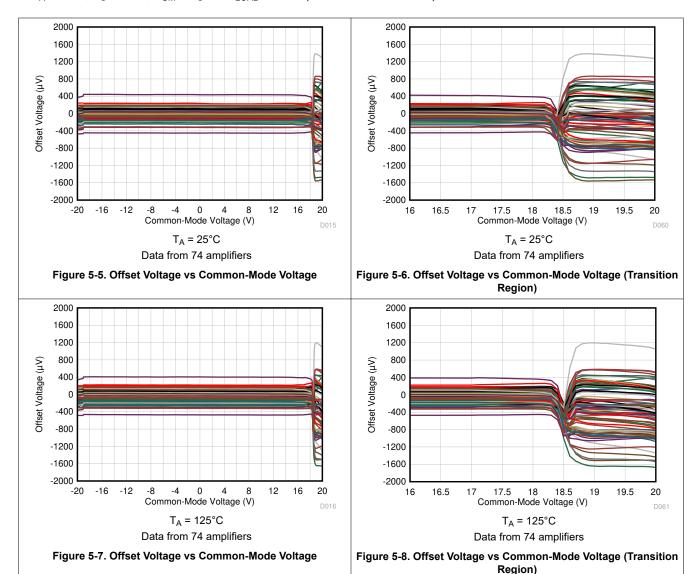
5.8 Typical Characteristics

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10k Ω (unless otherwise noted)



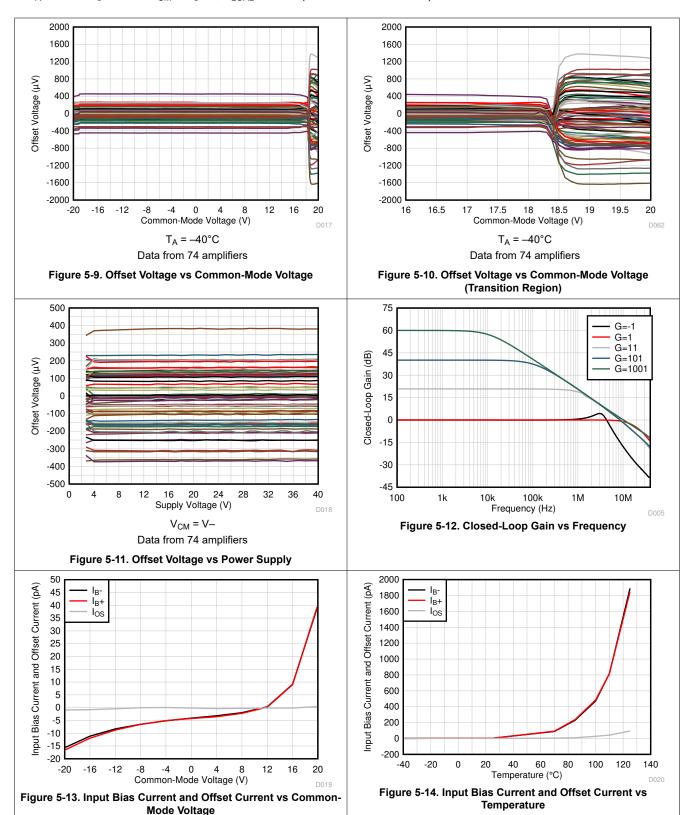


at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10k Ω (unless otherwise noted)



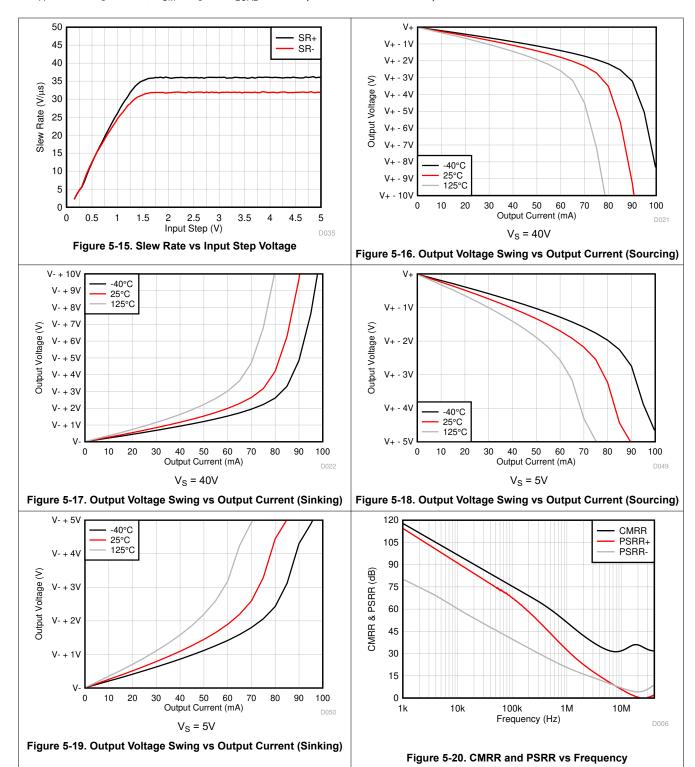


at $T_A = 25$ °C, $V_S = \pm 20$ V, $V_{CM} = V_S / 2$, $R_{LOAD} = 10$ k Ω (unless otherwise noted)



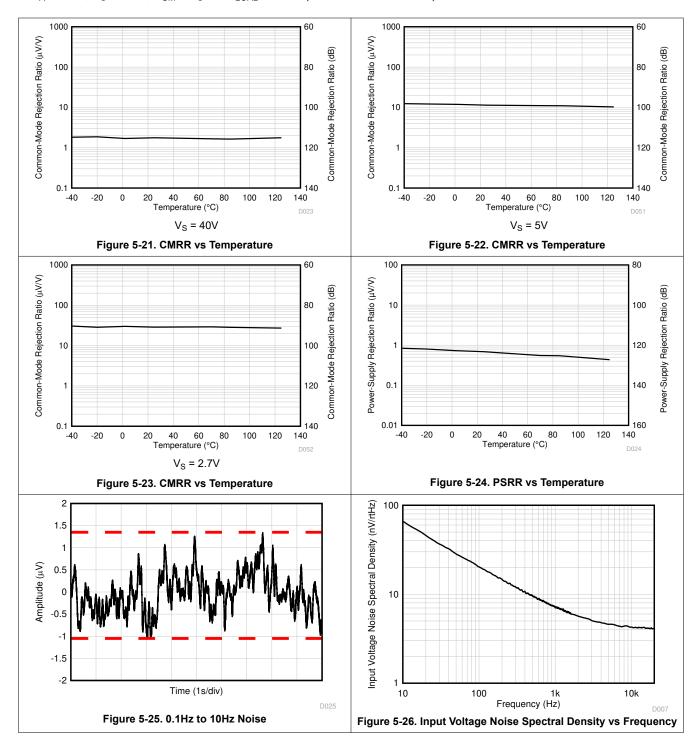


at $T_A = 25$ °C, $V_S = \pm 20$ V, $V_{CM} = V_S / 2$, $R_{LOAD} = 10$ k Ω (unless otherwise noted)



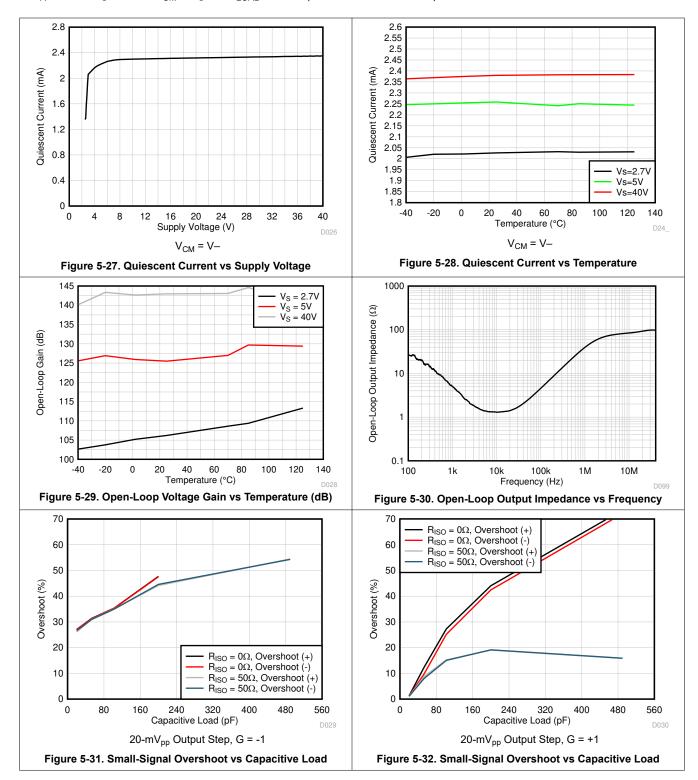


at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10k Ω (unless otherwise noted)



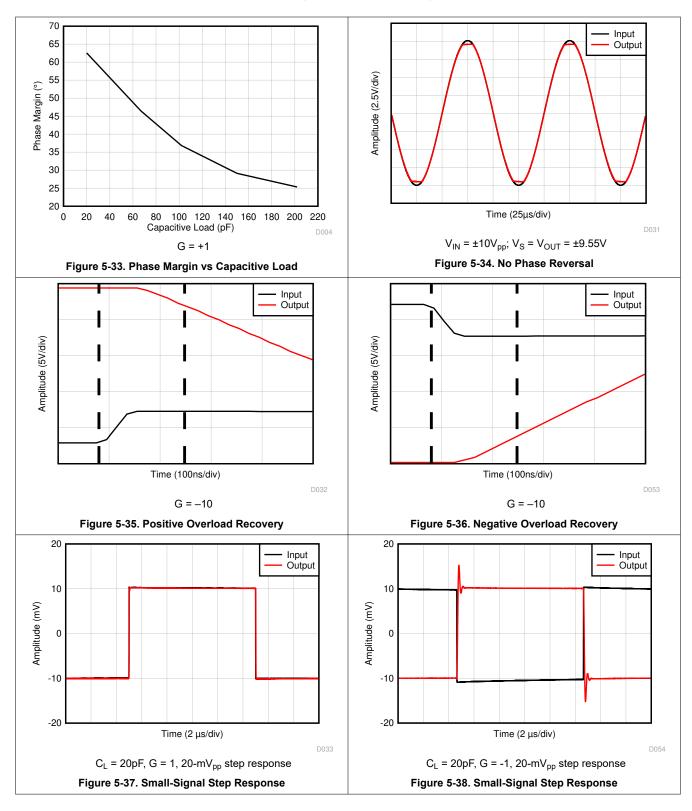


at $T_A = 25$ °C, $V_S = \pm 20$ V, $V_{CM} = V_S / 2$, $R_{LOAD} = 10$ k Ω (unless otherwise noted)



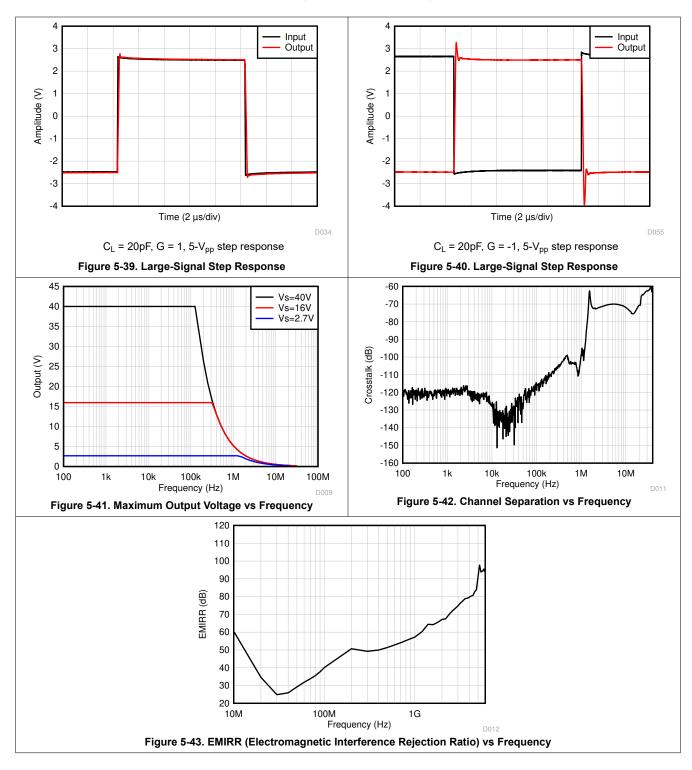


at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10k Ω (unless otherwise noted)





at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10k Ω (unless otherwise noted)





6 Detailed Description

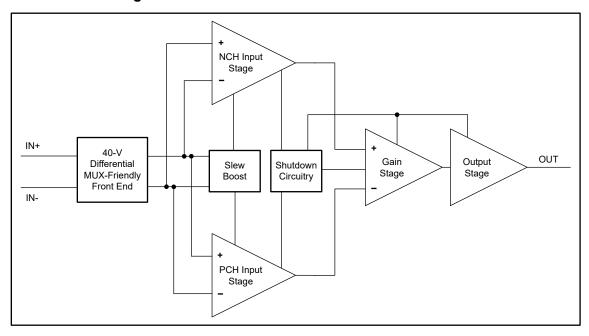
6.1 Overview

The OPAx992 family (OPA992, OPA2992, and OPA4992) is a family of high voltage (40V) general purpose operational amplifiers.

These devices offer excellent DC precision and AC performance, including rail-to-rail input/output, low offset $(\pm 210\mu V, typ)$, and low offset drift $(\pm 0.25\mu V)^{\circ}C$, typ).

Special features such as differential and common-mode input voltage range to the supply rail, high short-circuit current (±65mA), high slew rate (32V/µs), and shutdown make the OPAx992 an extremely flexible, robust, and high-performance operational amplifier for high-voltage industrial applications.

6.2 Functional Block Diagram





6.3 Feature Description

6.3.1 Input Protection Circuitry

The OPAx992 uses a special input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. Figure 6-1 shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 6-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time.

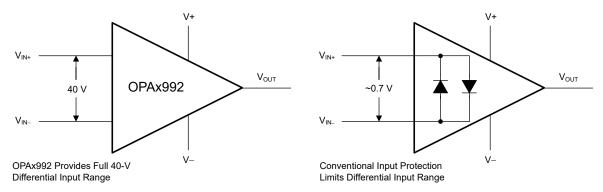


Figure 6-1. OPAx992 Input Protection Does Not Limit Differential Input Capability

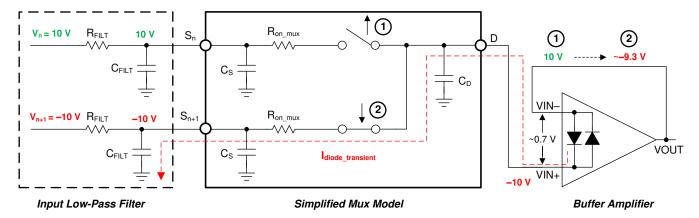


Figure 6-2. Back-to-Back Diodes Create Settling Issues

The OPAx992 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications using a patented input protection architecture that does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The OPAx992 tolerates a maximum differential swing (voltage between inverting and non-inverting pins of the op amp) of up to 40V, making the device suitable for use as a comparator or in applications with fast-ramping input signals such as data-acquisition systems; see the TI TechNote MUX-Friendly Precision Operational Amplifiers for more information.

6.3.2 EMI Rejection

The OPAx992 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx992 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. Figure 6-3 shows the results of this testing on the OPAx992. Table 6-1 shows the EMIRR IN+ values for the OPAx992 at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational*

Submit Document Feedback



Amplifiers application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

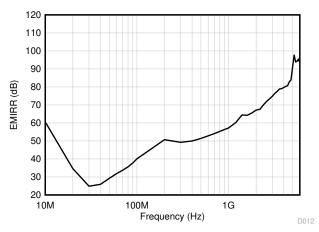


Figure 6-3. EMIRR Testing

Table 6-1. OPAx992 EMIRR IN+ For Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION				
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications				
900MHz	900MHz Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications				
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	65.6dB			
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	70.0dB			
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	78.9dB			
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	91.0dB			



6.3.3 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called self heating. The absolute maximum junction temperature of the OPAx992 is 150°C. Exceeding this temperature causes damage to the device. The OPAx992 has a thermal protection feature that reduces damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 170°C. Figure 6-4 shows an application example for the OPA2992 that has significant self heating because of its power dissipation (0.954 W). In this example, both channels have a quiescent power dissipation while one of the channels has a significant load. Thermal calculations indicate that for an ambient temperature of 55°C, the device junction temperature reaches 180°C. The actual device, however, turns off the output drive to recover towards a safe junction temperature. Figure 6-4 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3V. When self heating causes the device junction temperature to increase above the internal limit, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor R_I. If the condition that caused excessive power dissipation is not removed, the amplifier will oscillate between a shutdown and enabled state until the output fault is corrected. Please note that thermal performance can vary greatly depending on the package selected and the PCB layout design. This example uses the thermal performance of the SOIC (8) package.

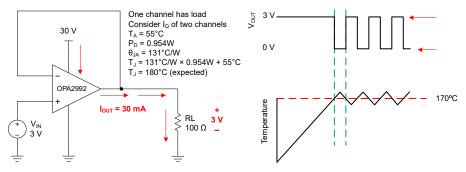


Figure 6-4. Thermal Protection

6.3.4 Capacitive Load and Stability

The OPAx992 features an output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive larger capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see Figure 6-5 and Figure 6-6. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

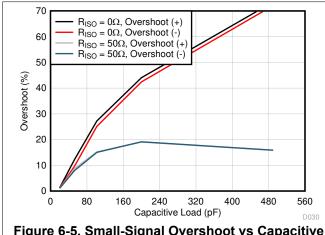


Figure 6-5. Small-Signal Overshoot vs Capacitive Load (20-mV_{pp} Output Step, G = +1)

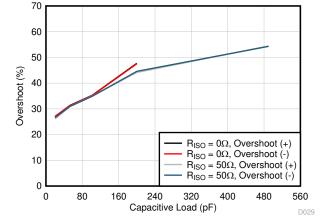


Figure 6-6. Small-Signal Overshoot vs Capacitive Load (20-mV_{pp} Output Step, G = -1)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small resistor, $R_{\rm ISO}$, in series with the output, as shown in Figure 6-7. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio $R_{\rm ISO}$ / $R_{\rm L}$, and is generally negligible at low output levels. A high capacitive load drive makes the OPAx992 well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in Figure 6-7 uses an isolation resistor, $R_{\rm ISO}$, to stabilize the output of an op amp. $R_{\rm ISO}$ modifies the open-loop gain of the system for increased phase margin.

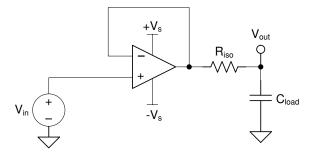


Figure 6-7. Extending Capacitive Load Drive With the OPA992

6.3.5 Common-Mode Voltage Range

The OPAx992 is a 40V, true rail-to-rail input operational amplifier with an input common-mode range that extends to both supply rails. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in Figure 6-8. The N-channel pair is active for input voltages close to the positive rail, typically from (V+) - 1V to the positive supply. The P-channel pair is active for inputs from the negative supply to approximately (V+) - 2V. There is a small transition region, typically (V+) - 2V to (V+) - 1V, in which both input pairs are on. This transition region can vary modestly with process variation. Within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

Figure 5-5 shows this transition region for a typical device in terms of input voltage offset in more detail.

For more information on common-mode voltage range and PMOS/NMOS pair interaction, see *Op Amps With Complementary-Pair Input Stages* application note.

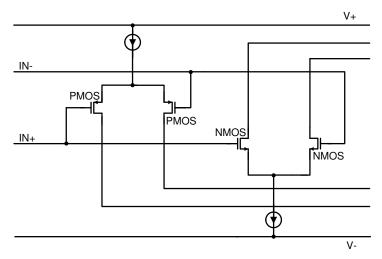


Figure 6-8. Rail-to-Rail Input Stage



6.3.6 Phase Reversal Protection

The OPAx992 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx992 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in Figure 6-9. For more information on phase reversal, see *Op Amps With Complementary-Pair Input Stages* application note.

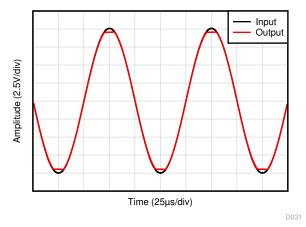


Figure 6-9. No Phase Reversal

Submit Document Feedback

Copyright © 2024 Texas Instruments Incorporated

6.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 6-10 shows an illustration of the ESD circuits contained in the OPAx992 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

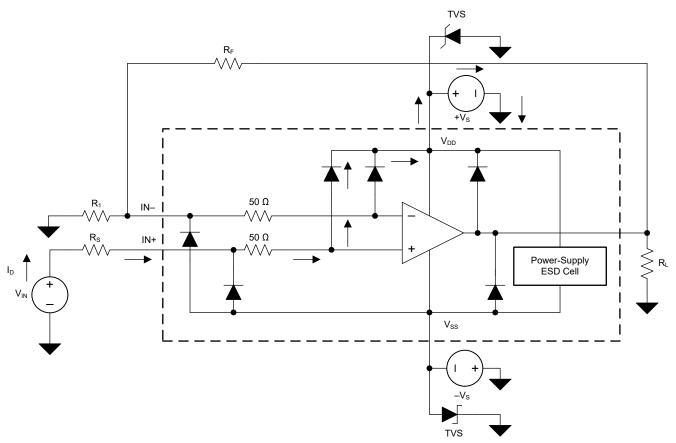


Figure 6-10. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example; 1 kV, 100ns), whereas an EOS event is long duration and lower voltage (for example; 50V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

6.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx992 is approximately 170ns.

6.3.9 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier in order to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* (*bell curve*), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in the *Electrical Characteristics* table.

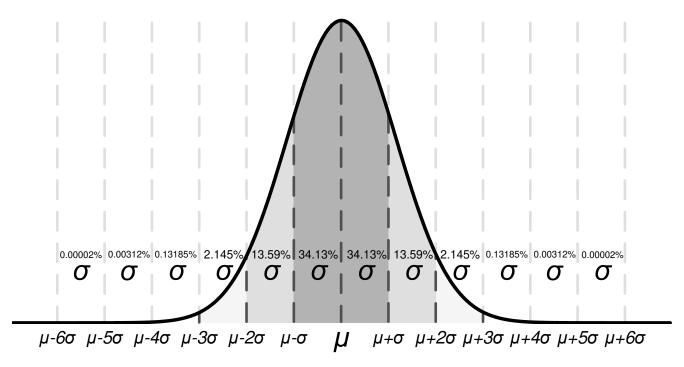


Figure 6-11. Ideal Gaussian Distribution

The Figure 6-11 figure shows an example distribution, where μ , or mu, is the mean of the distribution, and where σ , or sigma, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from μ – σ to μ + σ).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) in order to most accurately represent the typical value.

Use this chart to calculate approximate probability of a specification in a unit; for example, for OPAx992, the typical input voltage offset is $210\mu V$. So 68.2% of all OPAx992 devices are expected to have an offset from

 $-210\mu\text{V}$ to $+210\mu\text{V}$. At 4 σ ($\pm840\mu\text{V}$), 99.9937% of the distribution has an offset voltage less than $\pm840\mu\text{V}$, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are specified by design, and units outside these limits will be removed from production material. For example, the OPAx992 family has a maximum offset voltage of 1mV at 25°C, and even though this corresponds to slightly less than 5 σ (\approx 1 in 1.7 million units), which is extremely unlikely, any unit with larger offset than 1mV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for the application, and design worst-case conditions using this value. For example, the 6- σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guardband to design a system around. In this case, the OPAx992 family does not have a maximum or minimum for offset voltage drift. But based on the typical value of $0.25\mu\text{V/°C}$ in the *Electrical Characteristics* table, it can be calculated that the 6- σ value for offset voltage drift is about $1.5\mu\text{V/°C}$. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

Note that process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

6.3.10 Packages With an Exposed Thermal Pad

The OPAx992 family is available in the WSON-8 (DSG) package which features an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to V- or left floating. Attaching the thermal pad to a potential other than V- is not allowed, and performance of the device is not assured when doing so.

6.3.11 Shutdown

The OPAx992S devices feature one or more shutdown pins (SHDN) that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes about 40µA. The SHDN pins are active high, meaning that shutdown mode is enabled when the input to the SHDN pin is a valid logic high. The amplifier is enabled when the input to the SHDN pin is a valid logic low.

The SHDN pins are referenced to the negative supply rail of the op amp. The threshold of the shutdown feature lies around 800mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold for smooth switching characteristics. For optimal shutdown behavior, the SHDN pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V- and V- + 0.2V. A valid logic high is defined as a voltage between V- + 1.1V and V- + 20V. The shutdown pin circuitry includes a pull-down resistor, which will inherently pull the voltage of the pin to the negative supply rail if not driven. Thus, to enable the amplifier, the SHDN pins should either be left floating or driven to a valid logic low. To disable the amplifier, the SHDN pins must be driven to a valid logic high. The maximum voltage allowed at the SHDN pins is V- + 20V or V+, whichever is lower. Exceeding V- + 20V or V+, whichever is lower, will damage the device.

The SHDN pins are high-impedance CMOS inputs. Channels of single and dual op amp packages are independently controlled, and channels of quad op amp packages are controlled in pairs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The typical enable time out of shutdown is 15 μ s; disable time is 3 μ s. When disabled, the output assumes a high-impedance state. This architecture allows the OPAx992S family to operate as a gated amplifier, multiplexer, or programmable-gain amplifier. Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. For shutdown (disable) within a specific shutdown time, the specified 10k Ω load to V- is required. If using the OPAx992S without a load, the resulting turnoff time significantly increases.



6.4 Device Functional Modes

The OPAx992 has a single functional mode and is operational when the power-supply voltage is greater than or equal to 2.7V (±1.35V). The maximum power supply voltage for the OPAx992 is 40V (±20V).

The OPAx992S devices feature a shutdown pin, which can be used to place the op amp into a low-power mode.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx992 family offers excellent DC precision and AC performance. These devices operate up to 40V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 10.6MHz bandwidth and high output drive. These features make the OPAx992 a robust, high-performance operational amplifier for high-voltage industrial applications.

7.2 Typical Applications

7.2.1 Low-Side Current Measurement

Figure 7-1 shows the OPA992 configured in a low-side current sensing application. For a full analysis of the circuit shown in Figure 7-1 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0-A to 1-A Single-Supply Low-Side Current-Sensing Solution*.

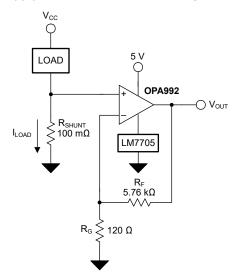


Figure 7-1. OPAx992 in a Low-Side, Current-Sensing Application

7.2.1.1 Design Requirements

The design requirements for this design are:

Load current: 0A to 1AMax output voltage: 4.9V

Maximum shunt voltage: 100mV

7.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 7-1 is given in Equation 1:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain$$
 (1)



The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is defined using Equation 2:

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100mV}{1A} = 100m\Omega$$
 (2)

Using Equation 2, R_{SHUNT} is calculated to be 100m Ω . The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the OPA992 to produce an output voltage of 0V to 4.9V. The gain needed by the OPA992 to produce the necessary output voltage is calculated using Equation 3:

$$Gain = \frac{\left(V_{OUT_MAX} - V_{OUT_MIN}\right)}{\left(V_{IN_MAX} - V_{IN_MIN}\right)}$$
(3)

Using Equation 3, the required gain is calculated to be 49V/V, which is set with resistors R_F and R_G . Equation 4 is used to size the resistors, R_F and R_G , to set the gain of the OPA992 to 49V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)}$$
(4)

Choosing R_F as 5.76k Ω , R_G is calculated to be 120 Ω . R_F and R_G were chosen as 5.76k Ω and 120 Ω because they are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. However, excessively large resistors will generate thermal noise that exceeds the intrinsic noise of the op amp. Figure 7-2 shows the measured transfer function of the circuit shown in Figure 7-1.

7.2.1.3 Application Curve

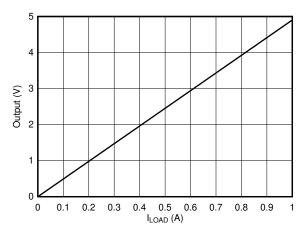


Figure 7-2. Low-Side, Current-Sense, Transfer Function

7.2.2 High Voltage Buffered Multiplexer

The OPAx992S shutdown devices can be configured to create a high voltage, buffered multiplexer. Outputs can be connected together on a common bus and the shutdown pins can be used to select the desired channel to pass through. Since the amplifier circuitry has been designed such that disable transitions occur significantly faster than enable transitions, the amplifier naturally exhibits a *break before make* switch topology. Amplifier outputs enter a high impedance state when placed in shutdown, so there is no risk of bus contention when connecting multiple channel outputs together. Additionally, because outputs are isolated from inputs, there is no concern about the impedance at the input of each channel interacting undesirably with the impedance at the output, like an amplifier gain stage or ADC driver circuit. Also, because this topology uses amplifiers instead of

Submit Document Feedback

Copyright © 2024 Texas Instruments Incorporated



MOSFET switches, other common issues with multiplexers such as charge injection or signal error due to R_{ON} effects are eliminated.

Figure 7-3 shows an example topology for a basic 2:1 multiplexer. When SEL is low, channel 1 is selected and active; when SEL is high, channel 2 is selected and active. For more information on how to use the OPAx992S shutdown function, see the shutdown section in Section 5.7.

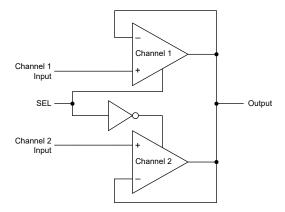


Figure 7-3. High Voltage Buffered Multiplexer

7.3 Power Supply Recommendations

The OPAx992 is specified for operation from 2.7V to 40V (±1.35V to ±20V); many specifications apply from –40°C to 125°C or with specific supply voltages and test conditions.

CAUTION

Supply voltages larger than 40V can permanently damage the device; see Section 5.1.

Place 0.1μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to Section 7.4.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself.
 Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for singlesupply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective
 methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes.
 A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital
 and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 7-5, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.



- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic
 package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to
 remove moisture introduced into the device packaging during the cleaning process. A low temperature, post
 cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

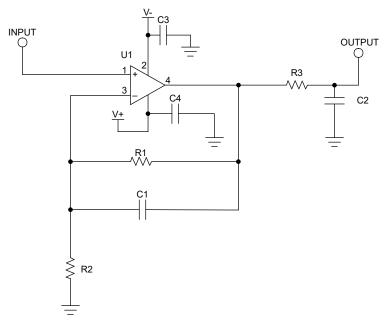


Figure 7-4. Schematic for Noninverting Configuration Layout Example

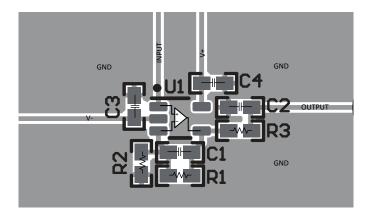


Figure 7-5. Operational Amplifier Board Layout for Noninverting Configuration - SC70 (DCK) Package

Submit Document Feedback

Copyright © 2024 Texas Instruments Incorporated



8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 TINA-TI[™] (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft[™]) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, MUX-Friendly, Precision Operational Amplifiers application brief
- Texas Instruments, EMI Rejection Ratio of Operational Amplifiers application report
- · Texas Instruments, Op Amps With Complementary-Pair Input Stages application note
- Texas Instruments, 0-1-A, Single-Supply, Low-Side, Current Sensing Solution reference design (TIPD129)

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TINA-TI™ is a trademark of Texas Instruments, Inc and DesignSoft, Inc.

TINA[™] and DesignSoft[™] are trademarks of DesignSoft, Inc.

TI E2E[™] is a trademark of Texas Instruments.

Bluetooth® is a registered trademark of Bluetooth SIG. Inc.

All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



8.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History NOTE: Page numbers for previous revisions may differ from page numbers in the current versions.	on
Changes from Revision E (January 2024) to Revision F (March 2024)	Page
 Changed the maximum PSRR (5V to 40V) for OPA2992SIRUGR from 1.3μV/V to 3.7μV/V 	
Changes from Revision D (August 2022) to Revision E (January 2024)	Page
Removed <i>Preview</i> comments for X2QFN (10) package	1 1
Changes from Revision C (March 2022) to Revision D (August 2022)	Page
 Added X2QFN (10) to Description with preview status. Added X2QFN (RUG) package to Pin Configuration and Functions with preview status. 	
Changes from Revision B (December 2021) to Revision C (March 2022)	Page
 Adjusted the typical CMRR value for V_S = 2.7 – 40 V, (V+) – 1 < V_{CM} < V+ (NMOS pair) from dB" in the <i>Electrical Characteristics</i> section	
 Adjusted the A_{OL} test condition from "V_S = 40 V, V_{CM} = V_S / 2, (V–) + 0.1 V < V_O < (V+) – 0 V, V_{CM} = V_S / 2, (V–) + 0.12 V < V_O < (V+) – 0.12 V" in the <i>Electrical Characteristics</i> section Adjusted the typical t_{ON} Amplifier Enable Time value from "15 μs" to "5 μs" in the <i>Electrical Characteristics</i> section. 	.1 V" to "V _S = 40
 Adjusted the typical SHDN pin input bias current value for V_S = 2.7 V to 40 V, (V−) ≤ SHDN from "150 nA" to "400 nA" in the Electrical Characteristics section 	≤ (V–) + 0.7 V
Removed "Open-Loop Gain and Phase vs Frequency" figure in <i>Typical Characteristics</i> sect	
Changes from Revision A (October 2021) to Revision B (December 2021)	Page
 Added PSRR specification for OPA4992 release in <i>Electrical Characteristics</i> section Added clarification to V_S = 2.7 V to 40 V PSRR specification noting that specification is for a channel variants	9
Changed y-axis from linear scale to logarithmic scale in "Input Voltage Noise Spectral Dens figure in Typical Characteristics section	
Corrected typo in <i>Shutdown</i> of <i>Feature Description</i> section from "specified 10kΩ load to n to "specified 10kΩ load to V-"	nidsupply (V_S / 2)"
Changes from Revision * (June 2021) to Revision A (October 2021)	
Changed the device status from Advance Information to Production Data	1

Submit Document Feedback



10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com

31-Oct-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
OPA2992IDDFR	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O92F
OPA2992IDDFR.A	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O92F
OPA2992IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2JUT
OPA2992IDGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2JUT
OPA2992IDR	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2992D
OPA2992IDR.A	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2992D
OPA2992IDRG4	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2992D
OPA2992IDRG4.A	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2992D
OPA2992IDSGR	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O92G
OPA2992IDSGR.A	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O92G
OPA2992IPWR	Active	Production	TSSOP (PW) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2992PW
OPA2992IPWR.A	Active	Production	TSSOP (PW) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2992PW
OPA2992SIRUGR	Active	Production	X2QFN (RUG) 10	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1N8
OPA2992SIRUGR.A	Active	Production	X2QFN (RUG) 10	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1N8
OPA4992IDR	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA4992D
OPA4992IDR.A	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA4992D
OPA4992IPWR	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O4992PW
OPA4992IPWR.A	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O4992PW
OPA992IDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	O92DB
OPA992IDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O92DB
OPA992IDCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1JS
OPA992IDCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1JS
OPA992SIDBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	O92SD
OPA992SIDBVR.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O92SD

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

PACKAGE OPTION ADDENDUM

www.ti.com 31-Oct-2025

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2992, OPA4992, OPA992:

Automotive: OPA2992-Q1, OPA4992-Q1, OPA992-Q1

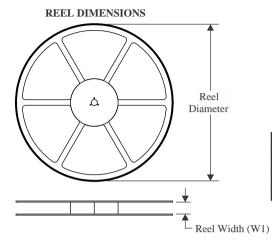
NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



www.ti.com 21-Aug-2025

TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2992IDDFR	SOT-23- THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2992IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2992IDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2992IDRG4	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2992IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA2992IPWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
OPA2992SIRUGR	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
OPA4992IDR	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4992IPWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA992IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA992SIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3



www.ti.com 21-Aug-2025



*All dimensions are nominal

7 til dilliciolorio are nominal								
Device	Package Type	Package Drawing	Pins SPQ		Length (mm)	Width (mm)	Height (mm)	
OPA2992IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0	
OPA2992IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0	
OPA2992IDR	SOIC	D	8	3000	353.0	353.0	32.0	
OPA2992IDRG4	SOIC	D	8	3000	353.0	353.0	32.0	
OPA2992IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0	
OPA2992IPWR	TSSOP	PW	8	3000	353.0	353.0	32.0	
OPA2992SIRUGR	X2QFN	RUG	10	3000	210.0	185.0	35.0	
OPA4992IDR	SOIC	D	14	3000	353.0	353.0	32.0	
OPA4992IPWR	TSSOP	PW	14	3000	353.0	353.0	32.0	
OPA992IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0	
OPA992SIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0	





- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



1.5 x 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





NOTES: All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
 C. QFN (Quad Flatpack No-Lead) package configuration.
 D. This package complies to JEDEC MO-288 variation X2EFD.



RUG (R-PQFP-N10)



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side





NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.





PLASTIC SMALL OUTLINE



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.



PLASTIC SMALL OUTLINE



- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC SMALL OUTLINE



- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 7. Board assembly site may have different recommendations for stencil design.







- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

- 4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- 5. Refernce JEDEC MO-178.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





PLASTIC SMALL OUTLINE - NO LEAD



- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC SMALL OUTLINE - NO LEAD



- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153, variation AA.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-187.





- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
- 9. Size of metal pad may vary due to creepage requirement.





- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025