













#### OPA325, OPA2325, OPA4325

SBOS637D -OCTOBER 2016-REVISED JUNE 2019

## OPAx325

# Precision, 10-MHz, Low-Noise, Low-Power, RRIO, CMOS Operational Amplifiers

#### 1 Features

· Precision with zero-crossover distortion:

Low offset voltage: 150 μV (maximum)

- High CMRR: 114 dB

- Rail-to-rail I/O

• Wide bandwidth: 10 MHz

Quiescent current: 650 μA/ch

Single-supply voltage range: 2.2 V to 5.5 V

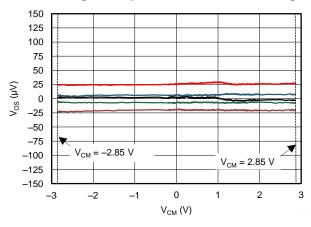
Low input bias current: 0.2 pA
 Low noise: 9 nV/\(\sqrt{Hz}\) at 10 kHz

Slew rate: 5 V/μsUnity-gain stable

#### 2 Applications

- · High-Z sensor signal conditioning
- Transimpedance amplifiers
- Test and measurement equipment
- Programmable logic controllers (PLCs)
- Motor control loops
- Communications
- · Input, output ADC, and DAC buffers
- Active filters

#### Offset Voltage vs Input Common-Mode Voltage



#### 3 Description

The OPA325, OPA2325, and OPA4325 (OPAx325) are precision, low-voltage complementary metal-oxide semiconductor (CMOS) operational amplifiers optimized for very low noise and wide bandwidth, while operating on a low quiescent current of only  $650~\mu\text{A}$ .

The OPAx325 feature a linear input stage with zerocrossover distortion that delivers excellent commonmode rejection ratio (CMRR) of typically 114 dB over the entire input range. The input common-mode range extends 100 mV beyond the negative and positive supply rails. The output voltage typically swings within 10 mV of the rails.

The zero-crossover distortion, combined with wide bandwidth (10 MHz), high slew rate (5 V/ $\mu$ s), and low noise (9 nV/ $\sqrt{Hz}$ ), make the OPAx325 a very good successive-approximation register (SAR) analog-to-digital converter (ADC) input driver amplifier. In addition, the OPAx325 have a wide supply-voltage range from 2.2 V to 5.5 V, with excellent power-supply rejection ratio (PSRR) over the entire supply range, making the device an excellent choice for precision, low-power applications that run directly from batteries without regulation.

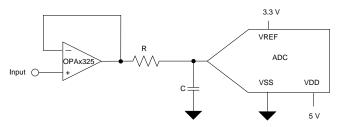
The OPA325 (single-channel version) is available in the SOT23-5 package. The OPA2325 (dual-channel version) is offered in SO-8 and MSOP-8 packages. The OPA4325 (quad-channel version) is available in TSSOP-14 package.

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE    | BODY SIZE (NOM)   |
|-------------|------------|-------------------|
| OPA325      | SOT-23 (5) | 2.90 mm × 1.60 mm |
| OPA2325     | SOIC (8)   | 4.90 mm × 3.91 mm |
| UPA2325     | VSSOP (8)  | 3.00 mm × 3.00 mm |
| OPA4325     | TSSOP (14) | 5.00 mm × 4.40 mm |

 For all available packages, see the package option addendum at the end of the data sheet.

#### The OPAx325 as an ADC Driver Amplifier





| 1 | Features 1   |    | 7.4 Device Functional Modes                          | . 18              |
|---|--|----|--|-------------------|
| 2 | Applications 1   | 8  | Application and Implementation                       | . 19              |
| 3 | Description 1  |    | 8.1 Application Information                          | . 19              |
| 4 | Revision History2  |    | 8.2 Typical Application                              | . 20              |
| 5 | Pin Configuration and Functions3   | 9  | Power Supply Recommendations                         | . 25              |
| 6 | Specifications5  | 10 | Layout   | . 25              |
| • | 6.1 Absolute Maximum Ratings   |    | 10.1 Layout Guidelines                               | . 25              |
|   | 6.2 ESD Ratings  |    | 10.2 Layout Example                                  | . 26              |
|   | 6.3 Recommended Operating Conditions                                       | 11 | Device and Documentation Support                     | . 27              |
|   | 6.4 Thermal Information: OPA325  |    | 11.1 Documentation Support                           | . 27              |
|   | 6.5 Thermal Information: OPA2325   |    | 11.2 Related Links                                   | . 27              |
|   | 6.6 Thermal Information: OPA4325   |    | 11.3 Receiving Notification of Documentation Updates | s <mark>27</mark> |
|   | 6.7 Electrical Characteristics: $V_S = 2.2 \text{ V to } 5.5 \text{ V or}$ |    | 11.4 Community Resources                             | . 27              |
|   | ±1.1 V to ±2.75 V  |    | 11.5 Trademarks                                      | . 27              |
|   | 6.8 Typical Characteristics9   |    | 11.6 Electrostatic Discharge Caution                 | . 27              |
| 7 | Detailed Description 16  |    | 11.7 Glossary  | . 27              |
|   | 7.1 Overview   | 12 | Mechanical, Packaging, and Orderable                 |                   |
|   | 7.2 Functional Block Diagram   |    | Information  | . 27              |
|   | 7.3 Feature Description  |    |  |                   |
|   |  |    |  |                   |

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

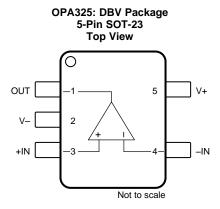
| Changes from Revision C (May 2019) to Revision D   | Page |
|--|------|
| Added OPA325 and associated content to data sheet  | 1    |
| Changes from Revision B (February 2019) to Revision C  | Page |
| Changed OPA4325 device status from preview to production data (active)   | 1    |
| Changes from Revision A (July 2017) to Revision B  | Page |
| Added OPA4325 advance information device to data sheet   | 1    |
| Added operating temperature to Absolute Maximum Ratings table  | 5    |
| Deleted specified temperature from Absolute Maximum Ratings table; specified temperature already listed in<br>Recommended Operating Conditions table |      |
| Changes from Original (October 2016) to Revision A   | Page |
| Added new VSSOP package option for dual-channel device   |      |
| Added top navigator icon for TI reference design   | 1    |

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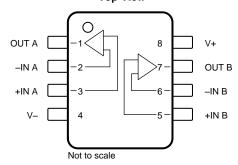
# 5 Pin Configuration and Functions



#### **Pin Functions: OPA325**

| PIN  |     | 1/0 | DESCRIPTION                     |  |
|------|-----|-----|---------------------------------|--|
| NAME | NO. | I/O | DESCRIPTION                     |  |
| -IN  | 4   | I   | Inverting input                 |  |
| +IN  | 3   | I   | Noninverting input              |  |
| OUT  | 1   | 0   | Output                          |  |
| V-   | 2   | _   | Negative (lowest) power supply  |  |
| V+   | 5   | _   | Positive (highest) power supply |  |

#### OPA2325: D and DGK Packages 8-Pin SOIC, 8-Pin VSSOP Top View

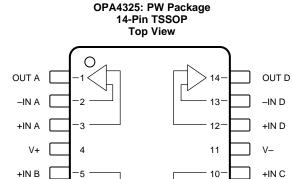


#### **Pin Functions: OPA2325**

| PIN   |     | 1/0 | DECORPTION                   |  |
|-------|-----|-----|------------------------------|--|
| NAME  | NO. | 1/0 | DESCRIPTION                  |  |
| -IN A | 2   |     | Inverting input channel A    |  |
| +IN A | 3   | ı   | Noninverting input channel A |  |
| –IN B | 6   | ı   | Inverting input channel B    |  |
| +IN B | 5   | ı   | Noninverting input channel B |  |
| OUT A | 1   | 0   | Output channel A             |  |
| OUT B | 7   | 0   | Output channel B             |  |
| V-    | 4   | _   | Negative supply              |  |
| V+    | 8   | _   | Positive supply              |  |

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#### **Pin Functions: OPA4325**

Not to scale

OUT B

-IN C OUT C

| Р     | IN  |     | DESCRIPTION                  |  |
|-------|-----|-----|------------------------------|--|
| NAME  | NO. | I/O |                              |  |
| -IN A | 2   | I   | Inverting input channel A    |  |
| +IN A | 3   | I   | Noninverting input channel A |  |
| –IN B | 6   | I   | Inverting input channel B    |  |
| +IN B | 5   | I   | Noninverting input channel B |  |
| -IN C | 9   | I   | Inverting input channel C    |  |
| +IN C | 10  | I   | Noninverting input channel C |  |
| –IN D | 13  | I   | Inverting input channel D    |  |
| +IN D | 12  | I   | Noninverting input channel D |  |
| OUT A | 1   | 0   | Output channel A             |  |
| OUT B | 7   | 0   | Output channel B             |  |
| OUT C | 8   | 0   | Output channel C             |  |
| OUT D | 14  | 0   | Output channel D             |  |
| V-    | 11  | _   | Negative supply              |  |
| V+    | 4   | _   | Positive supply              |  |



#### 6 Specifications

#### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                          |                                     | MIN        | MAX        | UNIT |
|--------------------------|-------------------------------------|------------|------------|------|
| Supply voltage           | $V_{S} = (V+) - (V-)$               |            | 6          | V    |
| Signal input pins        | Voltage <sup>(2)</sup>              | (V-) - 0.5 | (V+) + 0.5 | V    |
|                          | Current <sup>(2)</sup>              | -10        | 10         | mA   |
| Output short-circuit (3) | Output short-circuit <sup>(3)</sup> |            | S          | mA   |
|                          | Operating, T <sub>A</sub>           | -40        | 150        |      |
| Temperature              | Junction, T <sub>J</sub>            |            | 150        | °C   |
|                          | Storage, T <sub>stg</sub>           | -65        | 150        |      |

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### 6.2 ESD Ratings

|                      |                         |   | VALUE | UNIT |
|----------------------|-------------------------|---|-------|------|
| V <sub>(ESD)</sub> E | Clastrostatio discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>   | ±4000 |      |
|                      | Electrostatic discharge | Charged-device model (CDM), per JEDEC specification JESD22-C101 (2) | ±1000 | V    |

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

#### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                |                       |               | MIN  | NOM MAX | UNIT |
|----------------|-----------------------|---------------|------|---------|------|
| V <sub>S</sub> | Supply voltage        | Single supply | 2.2  | 5.5     | V    |
|                |                       | Dual supply   | ±1.1 | ±2.75   |      |
| T <sub>A</sub> | Specified temperature |               | -40  | 125     | °C   |

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<sup>(2)</sup> Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.

<sup>(3)</sup> Short-circuit to ground, one amplifier per package.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



#### 6.4 Thermal Information: OPA325

|                      |  | OPA325    |      |
|----------------------|--|-----------|------|
|                      | THERMAL METRIC <sup>(1)</sup>                | DBV (SOT) | UNIT |
|                      |  | 5 PINS    |      |
| $R_{\theta JA}$      | Junction-to-ambient thermal resistance       | 205       | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance    | 200       | °C/W |
| $R_{\theta JB}$      | Junction-to-board thermal resistance         | 113       | °C/W |
| $\Psi_{JT}$          | Junction-to-top characterization parameter   | 38.2      | °C/W |
| $\Psi_{JB}$          | Junction-to-board characterization parameter | 104.9     | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A       | °C/W |

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

#### 6.5 Thermal Information: OPA2325

|                      |  | OP       | OPA2325     |      |  |
|----------------------|--|----------|-------------|------|--|
|                      | THERMAL METRIC <sup>(1)</sup>                | D (SOIC) | DGK (VSSOP) | UNIT |  |
|                      |  | 8 PINS   | 8 PINS      |      |  |
| $R_{\theta JA}$      | Junction-to-ambient thermal resistance       | 119      | 143         | °C/W |  |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance    | 60       | 47          | °C/W |  |
| $R_{\theta JB}$      | Junction-to-board thermal resistance         | 61       | 64          | °C/W |  |
| $\Psi_{\text{JT}}$   | Junction-to-top characterization parameter   | 15.0     | 5.3         | °C/W |  |
| $\Psi_{JB}$          | Junction-to-board characterization parameter | 60.4     | 62.8        | °C/W |  |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A      | N/A         | °C/W |  |

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

#### 6.6 Thermal Information: OPA4325

|                      |  | OPA4325    |      |
|----------------------|--|------------|------|
|                      | THERMAL METRIC <sup>(1)</sup>                | PW (TSSOP) | UNIT |
|                      |  | 14 PINS    |      |
| $R_{\theta JA}$      | Junction-to-ambient thermal resistance       | 93         | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance    | 28         | °C/W |
| $R_{\theta JB}$      | Junction-to-board thermal resistance         | 34         | °C/W |
| $\Psi_{JT}$          | Junction-to-top characterization parameter   | 1.9        | °C/W |
| $\Psi_{JB}$          | Junction-to-board characterization parameter | 33.1       | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A        | °C/W |

 For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.



## 6.7 Electrical Characteristics: $V_s = 2.2 \text{ V}$ to 5.5 V or ±1.1 V to ±2.75 V

at T\_A = 25°C, R\_L = 10 k $\Omega$  connected to V\_S / 2, V\_{CM} = V\_S / 2, and V\_{OUT} = V\_S / 2 (unless otherwise noted)

|                      | PARAMETER  | TEST CONDITIONS  | MIN        | TYP    | MAX        | UNIT               |
|----------------------|--|--|------------|--------|------------|--------------------|
| OFFSET V             | /OLTAGE  |  |            |        |            |                    |
| Vos                  | Input offset voltage   |  |            | 40     | 150        | μV                 |
| dV <sub>OS</sub> /dT | Input offset voltage drift   | $V_S = 5.5 \text{ V}, T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$  |            | 2      | 7.5        | μV/°C              |
| DCDD                 | Daniel de la companie | V <sub>S</sub> = 2.2 V to +5.5 V   |            | 6      | 20         | \/\/               |
| PSRR                 | Power-supply rejection ratio   | $V_S = 2.2 \text{ V to } 5.5 \text{ V}, T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$  |            | 15     |            | μV/V               |
|                      | Channel separation   | At 1 kHz   |            | 130    |            | dB                 |
| INPUT VO             | LTAGE  |  |            |        |            |                    |
| V <sub>CM</sub>      | Common-mode voltage range  |  | (V-) - 0.1 |        | (V+) + 0.1 | V                  |
|                      | Common and a selection and   | $V_S = 5.5 \text{ V}, (V-) - 0.1 \text{ V} < V_{CM} < (V+) + 0.1 \text{ V}$  | 100        | 114    |            | -10                |
| CMRR                 | RR Common-mode rejection ratio   | $T_A = -40$ °C to +125°C   | 95         |        |            | dB                 |
| INPUT BIA            | AS CURRENT   |  |            |        |            |                    |
|                      |  |  |            | ±0.2   | ±10        | - ^                |
| I <sub>B</sub>       | B Input bias current   | $T_A = -40$ °C to +85°C  |            |        | ±500       | pА                 |
|                      |  | $T_A = -40$ °C to +125°C   |            |        | ±10        | nA                 |
|                      |  |  |            | ±0.2   | ±10        |                    |
| los                  | Input offset current   | $T_A = -40$ °C to +85°C  |            |        | ±500       | pА                 |
|                      |  | $T_A = -40$ °C to +125°C   |            |        | ±10        | nA                 |
| NOISE                |  |  |            |        |            |                    |
|                      | Input voltage noise  | f = 0.1 Hz to 10 Hz  |            | 2.8    |            | $\mu V_{PP}$       |
|                      | e <sub>n</sub> Input voltage noise density   | f = 1 kHz  |            | 10     |            | \                  |
| e <sub>n</sub>       |  | f = 10 kHz   |            | 9      |            | nV/√Hz             |
| i <sub>n</sub>       | Input current noise density  | f = 1 kHz  |            | 1.3    |            | fA/√ <del>Hz</del> |
| INPUT CA             | PACITANCE  |  |            |        |            |                    |
|                      | Differential   |  |            | 5      |            | pF                 |
|                      | Common-mode  |  |            | 4      |            | pF                 |
| OPEN-LO              | OP GAIN  |  |            |        |            |                    |
|                      |  | $0.1 \text{ V} < \text{V}_{\text{O}} < (\text{V+}) - 0.1 \text{ V}, \text{R}_{\text{L}} = 10 \text{ k}\Omega$  | 105        | 130    |            |                    |
| A <sub>OL</sub>      | Open-loop voltage gain   | $0.1 \text{ V} < \text{V}_{\text{O}} < (\text{V+}) - 0.1 \text{ V}, \text{ R}_{\text{L}} = 10 \text{ k}\Omega,$ $\text{T}_{\text{A}} = -40^{\circ}\text{C} \text{ to } +125^{\circ}\text{C}$ | 95         | 128    |            | dB                 |
|                      |  | $0.2 \text{ V} < \text{V}_{\text{O}} < (\text{V+}) - 0.2 \text{ V}, \text{ R}_{\text{L}} = 2 \text{ k}\Omega$  | 100        | 110    |            |                    |
| PM                   | Phase margin   | G = 1 V/V, V <sub>S</sub> = 5 V, C <sub>L</sub> = 15 pF  |            | 67     |            | Degrees            |
| FREQUEN              | ICY RESPONSE (V <sub>S</sub> = 5.0 V, C <sub>L</sub> = 50 pF)  |  |            |        |            |                    |
| GBP                  | Gain bandwidth product   | Unity gain   |            | 10     |            | MHz                |
| SR                   | Slew rate  | G = +1   |            | 5      |            | V/μs               |
|                      | 0  | To 0.1%, 2-V step, G = +1  | 0.6        |        |            |                    |
| t <sub>S</sub>       | Settling time  | To 0.01%, 2-V step, G = +1   | 1          |        |            | μs                 |
|                      | Overload recovery time   | $V_{IN} \times G > V_{S}$  |            | 200    |            | ns                 |
|                      |  | $V_{O} = 4 V_{PP}, G = +1, f = 10 \text{ kHz}, R_{L} = 10 \text{ k}\Omega$   | 0.0005%    |        |            |                    |
| THD+N                | Total harmonic distortion + noise <sup>(1)</sup>   | $V_{O} = 2 V_{PP}, G = +1, f = 10 \text{ kHz}, R_{L} = 600 \Omega$   |            | 0.005% |            |                    |

<sup>(1)</sup> Third-order filter; bandwidth = 80 kHz at −3 dB.



## Electrical Characteristics: $V_S = 2.2 \text{ V}$ to 5.5 V or ±1.1 V to ±2.75 V (continued)

at  $T_A$  = 25°C,  $R_L$  = 10 k $\Omega$  connected to  $V_S$  / 2,  $V_{CM}$  =  $V_S$  / 2, and  $V_{OUT}$  =  $V_S$  / 2 (unless otherwise noted)

| PARAMETER       |                                      | TEST CONDITIONS  | MIN                             | TYP  | MAX     | UNIT |
|-----------------|--------------------------------------|--|---------------------------------|------|---------|------|
| OUTPU           | Т                                    |  |                                 |      |         |      |
|                 |                                      | $R_L = 10 \text{ k}\Omega$   |                                 | 10   | 20      |      |
| W               | Voltage output swing from both rails | $R_L = 10 \text{ k}\Omega, T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$ |                                 |      | 30      | mV   |
| Vo              | voltage output swing from both rails | $R_L = 2 \text{ k}\Omega$  |                                 |      |         |      |
|                 |                                      | $R_L = 2 \text{ k}\Omega$ , $T_A = -40^{\circ}\text{C}$ to +125°C              |                                 |      | 55      |      |
| I <sub>SC</sub> | Short-circuit current                | V <sub>S</sub> = 5.5 V   | See the Typical Characteristics |      |         | mA   |
| $C_L$           | Capacitive load drive                |  | See the Typical Characteristics |      | ristics |      |
| $R_{O}$         | Open-loop output resistance          | $I_O = 0$ mA, $f = 1$ MHz  | 180                             |      |         | Ω    |
| POWER           | RSUPPLY                              |  |                                 |      |         |      |
|                 | Ouissent surrent per amplifier       | $I_{O} = 0 \text{ mA}, V_{S} = 5.5 \text{ V}$                                  |                                 | 0.65 | 0.75    | A    |
| IQ              | Quiescent current per amplifier      | $I_{O} = 0$ mA, $V_{S} = 5.5$ V, $T_{A} = -40$ °C to +125°C                    | 0.8                             |      |         | mA   |
|                 | Power-on time                        | V+ = 0 V to 5 V, to 90% I <sub>Q</sub> level                                   |                                 | 28   |         | μs   |

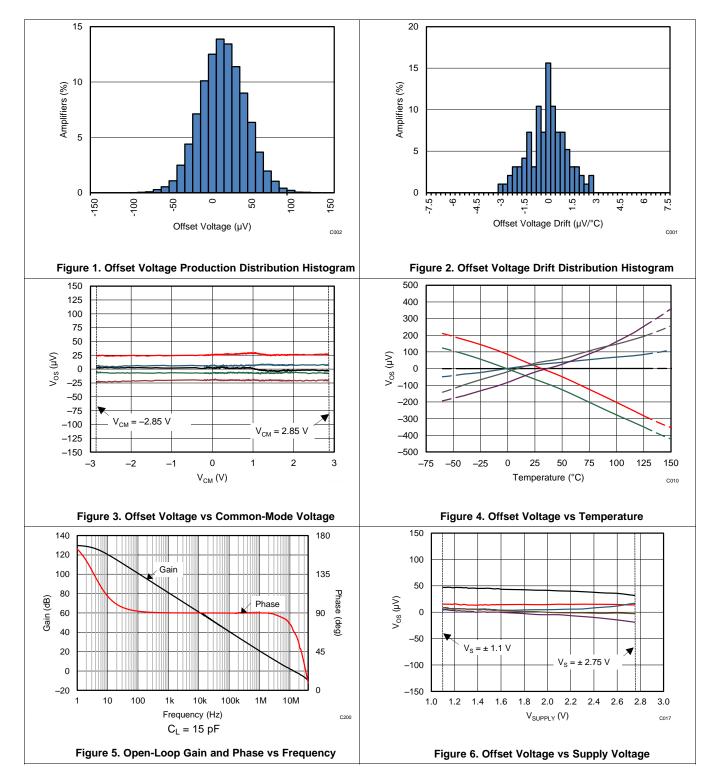
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#### 6.8 Typical Characteristics

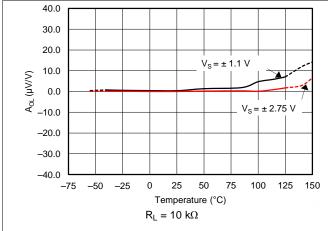
at  $T_A$  = 25°C,  $V_{CM}$  =  $V_{OUT}$  = midsupply, and  $R_L$  = 10  $k\Omega$  (unless otherwise noted)



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#### **Typical Characteristics (continued)**

at  $T_A = 25$ °C,  $V_{CM} = V_{OUT} = midsupply$ , and  $R_L = 10 \text{ k}\Omega$  (unless otherwise noted)



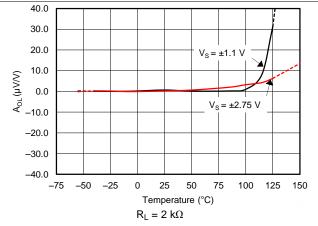
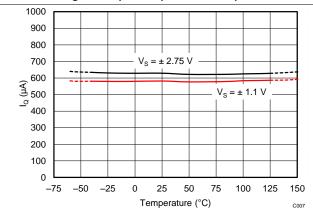


Figure 7. Open-Loop Gain vs Temperature

Figure 8. Open-Loop Gain vs Temperature



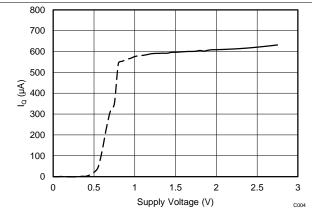


Figure 9. Quiescent Current vs Temperature

Figure 10. Quiescent Current vs Supply Voltage

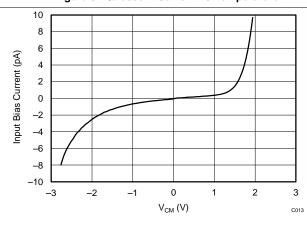


Figure 11. Input Bias Current vs Common-Mode Voltage

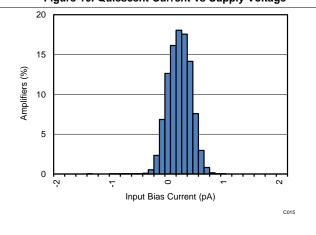
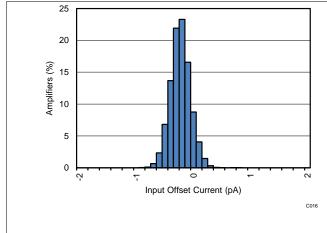


Figure 12. Input Bias Current Distribution Histogram



#### **Typical Characteristics (continued)**

at  $T_A$  = 25°C,  $V_{CM}$  =  $V_{OUT}$  = midsupply, and  $R_L$  = 10 k $\Omega$  (unless otherwise noted)



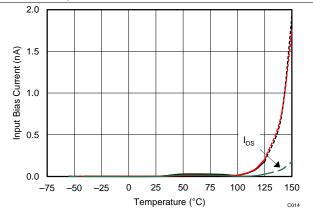
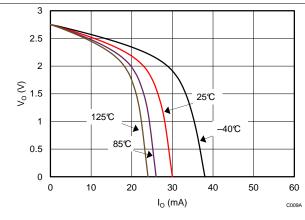


Figure 13. Input Offset Current Distribution Histogram

Figure 14. Input Bias Current vs Temperature



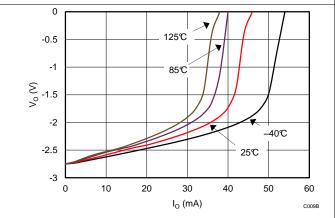
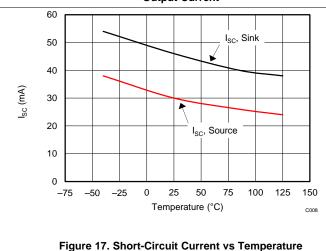


Figure 15. Output Voltage Swing (Positive) vs Output Current

Figure 16. Output Voltage Swing (Negative) vs Output Current



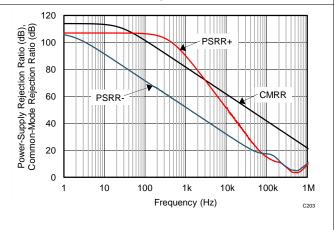
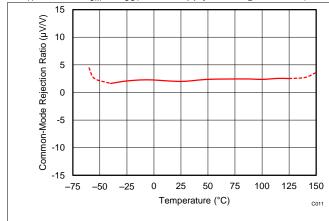


Figure 18. CMRR and PSRR vs Frequency

# TEXAS INSTRUMENTS

#### **Typical Characteristics (continued)**

at  $T_A = 25$ °C,  $V_{CM} = V_{OUT} = midsupply$ , and  $R_L = 10 \text{ k}\Omega$  (unless otherwise noted)



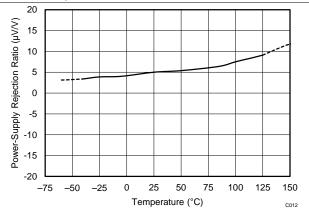
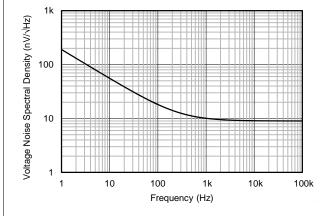


Figure 19. CMRR vs Temperature

Figure 20. PSRR vs Temperature



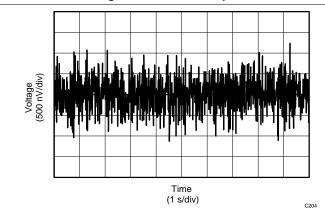
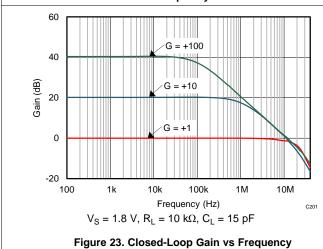
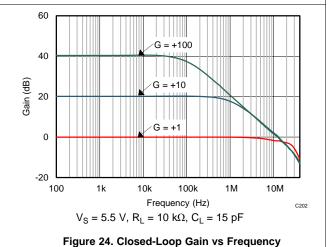


Figure 21. Input Voltage Noise Spectral Density vs Frequency

Figure 22. 0.1-Hz to 10-Hz Input Voltage Noise

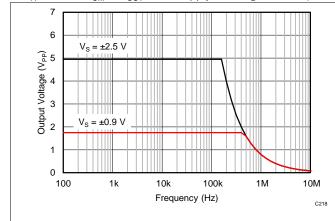






#### **Typical Characteristics (continued)**

at  $T_A = 25$ °C,  $V_{CM} = V_{OUT} = midsupply$ , and  $R_L = 10 \text{ k}\Omega$  (unless otherwise noted)



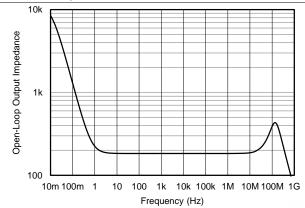
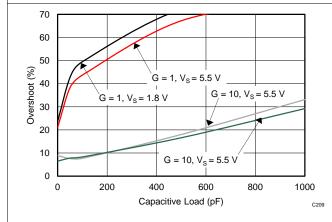


Figure 25. Maximum Output Voltage vs Frequency

Figure 26. Open-Loop Output Impedance vs Frequency



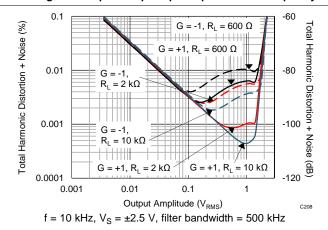
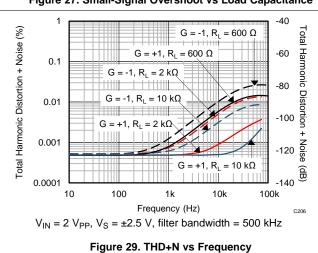


Figure 27. Small-Signal Overshoot vs Load Capacitance





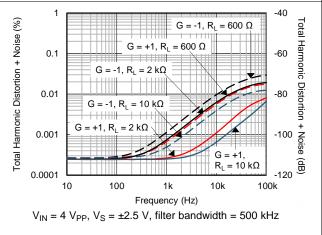
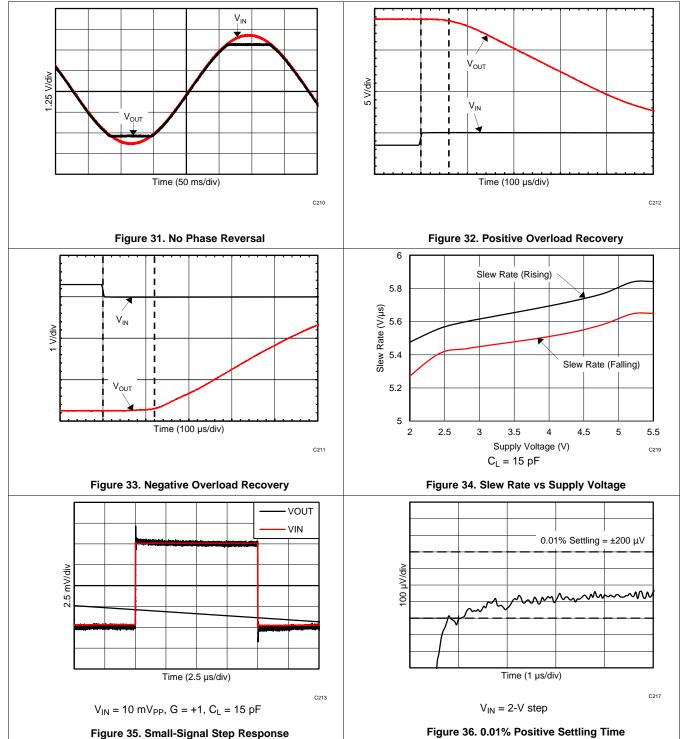


Figure 30. THD+N vs Frequency

# TEXAS INSTRUMENTS

#### **Typical Characteristics (continued)**

at  $T_A$  = 25°C,  $V_{CM}$  =  $V_{OUT}$  = midsupply, and  $R_L$  = 10  $k\Omega$  (unless otherwise noted)





#### **Typical Characteristics (continued)**

at  $T_A$  = 25°C,  $V_{CM}$  =  $V_{OUT}$  = midsupply, and  $R_L$  = 10  $k\Omega$  (unless otherwise noted)

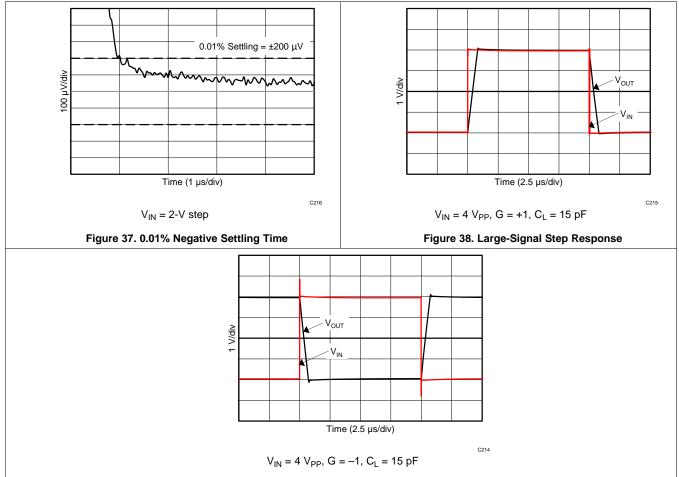


Figure 39. Large-Signal Step Response

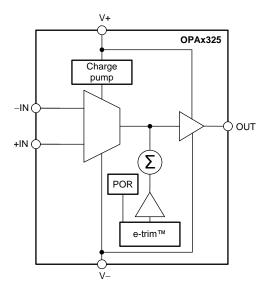


#### 7 Detailed Description

#### 7.1 Overview

The OPA325, OPA2325, and OPA4325 (OPAx325) belong to a new generation of low-noise, e-trim™ operational amplifiers that provide outstanding dc precision. The OPAx325 also have a highly linear input stage with zero-crossover distortion that delivers excellent CMRR and distortion performance across the full rail-to-rail input range. In addition, this device has a wide supply range with excellent PSRR. This feature, combined with low quiescent current, makes the OPAx325 an excellent choice for applications that are battery-powered without regulation.

#### 7.2 Functional Block Diagram





#### 7.3 Feature Description

#### 7.3.1 Zero-Crossover Input Stage

Traditional complementary metal-oxide semiconductor (CMOS) rail-to-rail input amplifiers use a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. This configuration results in sudden change in offset voltage when the input stage transitions from the p-channel metal-oxide-semiconductor field effect transistor (PMOS) to the n-type field effect transistor (NMOS), or vice-versa, as shown in Figure 40. This transition results in significant degradation of CMRR and PSRR performance of the amplifier.

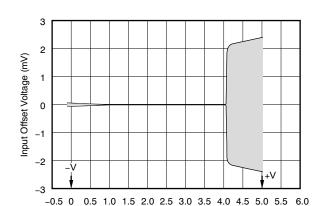


Figure 40. Input Common-Mode Voltage vs Input Offset Voltage (Traditional Rail-to-Rail Input CMOS Amplifiers)

Input Common-Mode Voltage (V)

The OPAx325 series of amplifiers includes an internal charge pump that powers the amplifier input stage with an internal supply rail that is higher than the external power supply. The internal supply rail allows a single differential pair to operate and to be linear across the entire input common-mode voltage range, thus eliminating crossover distortion. Rail-to-rail amplifiers that use this technique to eliminate crossover distortion are called *zero-crossover amplifiers*.

The single differential pair combined with the charge pump allows the OPAx325 to provide superior CMRR across the entire common-mode input range, which extends 100 mV beyond both power-supply rails. Figure 41 shows the input offset voltage versus input common-mode voltage plot for the OPAx325. Note that unlike traditional rail-to-rail CMOS amplifiers, there is no transition region for the OPAx325.

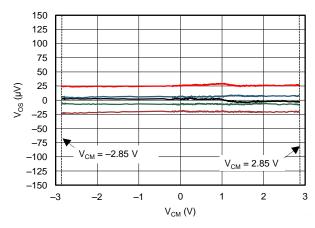


Figure 41. Offset Voltage vs Common-Mode Voltage (Zero-Crossover)

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#### **Feature Description (continued)**

#### 7.3.2 Low Input Offset Voltage

The OPAx325 are manufactured using TI's e-trim technology. Each amplifier is trimmed in production, thereby minimizing errors associated with input offset voltage. The e-trim technology is a TI proprietary method of trimming internal device parameters during either wafer probing or final testing. This process allows the OPAx325 to have an excellent offset specification of 150  $\mu$ V (maximum). Figure 42 shows the offset voltage distribution for the OPAx325.

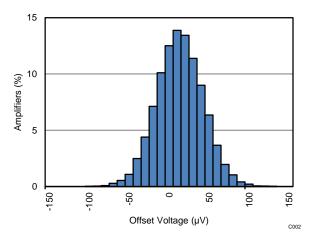
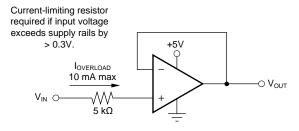


Figure 42. Offset Voltage Distribution

#### 7.3.3 Input and ESD Protection

The OPAx325 incorporate internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings* table. Figure 43 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input; thus, keep the value to a minimum in noise-sensitive applications.



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#### 7.4 Device Functional Modes

The OPAx325 have a single functional mode and are operational when the power-supply voltage is greater than 2.2 V (±1.1 V). The maximum power-supply voltage for the OPAx325 is 5.5 V (±2.75 V).

Figure 43. Input Current Protection



#### 8 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

#### 8.1 Application Information

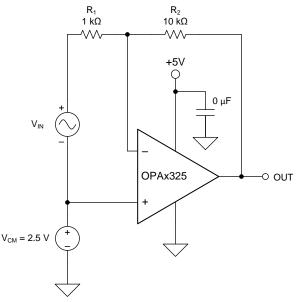
The OPAx325 series features e-trim, a proprietary technique in which the offset voltage is adjusted during the final steps of manufacturing. As a result, the OPAx325 deliver excellent offset voltage (40  $\mu$ V, typical). Additionally, the amplifier boasts a fast slew rate, low drift, low noise, and excellent PSRR and A<sub>OL</sub>. The OPAx325 also feature a linear input stage with zero-crossover distortion, resulting in excellent CMRR over the entire input range, which extends from 100 mV below the negative rail to 100 mV above the positive rail.

#### 8.1.1 Operating Characteristics

The OPAx325 family of amplifiers has parameters that are fully specified from 2.2 V to 5.5 V ( $\pm$ 1.1 V to  $\pm$ 2.75 V). Many of the specifications apply from  $-40^{\circ}$ C to  $\pm$ 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

#### 8.1.2 Basic Amplifier Configurations

The OPAx325 are unity-gain stable. The devices do not exhibit output phase inversion when the input is overdriven. A typical single-supply connection is shown in Figure 44. The OPAx325 are configured as a basic inverting amplifier with a gain of -10 V/V. This single-supply connection has an output centered on the common-mode voltage,  $V_{CM}$ . For the circuit shown, this voltage is 2.5 V, but can be any value within the common-mode input voltage range.



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Figure 44. Basic Single-Supply Connection



#### **Application Information (continued)**

#### 8.1.3 Driving an Analog-to-Digital Converter

The low-noise and wide-gain bandwidth of the OPAx325, combined with rail-to-rail input/output and zero-crossover distortion, make these devices an excellent input driver for ADCs. Figure 45 shows the OPAx325 driving an ADC. The amplifier is connected as a unity-gain, noninverting buffer.

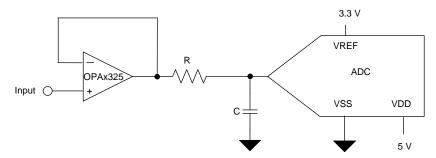


Figure 45. The OPAx325 as an Input Driver for ADCs

#### 8.2 Typical Application

Operational amplifiers are commonly used as unity-gain buffers. Figure 46 shows the schematic for an amplifier configured as a unity-gain buffer. If the input signal range to the amplifier is very close to the rails or includes the rails, a rail-to-rail amplifier must be used. However, regular rail-to-rail amplifiers introduce significant distortion to the signal. This design compares the distortion introduced by a typical CMOS input amplifier with that of the OPAx325 (a zero-crossover amplifier).

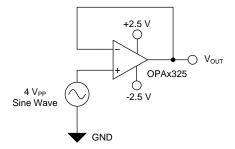


Figure 46. The OPAx325 Configured as a Unity-Gain Buffer Amplifier

#### 8.2.1 Design Requirements

The following parameters are used for this design example:

- Gain = +1 V/V (inverting gain)
- V+ = 2.5 V, V- = -2.5 V
- Input signal = 4 V<sub>PP</sub>, f = 1-kHz sine wave



#### 8.2.2 Detailed Design Procedure

Traditional CMOS rail-to-rail input amplifiers use a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in Figure 47.

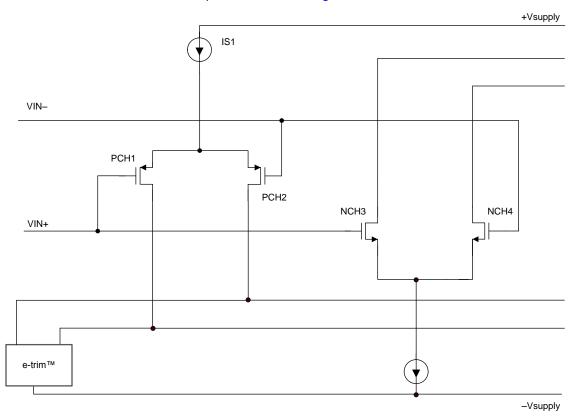


Figure 47. Complementary Input Stage (Traditional Rail-to-Rail Input CMOS Amplifiers)



The N-channel pair is active for input voltages close to the positive rail, typically (V+) - 1 V to 200 mV above the positive supply, and the P-channel pair is on for inputs from 200 mV below the negative supply to approximately (V+) - 1 V. There is a small transition region, typically (V+) - 1.1 V to (V+) - 0.9 V, in which both pairs are on. This transition region is shown in Figure 48 for a traditional rail-to-rail input CMOS amplifier. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded when compared to device operation outside of this region.

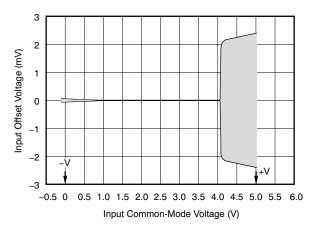


Figure 48. Input Offset Voltage vs Common-Mode Voltage (For Traditional Rail-to-Rail Input CMOS Amplifiers)

The OPAx325 amplifiers include an internal charge pump that powers the amplifier input stage with an internal supply rail that is higher than the external power supply. The internal supply rail allows a single differential pair to operate and to be linear across the entire input common-mode voltage range, as shown in Table 1.

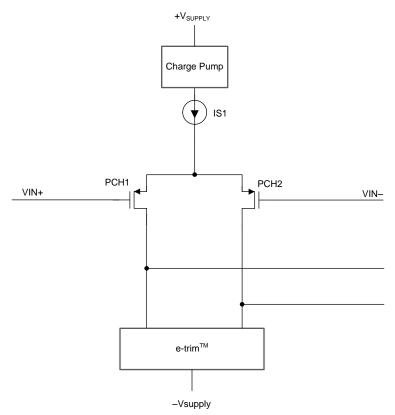


Figure 49. Single Differential Input Pair with a Charge Pump (Zero-Crossover)

22



The unique zero-crossover topology shown in Table 1 eliminates the input offset transition region, typical of most rail-to-rail input operational amplifiers. This topology allows the OPAx325 to provide superior CMRR across the entire common-mode input range that extends 100 mV beyond both power-supply rails. Figure 50 shows the input offset voltage versus input common-mode voltage plot for the OPAx325.

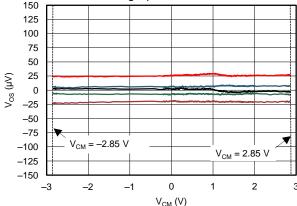


Figure 50. Offset Voltage vs Common-Mode Voltage (OPAx325, Zero-Crossover Amplifier)

The OPAx325 and a typical CMOS amplifier were used in identical circuits where these amplifiers were configured as a unity-gain buffer amplifier; see Figure 51 and Figure 52. A pure sine wave with an amplitude of 2 V (4 V<sub>PP</sub>) was given as input to the two identical circuits of Figure 51 and Figure 52. The outputs of these circuits were captured on a spectrum analyzer. Figure 53 and Figure 54 illustrate the output voltage spectrum for the OPAx325 and a typical CMOS rail-to-rail amplifier, respectively. The output of the OPAx325 has very few spurs and harmonics when compared to the typical rail-to-rail CMOS amplifier, as illustrated in Figure 55.

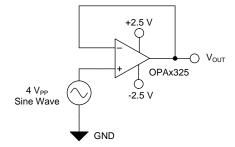


Figure 51. OPAx325 as a Unity-Gain Buffer

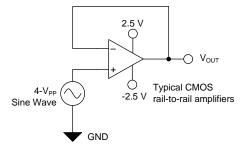
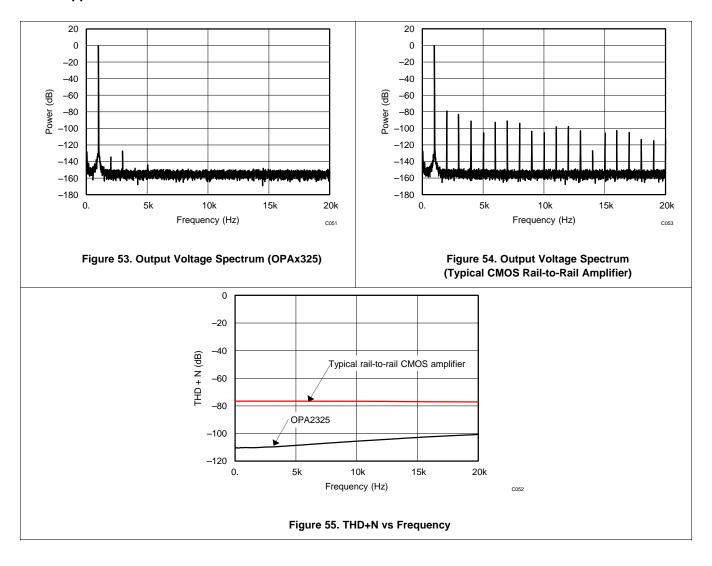


Figure 52. Typical CMOS Rail-to-Rail Amplifier as a Unity-Gain Buffer



#### 8.2.3 Application Curves





#### 9 Power Supply Recommendations

The OPAx325 are specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

#### 10 Layout

#### 10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for singlesupply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective
  methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes.
  A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure
  to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more
  detailed information refer to, see Circuit Board Layout Techniques.
- In order to reduce parasitic coupling, run the input traces as far away as possible from the supply or output
  traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as
  opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As illustrated in Figure 57, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, clean the PCB following board assembly.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the
  plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to
  remove moisture introduced into the device packaging during the cleaning process. A low-temperature, postcleaning bake at 85°C for 30 minutes is sufficient for most circumstances.



#### 10.2 Layout Example

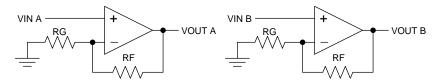


Figure 56. Schematic Representation for Figure 57

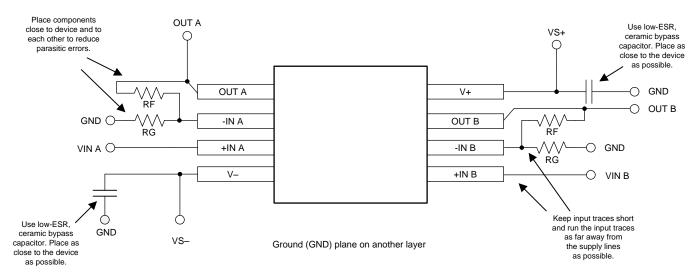


Figure 57. Layout Example



#### 11 Device and Documentation Support

#### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

Texas Instruments, Circuit Board Layout Techniques application report

#### 11.2 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 1. Related Links

| PARTS   | PRODUCT FOLDER | ORDER NOW  | TECHNICAL DOCUMENTS | TOOLS &<br>SOFTWARE | SUPPORT & COMMUNITY |
|---------|----------------|------------|---------------------|---------------------|---------------------|
| OPA325  | Click here     | Click here | Click here          | Click here          | Click here          |
| OPA2325 | Click here     | Click here | Click here          | Click here          | Click here          |
| OPA4325 | Click here     | Click here | Click here          | Click here          | Click here          |

#### 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 11.5 Trademarks

e-trim, E2E are trademarks of Texas Instruments.

All other trademarks are the property of their respective owners.

#### 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 11.7 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

#### 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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10-Nov-2025

#### PACKAGING INFORMATION

| Orderable part number | Status | Material type | Package   Pins   | Package qty   Carrier | RoHS | Lead finish/<br>Ball material | MSL rating/<br>Peak reflow | Op temp (°C) | Part marking (6) |
|-----------------------|--------|---------------|------------------|-----------------------|------|-------------------------------|----------------------------|--------------|------------------|
|                       |        |               |                  |                       |      | (4)                           | (5)                        |              |                  |
| OPA2325ID             | Active | Production    | SOIC (D)   8     | 75   TUBE             | Yes  | NIPDAU                        | Level-2-260C-1 YEAR        | -40 to 125   | O2325            |
| OPA2325ID.B           | Active | Production    | SOIC (D)   8     | 75   TUBE             | Yes  | NIPDAU                        | Level-2-260C-1 YEAR        | -40 to 125   | O2325            |
| OPA2325IDGKR          | Active | Production    | VSSOP (DGK)   8  | 2500   LARGE T&R      | Yes  | NIPDAUAG   SN                 | Level-2-260C-1 YEAR        | -40 to 125   | 18L6             |
| OPA2325IDGKR.B        | Active | Production    | VSSOP (DGK)   8  | 2500   LARGE T&R      | Yes  | SN                            | Level-2-260C-1 YEAR        | -40 to 125   | 18L6             |
| OPA2325IDGKT          | Active | Production    | VSSOP (DGK)   8  | 250   SMALL T&R       | Yes  | NIPDAUAG   SN                 | Level-2-260C-1 YEAR        | -40 to 125   | 18L6             |
| OPA2325IDGKT.B        | Active | Production    | VSSOP (DGK)   8  | 250   SMALL T&R       | Yes  | SN                            | Level-2-260C-1 YEAR        | -40 to 125   | 18L6             |
| OPA2325IDR            | Active | Production    | SOIC (D)   8     | 2500   LARGE T&R      | Yes  | NIPDAU                        | Level-2-260C-1 YEAR        | -40 to 125   | O2325            |
| OPA2325IDR.B          | Active | Production    | SOIC (D)   8     | 2500   LARGE T&R      | Yes  | NIPDAU                        | Level-2-260C-1 YEAR        | -40 to 125   | O2325            |
| OPA2325IDRG4          | Active | Production    | SOIC (D)   8     | 2500   LARGE T&R      | Yes  | NIPDAU                        | Level-2-260C-1 YEAR        | -40 to 125   | O2325            |
| OPA2325IDRG4.B        | Active | Production    | SOIC (D)   8     | 2500   LARGE T&R      | Yes  | NIPDAU                        | Level-2-260C-1 YEAR        | -40 to 125   | O2325            |
| OPA325IDBVR           | Active | Production    | SOT-23 (DBV)   5 | 3000   LARGE T&R      | Yes  | NIPDAU                        | Level-2-260C-1 YEAR        | -40 to 125   | 1UEV             |
| OPA325IDBVR.B         | Active | Production    | SOT-23 (DBV)   5 | 3000   LARGE T&R      | Yes  | NIPDAU                        | Level-2-260C-1 YEAR        | -40 to 125   | 1UEV             |
| OPA325IDBVRG4         | Active | Production    | SOT-23 (DBV)   5 | 3000   LARGE T&R      | Yes  | NIPDAU                        | Level-2-260C-1 YEAR        | -40 to 125   | 1UEV             |
| OPA325IDBVRG4.B       | Active | Production    | SOT-23 (DBV)   5 | 3000   LARGE T&R      | Yes  | NIPDAU                        | Level-2-260C-1 YEAR        | -40 to 125   | 1UEV             |
| OPA325IDBVT           | Active | Production    | SOT-23 (DBV)   5 | 250   SMALL T&R       | Yes  | NIPDAU                        | Level-2-260C-1 YEAR        | -40 to 125   | 1UEV             |
| OPA325IDBVT.B         | Active | Production    | SOT-23 (DBV)   5 | 250   SMALL T&R       | Yes  | NIPDAU                        | Level-2-260C-1 YEAR        | -40 to 125   | 1UEV             |
| OPA4325IPW            | Active | Production    | TSSOP (PW)   14  | 90   TUBE             | Yes  | NIPDAU                        | Level-2-260C-1 YEAR        | -40 to 125   | 4325             |
| OPA4325IPW.B          | Active | Production    | TSSOP (PW)   14  | 90   TUBE             | Yes  | NIPDAU                        | Level-2-260C-1 YEAR        | -40 to 125   | 4325             |
| OPA4325IPWR           | Active | Production    | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes  | NIPDAU                        | Level-2-260C-1 YEAR        | -40 to 125   | 4325             |
| OPA4325IPWR.B         | Active | Production    | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes  | NIPDAU                        | Level-2-260C-1 YEAR        | -40 to 125   | 4325             |

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.



#### PACKAGE OPTION ADDENDUM

www.ti.com 10-Nov-2025

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

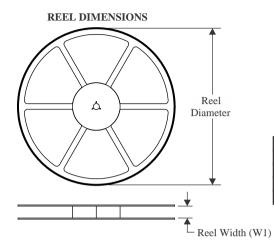
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www.ti.com 24-Jul-2025

#### TAPE AND REEL INFORMATION

NSTRUMENTS



# TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

| A0 | Dimension designed to accommodate the component width     |
|----|---|
| В0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

| Device        | Package<br>Type | Package<br>Drawing |    | SPQ  | Reel<br>Diameter<br>(mm) | Reel<br>Width<br>W1 (mm) | A0<br>(mm) | B0<br>(mm) | K0<br>(mm) | P1<br>(mm) | W<br>(mm) | Pin1<br>Quadrant |
|---------------|-----------------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| OPA2325IDGKR  | VSSOP           | DGK                | 8  | 2500 | 330.0                    | 12.4                     | 5.25       | 3.35       | 1.25       | 8.0        | 12.0      | Q1               |
| OPA2325IDGKT  | VSSOP           | DGK                | 8  | 250  | 330.0                    | 12.4                     | 5.25       | 3.35       | 1.25       | 8.0        | 12.0      | Q1               |
| OPA2325IDR    | SOIC            | D                  | 8  | 2500 | 330.0                    | 12.4                     | 6.4        | 5.2        | 2.1        | 8.0        | 12.0      | Q1               |
| OPA2325IDRG4  | SOIC            | D                  | 8  | 2500 | 330.0                    | 12.4                     | 6.4        | 5.2        | 2.1        | 8.0        | 12.0      | Q1               |
| OPA325IDBVR   | SOT-23          | DBV                | 5  | 3000 | 180.0                    | 8.4                      | 3.23       | 3.17       | 1.37       | 4.0        | 8.0       | Q3               |
| OPA325IDBVRG4 | SOT-23          | DBV                | 5  | 3000 | 180.0                    | 8.4                      | 3.23       | 3.17       | 1.37       | 4.0        | 8.0       | Q3               |
| OPA325IDBVT   | SOT-23          | DBV                | 5  | 250  | 180.0                    | 8.4                      | 3.23       | 3.17       | 1.37       | 4.0        | 8.0       | Q3               |
| OPA4325IPWR   | TSSOP           | PW                 | 14 | 2000 | 330.0                    | 12.4                     | 6.9        | 5.6        | 1.6        | 8.0        | 12.0      | Q1               |



www.ti.com 24-Jul-2025



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| OPA2325IDGKR  | VSSOP        | DGK             | 8    | 2500 | 366.0       | 364.0      | 50.0        |
| OPA2325IDGKT  | VSSOP        | DGK             | 8    | 250  | 366.0       | 364.0      | 50.0        |
| OPA2325IDR    | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| OPA2325IDRG4  | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| OPA325IDBVR   | SOT-23       | DBV             | 5    | 3000 | 213.0       | 191.0      | 35.0        |
| OPA325IDBVRG4 | SOT-23       | DBV             | 5    | 3000 | 213.0       | 191.0      | 35.0        |
| OPA325IDBVT   | SOT-23       | DBV             | 5    | 250  | 213.0       | 191.0      | 35.0        |
| OPA4325IPWR   | TSSOP        | PW              | 14   | 2000 | 353.0       | 353.0      | 32.0        |

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 24-Jul-2025

#### **TUBE**



\*All dimensions are nominal

| Device       | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| OPA2325ID    | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA2325ID.B  | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA4325IPW   | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |
| OPA4325IPW.B | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |



SMALL OUTLINE INTEGRATED CIRCUIT



#### NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE TRANSISTOR



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







#### NOTES:

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- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-187.





NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
- 9. Size of metal pad may vary due to creepage requirement.





NOTES: (continued)

- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.



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