

SBOS167D - NOVEMBER 2000- REVISED JULY 2007

*micro*Power, Rail-to-Rail Operational Amplifiers

FEATURES

• LOW I_O: 20μA

microSIZE PACKAGES: WCSP-8, SC70-5 SOT23-5, SOT23-8, and TSSOP-14

 HIGH SPEED/POWER RATIO WITH BANDWIDTH: 350kHz

● RAIL-TO-RAIL INPUT AND OUTPUT

● SINGLE SUPPLY: 2.3V to 5.5V

APPLICATIONS

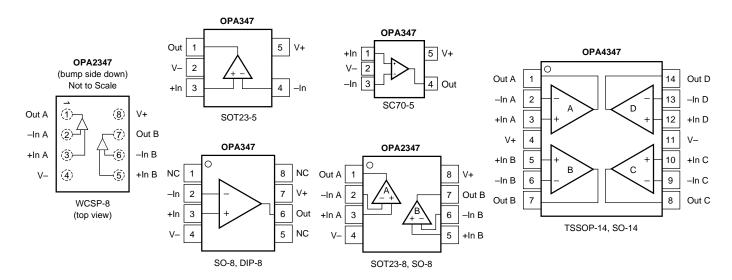
- PORTABLE EQUIPMENT
- BATTERY-POWERED EQUIPMENT
- 2-WIRE TRANSMITTERS
- SMOKE DETECTORS
- CO DETECTORS

DESCRIPTION

The OPA347 is a *micro*Power, low-cost operational amplifier available in *micro*packages. The OPA347 (single version) is available in the SC-70 and SOT23-5 packages. The OPA2347 (dual version) is available in the SOT23-8 and WCSP-8 packages. Both are also available in the SO-8. The OPA347 is also available in the DIP-8. The OPA4347 (quad) is available in the SO-14 and the TSSOP-14.

The small size and low power consumption ($34\mu A$ per channel maximum) of the OPA347 make it ideal for portable and battery-powered applications. The input range of the OPA347 extends 200mV beyond the rails, and the output range is within 5mV of the rails. The OPA347 also features an excellent speed/power ratio with a bandwidth of 350kHz.

The OPA347 can be operated with a single or dual power supply from 2.3V to 5.5V. All models are specified for operation from -55° C to $+125^{\circ}$ C.





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ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V+ to V	7.5V
Signal Input Terminals, Voltage(2)	
Current ⁽²⁾	10mA
Output Short-Circuit ⁽³⁾	Continuous
Operating Temperature	65°C to +150°C
Storage Temperature	65°C to +150°C
Junction Temperature	150°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only. Functional operation of the device at these conditions, or beyond the specified operating conditions, is not implied. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE/LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA347NA	SOT23-5	DBV "	A47
OPA347PA OPA347UA	DIP-8 SO-8	P D "	OPA347PA OPA347UA
OPA347SA	SC-70	DCK "	S47
OPA2347EA	SOT23-8	DCN "	B47
OPA2347UA "	SO-8	D "	OPA2347UA "
OPA2347YED	WCSP-8	YED "	YMD CCS
OPA2347YZDR	Lead-Free WCSP-8	YZD	A9
OPA4347EA	TSSOP-14	PW "	OPA4347EA
OPA4347UA "	SO-14	D "	OPA4347UA "

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com.



ELECTRICAL CHARACTERISTICS: $V_S = 2.5V$ to 5.5V

Boldface limits apply over the specified temperature range, $T_A = -55^{\circ}C$ to +125°C.

At T_A = +25°C, R_L = 100k Ω connected to V_S/2 and V_{OUT} = V_S/2, unless otherwise noted.

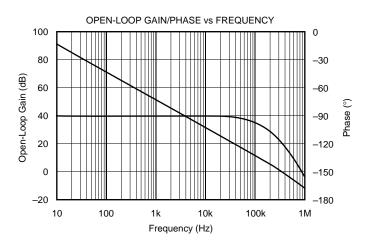
		OP		YED	
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
OFFSET VOLTAGE Input Offset Voltage over Temperature Drift			2 2 3 60 0.3 128	6 7 175 300	mV mV μ V/°C μV/V μ V/V μV/V dB
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection Ratio Over Temperature Over Temperature		(V-) - 0.2 70 66 54 48	80 70	(V+) + 0.2	V dB dB dB dB
INPUT BIAS CURRENT ⁽¹⁾ Input Bias Current Input Offset Current Input Offset Current			±0.5 ±0.5	±10 ±10	pA pA
INPUT IMPEDANCE Differential Common-Mode			10 ¹³ 3 10 ¹³ 6		Ω pF Ω pF
NOISEInput Voltage Noise, $f = 0.1Hz$ to $10Hz$ Input Voltage Noise Density, $f = 1kHz$ Input Current Noise Density, $f = 1kHz$			12 60 0.7		μV _{PP} nV/√ <u>Hz</u> fA/√Hz
OPEN-LOOP GAIN Open-Loop Voltage Gain over Temperature	$V_S = 5.5V$, $R_L = 100k\Omega$, $0.015V < V_O < 5.485V$ $V_S = 5.5V$, $R_L = 100k\Omega$, $0.015V < V_O < 5.485V$ $V_S = 5.5V$, $R_L = 5k\Omega$, $0.125V < V_O < 5.375V$	100 88 100	115 115		dB dB dB
over Temperature A _{OL} (SC-70 only)	$V_S = 5.5V$, $R_L = 5k\Omega$, $0.125V < V_O < 5.375V$	88 96	115		dB dB
OUTPUT Voltage Output Swing from Rail over Temperature over Temperature Short-Circuit Current Capacitive Load Drive CULTY COUTPUT Voltage Volt		See T	5 90 ±17 Typical Characte	15 15 125 125	mV mV mV mV mA
FREQUENCY RESPONSE Gain-Bandwidth Product GBW Slew Rate SR Settling Time, 0.1% t ₅ 0.01% Overload Recovery Time	G = +1		350 0.17 21 27 23		kHz V/μs μs μs μs
POWER SUPPLY Specified Voltage Range Minimum Operating Voltage Minimum Operating Voltage (OPA347SA) Quiescent Current (per amplifier) over Temperature		2.5	2.3 2.4 20	5.5 34 38	V V V μΑ
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance θ _{J/ε} SOT23-5 Surface-Mount SOT23-8 Surface-Mount SO-8 Surface-Mount SO-14 Surface-Mount TSSOP-14 Surface-Mount DIP-8 SC70-5 Surface-Mount WCSP		-55 -65 -65	200 150 150 100 100 100 250 250	125 150 150	°C °C °C °C/W °C/W °C/W °C/W °C/W °C/W °

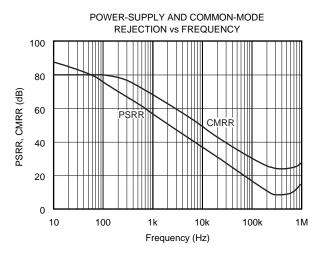
NOTE: (1) Input bias current for the OPA2347YED package is specified in the absence of light. See the Photosensitivity section for further detail.

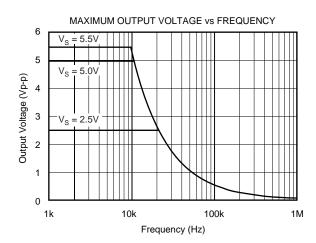


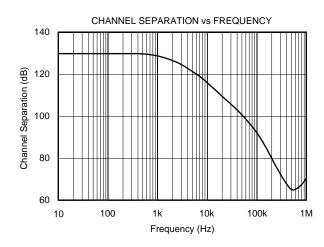
TYPICAL CHARACTERISTICS

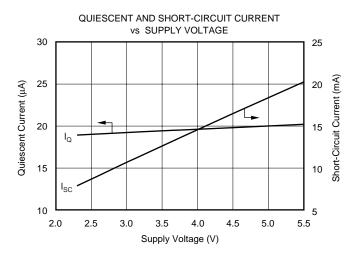
At T_A = +25°C, V_S = +5V, and R_L = 100k Ω connected to $V_S/2$, unless otherwise noted.

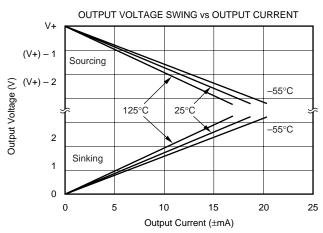








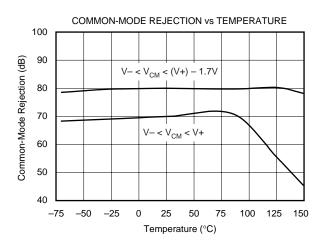


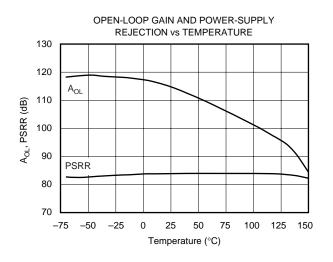


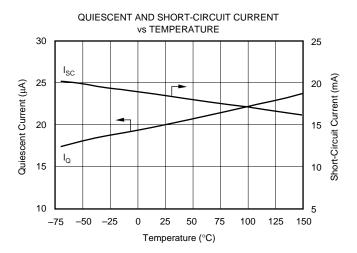


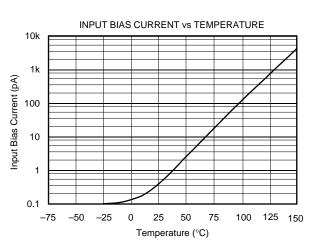
TYPICAL CHARACTERISTICS (Cont.)

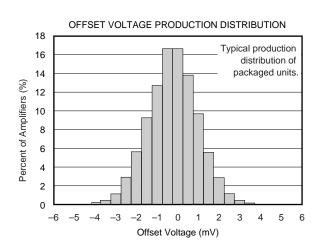
At $T_A = +25$ °C, $V_S = +5V$, and $R_L = 100$ k Ω connected to $V_S/2$, unless otherwise noted.

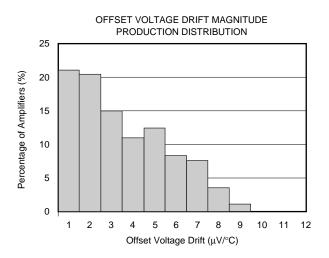






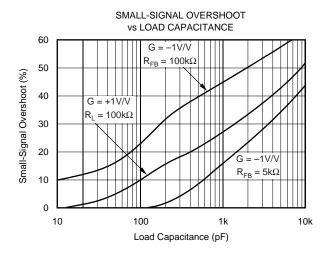


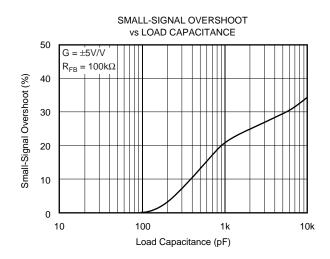


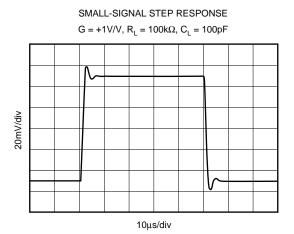


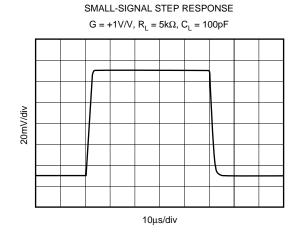
TYPICAL CHARACTERISTICS (Cont.)

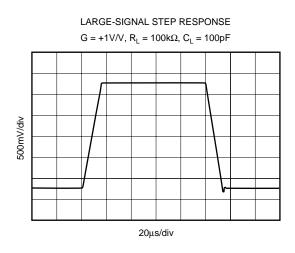
At T_A = +25°C, V_S = +5V, and R_L = 100k Ω connected to $V_S/2$, unless otherwise noted.

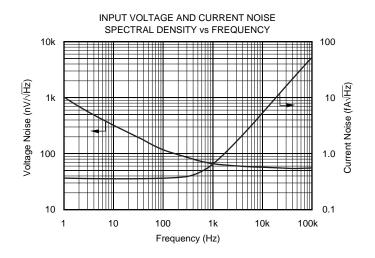












APPLICATIONS INFORMATION

The OPA347 series op amps are unity-gain stable and can operate on a single supply, making them highly versatile and easy to use.

Rail-to-rail input and output swing significantly increases dynamic range, especially in low supply applications. Figure 1 shows the input and output waveforms for the OPA347 in unity-gain configuration. Operation is from $V_S = +5V$ with a $100k\Omega$ load connected to $V_S/2$. The input is a $5V_{PP}$ sinusoid. Output voltage is approximately $4.995V_{PP}$.

Power-supply pins should be bypassed with $0.01\mu\text{F}$ ceramic capacitors.

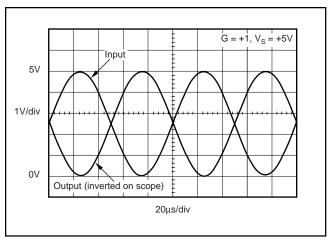


FIGURE 1. Rail-to-Rail Input and Output.

OPERATING VOLTAGE

The OPA347 series op amps are fully specified and ensured from 2.5V to 5.5V. In addition, many specifications apply from –55°C to +125°C. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristics.

RAIL-TO-RAIL INPUT

The input common-mode voltage range of the OPA347 series extends 200mV beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair, as shown in Figure 2. The N-channel pair is active for input voltages close to the positive rail, typically (V+) - 1.3V to 200mV above the positive supply, while the P-channel pair is on for inputs from 200mV below the negative supply to approximately (V+) - 1.3V. There is a small transition region, typically (V+) - 1.5V to (V+) - 1.1V, in which both pairs are on. This 400mV transition region can vary 300mV with process variation. Thus, the transition region (both stages on) can range from (V+) - 1.65V to (V+) - 1.25V on the low end, up to (V+) - 1.35V to (V+) - 0.95V on the high end. Within the 400mV transition region PSRR, CMRR, offset voltage, and offset drift may be degraded compared to operation outside this region. For more information on designing with rail-to-rail input op amps, see Figure 3, Design Optimization with Rail-to-Rail Input Op Amps.

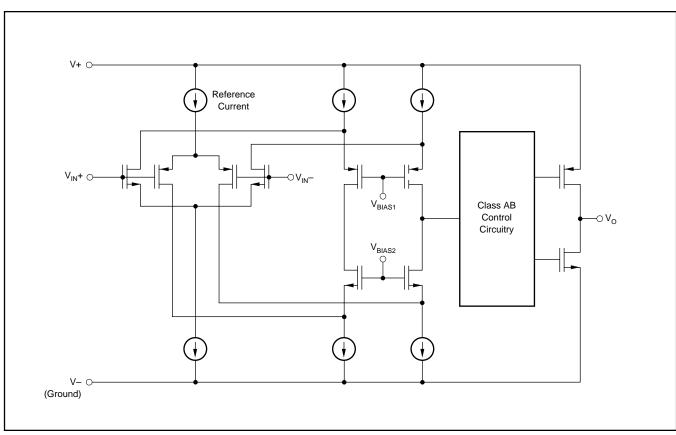


FIGURE 2. Simplified Schematic.



DESIGN OPTIMIZATION WITH RAIL-TO-RAIL INPUT OP AMPS

Rail-to-rail op amps can be used in virtually any op amp configuration. To achieve optimum performance, however, applications using these special double-input-stage op amps may benefit from consideration of their special behavior.

In many applications, operation remains within the common-mode range of only one differential input pair. However, some applications exercise the amplifier through the transition region of both differential input stages. A small discontinuity may occur in this transition. Careful selection of the circuit configuration, signal levels, and biasing can often avoid this transition region.

With a unity-gain buffer, for example, signals will traverse this transition at approximately 1.3V below the V+ supply and may exhibit a small discontinuity at this point.

The common-mode voltage of the noninverting amplifier is equal to the input voltage. If the input signal always remains less than the transition voltage, no discontinuity will be created. The closed-loop gain of this configuration can still produce a rail-to-rail output.

Inverting amplifiers have a constant common-mode voltage equal to V_B . If this bias voltage is constant, no discontinuity will be created. The bias voltage can generally be chosen to avoid the transition region.

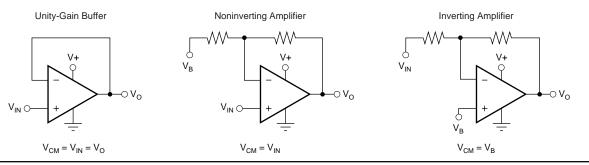


FIGURE 3. Design Optimization with Rail-to-Rail Input Op Amps.

COMMON-MODE REJECTION

The CMRR for the OPA347 is specified in several ways so the best match for a given application may be used. First, the CMRR of the device in the common-mode range below the transition region ($V_{CM} < (V+) - 1.7V$) is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR at $V_S = 5.5V$ over the entire common-mode range is specified.

INPUT VOLTAGE

The input common-mode range extends from (V-) - 0.2V to (V+) + 0.2V. For normal operation, inputs should be limited to this range. The absolute maximum input voltage is 500mV beyond the supplies. Inputs greater than the input common-mode range but less than the maximum input voltage, while not valid, will not cause any damage to the op amp. Furthermore, if input current is limited the inputs may go beyond the power supplies without phase inversion, as shown in Figure 4, unlike some other op amps.

Normally, input currents are 0.4pA. However, large inputs (greater than 500mV beyond the supply rails) can cause excessive current to flow in or out of the input pins. Therefore, as well as keeping the input voltage below the maximum rating, it is also important to limit the input current to less than 10mA. This is easily accomplished with an input resistor, as shown in Figure 5.

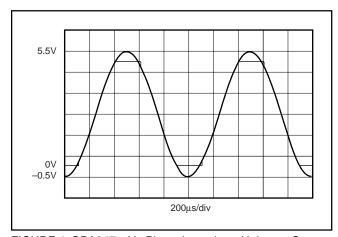


FIGURE 4. OPA347—No Phase Inversion with Inputs Greater than the Power-Supply Voltage.

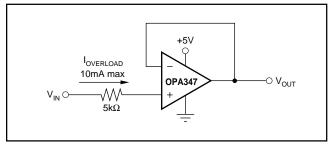


FIGURE 5. Input Current Protection for Voltages Exceeding the Supply Voltage.



RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving $5k\Omega$ loads connected to any potential between V+ and ground. For light resistive loads (> $100k\Omega$), the output voltage can typically swing to within 5mV from supply rail. With moderate resistive loads ($10k\Omega$ to $50k\Omega$), the output can swing to within a few tens of millivolts from the supply rails while maintaining high open-loop gain (see the typical characteristic Output Voltage Swing vs Output Current).

CAPACITIVE LOAD AND STABILITY

The OPA347 in a unity-gain configuration can directly drive up to 250pF pure capacitive load. Increasing the gain enhances the amplifier's ability to drive greater capacitive loads (see the characteristic curve Small-Signal Overshoot vs Capacitive Load). In unity-gain configurations, capacitive load drive can be improved by inserting a small (10 Ω to 20Ω) resistor, $R_{\rm S}$, in series with the output, as shown in Figure 6. This significantly reduces ringing while maintaining Direct Current (DC) performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a DC error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio $R_{\rm S}/R_{\rm L}$, and is generally negligible.

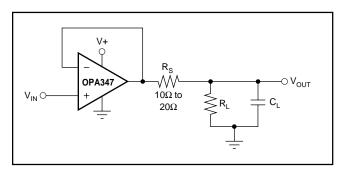


FIGURE 6. Series Resistor in Unity-Gain Buffer Configuration Improves Capacitive Load Drive.

In unity-gain inverter configuration, phase margin can be reduced by the reaction between the capacitance at the op amp input, and the gain setting resistors, thus degrading capacitive load drive. Best performance is achieved by using small valued resistors. For example, when driving a 500pF

load, reducing the resistor values from 100k Ω to 5k Ω decreases overshoot from 40% to 8% (see the characteristic curve Small-Signal Overshoot vs Load Capacitance). However, when large-valued resistors can not be avoided, a small (4pF to 6pF) capacitor, C_{FB} , can be inserted in the feedback, as shown in Figure 7. This significantly reduces overshoot by compensating the effect of capacitance, C_{IN} , which includes the amplifier input capacitance and PC board parasitic capacitance.

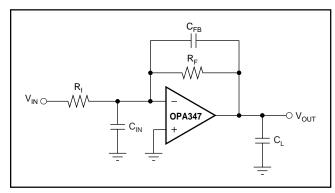


FIGURE 7. Adding a Feedback Capacitor In the Unity-Gain Inverter Configuration Improves Capacitative Load.

DRIVING ADCs

The OPA347 series op amps are optimized for driving medium-speed sampling Analog-to-Digital Converters (ADCs). The OPA347 op amps buffer the ADC's input capacitance and resulting charge injection while providing signal gain.

See Figure 8 for the OPA347 in a basic noninverting configuration driving the ADS7822. The ADS7822 is a 12-bit, *micro*Power sampling converter in the MSOP-8 package. When used with the low-power, miniature packages of the OPA347, the combination is ideal for space-limited, low-power applications. In this configuration, an RC network at the ADC input can be used to provide for anti-aliasing filter and charge injection current.

See Figure 9 for the OPA2347 driving an ADS7822 in a speech bandpass filtered data acquisition system. This small, low-cost solution provides the necessary amplification and signal conditioning to interface directly with an electret microphone. This circuit will operate with $V_S = 2.7 V$ to 5V with less than 250 μ A typical quiescent current.

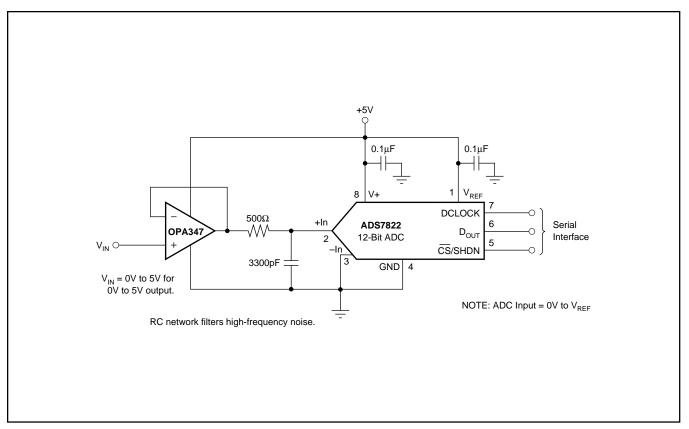


FIGURE 8. OPA347 in Noninverting Configuration Driving ADS7822.

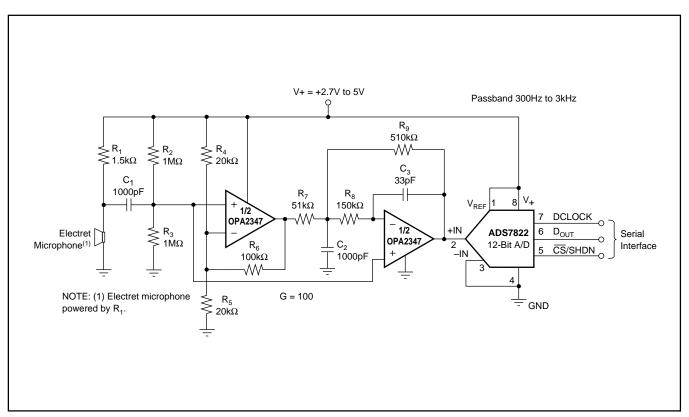


FIGURE 9. Speech Bandpass Filtered Data Acquisition System.

OPA2347 WCSP PACKAGE

The OPA2347YED and OPA2347YZDR are die-level packages using bump-on-pad technology. The OPA2347YED device has tin-lead balls; the OPA2347YZDR has lead-free balls. Unlike devices that are in plastic packages, these devices have no molding compound, lead frame, wire bonds, or leads. Using standard surface-mount assembly procedures, the WCSP can be mounted to a printed circuit board without additional under fill. Figures 10 and 11 detail pinout and package marking.

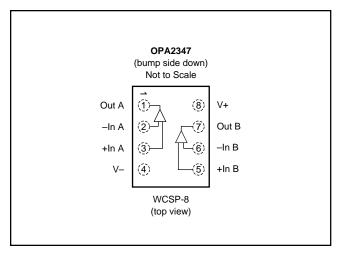


FIGURE 10. Pin Description.

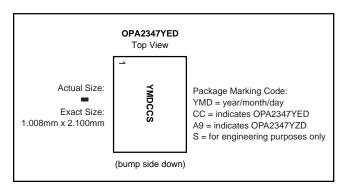


FIGURE 11. Top View Package Marking.

PHOTOSENSITIVITY

Although the OPA2347YED/YZD package has a protective backside coating that reduces the amount of light exposure on the die, unless fully shielded, ambient light will still reach the active region of the device. Input bias current for the OPA2347YED/YZD package is specified in the absence of light. Depending on the amount of light exposure in a given application, an increase in bias current, and possible increases in offset voltage should be expected. In circuit board tests under ambient light conditions, a typical increase in bias current reached 100pA. Flourescent lighting may introduce noise or hum due to their time varying light output. Best practice should include end-product packaging that provides shielding from possible light souces during operation.

RELIABILITY TESTING

To ensure reliability, the OPA2347YED and OPA2347YZDR devices have been verified to successfully pass a series of reliability stress tests. A summary of JEDEC standard reliability tests is shown in Table I.

TEST	CONDITION	ACCEPT CRITERIA (ACTUAL)	SAMPLE SIZE
Temperature Cycle	-40°C to 125°C, 1 Cycle/hr, 15 Minute Ramp ⁽¹⁾ 10 Minute Dwell	500 (1600) Cycles, R < 1.2X from R ₀	36
Drop	50cm	10 (129) Drops, R < 1.2X from R ₀	8
Key Push	100 Cycles/min, 1300 με, Displacement = 2.7mm Max	5K (6.23K) Cycles, R < 1.2X from R ₀	8
3 Point Bend	Strain Rate 5 mm/min, 85 mm Span	R < 1.2X from R ₀	8
NOTE: (1) Per IPC970	1.		•

TABLE I. Reliability Test Results.



LAND PATTERNS AND ASSEMBLY

The recommended land pattern for the OPA2347YED package is detailed in Figure 12 with specifications listed in Table II. The maximum amount of force during assembly should be limited to 30 grams of force per bump.

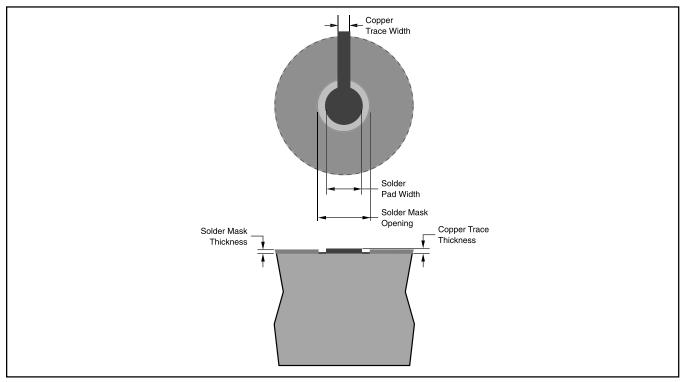


FIGURE 12. Recommended Land Area.

SOLDER PAD DEFINITION	COPPER PAD	SOLDER MASK OPENING	COPPER THICKNESS	STENCIL OPENING	STENCIL THICKNESS
Non-Solder Mask Defined (NSMD)	275μm (+0.0, –25μm)	375μm (+0.0, –25μm)	1 oz max	275μm X 275μm, sq	125μm Thick

NOTES: (1) Circuit traces from NSMD-defined PWB lands should be less tham $100\mu m$ (preferrably = $75\mu m$) wide in the exposed area inside the solder mask opening. Wider trace widths will reduce device stand off and impact reliability. (2) Recommended solder paste is type 3 or type 4. (3) Best reliability results are achieved when the PWB laminate glass transistion temperature is above the operating range of the intended application. (4) For PWB using an Ni/Au surface finish, the gold thickness should be less than 0.5um to avoid solder embrittlement and a reduction in thermal fatigue performance. (5) Solder mask thickness should be less than 20um on top of the copper circuit pattern. (6) Best solder stencil performance will be achieved using laser-cut stencils with electro polishing. Use of chemically etched stencils results in inferior solder paste volume control. (7) Trace routing away from the WLCSP device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

TABLE II. Recommended Land Pattern.

www.ti.com

11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
OPA2347EA/250	Active	Production	SOT-23 (DCN) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	B47
OPA2347EA/250.B	Active	Production	SOT-23 (DCN) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	B47
OPA2347EA/250G4	Active	Production	SOT-23 (DCN) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	B47
OPA2347EA/3K	Active	Production	SOT-23 (DCN) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	B47
OPA2347EA/3K.B	Active	Production	SOT-23 (DCN) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	B47
OPA2347EA/3KG4	Active	Production	SOT-23 (DCN) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	B47
OPA2347UA	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 2347UA
OPA2347UA.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 2347UA
OPA2347UA/2K5	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 2347UA
OPA2347UA/2K5.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 2347UA
OPA2347UA/2K5G4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 2347UA
OPA2347YZDR	Active	Production	DSBGA (YZD) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-	(A9, OPA2347)
OPA2347YZDR.B	Active	Production	DSBGA (YZD) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 125	(A9, OPA2347)
OPA2347YZDT	Active	Production	DSBGA (YZD) 8	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 125	OPA2347
OPA2347YZDT.B	Active	Production	DSBGA (YZD) 8	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 125	OPA2347
OPA347NA/250	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	A47
OPA347NA/250.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	A47
OPA347NA/250G4	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	A47
OPA347NA/250G4.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	A47
OPA347NA/3K	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	A47
OPA347NA/3K.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	A47
OPA347PA	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	OPA347PA
OPA347PA.B	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	OPA347PA
OPA347PAG4	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	OPA347PA
OPA347SA/250	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	S47





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Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
OPA347SA/250.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	S47
OPA347SA/3K	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	S47
OPA347SA/3K.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	S47
OPA347SA/3KG4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	S47
OPA347UA	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 347UA
OPA347UA.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 347UA
OPA347UA/2K5	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 347UA
OPA347UA/2K5.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 347UA
OPA4347EA/250	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 4347EA
OPA4347EA/250.B	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 4347EA
OPA4347EA/2K5	Active	Production	TSSOP (PW) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 4347EA
OPA4347EA/2K5.B	Active	Production	TSSOP (PW) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 4347EA
OPA4347EA/2K5G4	Active	Production	TSSOP (PW) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 4347EA
OPA4347EA/2K5G4.B	Active	Production	TSSOP (PW) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 4347EA
OPA4347UA	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA4347UA
OPA4347UA.B	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA4347UA
OPA4347UA/2K5	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA4347UA
OPA4347UA/2K5.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA4347UA
OPA4347UAG4	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA4347UA
OPA4347UAG4.B	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA4347UA

⁽¹⁾ Status: For more details on status, see our product life cycle.



PACKAGE OPTION ADDENDUM

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- (2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2347EA/250	SOT-23	DCN	8	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2347EA/3K	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2347UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2347YZDR	DSBGA	YZD	8	3000	178.0	9.2	1.23	2.27	0.73	4.0	8.0	Q1
OPA2347YZDT	DSBGA	YZD	8	250	178.0	9.2	1.23	2.27	0.73	4.0	8.0	Q1
OPA347NA/250	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA347NA/250G4	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA347NA/3K	SOT-23	DBV	5	3000	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA347SA/250	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA347SA/3K	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA347UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4347EA/250	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4347EA/2K5	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4347EA/2K5G4	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4347UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2347EA/250	SOT-23	DCN	8	250	200.0	183.0	25.0
OPA2347EA/3K	SOT-23	DCN	8	3000	200.0	183.0	25.0
OPA2347UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA2347YZDR	DSBGA	YZD	8	3000	220.0	220.0	35.0
OPA2347YZDT	DSBGA	YZD	8	250	220.0	220.0	35.0
OPA347NA/250	SOT-23	DBV	5	250	445.0	220.0	345.0
OPA347NA/250G4	SOT-23	DBV	5	250	445.0	220.0	345.0
OPA347NA/3K	SOT-23	DBV	5	3000	445.0	220.0	345.0
OPA347SA/250	SC70	DCK	5	250	200.0	183.0	25.0
OPA347SA/3K	SC70	DCK	5	3000	200.0	183.0	25.0
OPA347UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA4347EA/250	TSSOP	PW	14	250	213.0	191.0	35.0
OPA4347EA/2K5	TSSOP	PW	14	2500	353.0	353.0	32.0
OPA4347EA/2K5G4	TSSOP	PW	14	2500	353.0	353.0	32.0
OPA4347UA/2K5	SOIC	D	14	2500	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2347UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2347UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA347PA	Р	PDIP	8	50	506	13.97	11230	4.32
OPA347PA.B	Р	PDIP	8	50	506	13.97	11230	4.32
OPA347PAG4	Р	PDIP	8	50	506	13.97	11230	4.32
OPA347UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA347UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA4347UA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4347UA.B	D	SOIC	14	50	506.6	8	3940	4.32
OPA4347UAG4	D	SOIC	14	50	506.6	8	3940	4.32
OPA4347UAG4.B	D	SOIC	14	50	506.6	8	3940	4.32

DCN (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
- D. Package outline inclusive of solder plating.
- E. A visual index feature must be located within the Pin 1 index area.
- F. Falls within JEDEC MO-178 Variation BA.
- G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.



DCN (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.







- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





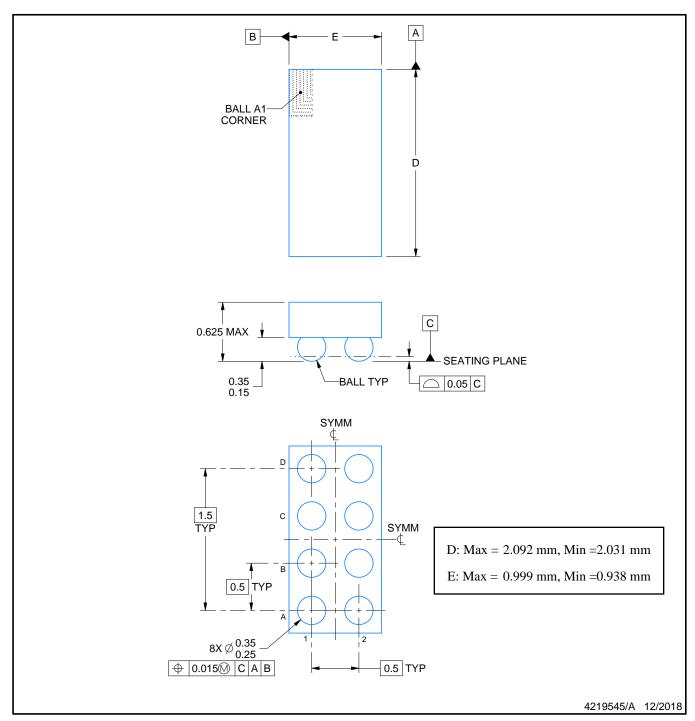
NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY

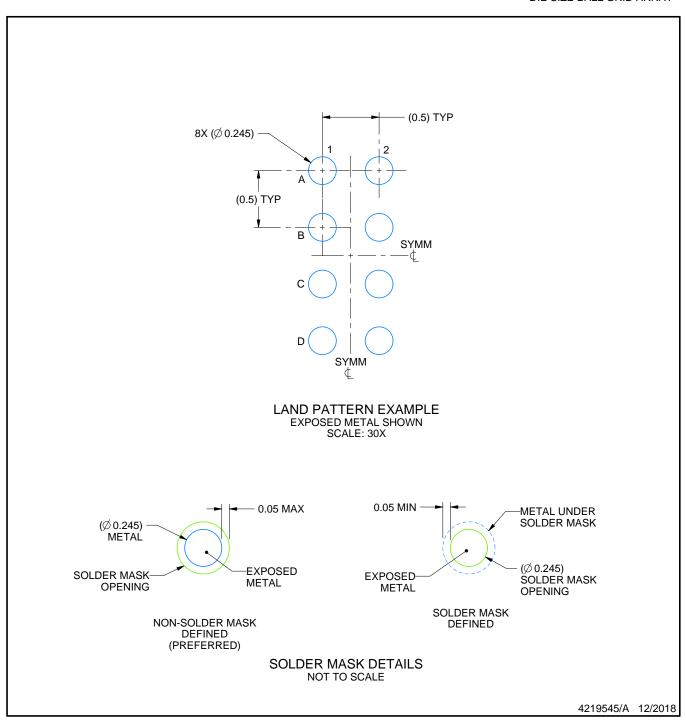


- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY

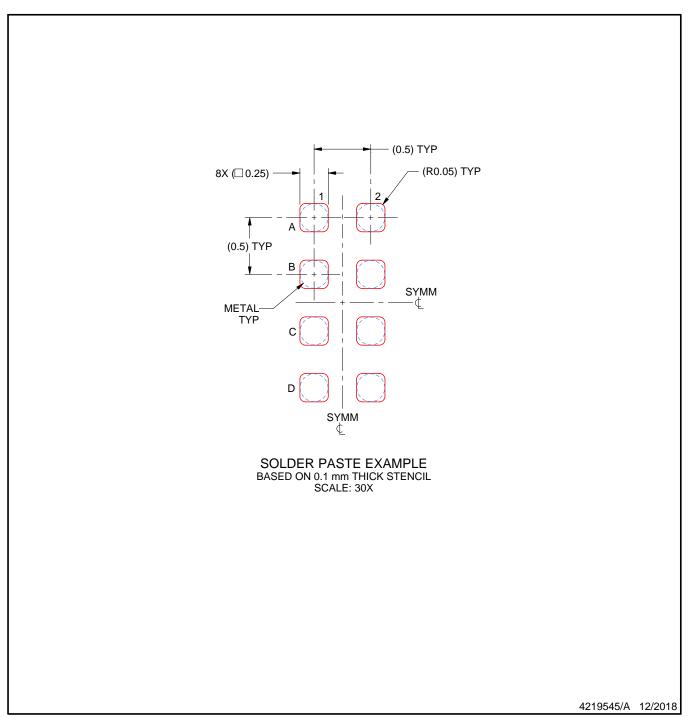


NOTES: (continued)

Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side





NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.







- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.





SMALL OUTLINE PACKAGE



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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