OPA333-Q1 Automotive, 1.8-V, Micropower, CMOS, Zero-Drift Operational Amplifier

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Low offset voltage: 10 μV (maximum)
- 0.01-Hz to 10-Hz noise: 1.1 μV_{PP}
- Quiescent current: 17 μA
- Single-supply operation
- Supply voltage: 1.8 V to 5.5 V
- Rail-to-rail input and output
- Microsize 5-pin SOT-23 (DBV) package

2 Applications

- Pump
- Position sensor
- Vehicle occupant detection sensor
- Brake system
- Airbag

3 Description

The OPA333-Q1 CMOS operational amplifier uses a proprietary autocalibration technique to simultaneously provide verylow offset voltage (10 μV maximum) and near-zero drift over time and temperature. This miniature, high-precision, low-quiescent-current amplifier offers high-impedance inputs that have a common-mode range 100 mV beyond the rails, and rail-to-rail output that swings within 50 mV of the rails. The device can use single or dual supplies as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V), and is optimized for low-voltage single-supply operation.

The OPA333-Q1 device offers excellent common-mode rejection ratio (CMRR) without the crossover associated with traditional complementary input stages. This design results in superior performance for driving analog-to-digital converters (ADCs) without degradation of differential linearity.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA333-Q1	SOT-23 (5)	1.60 mm × 2.90 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

0.1-Hz to 10-Hz Noise

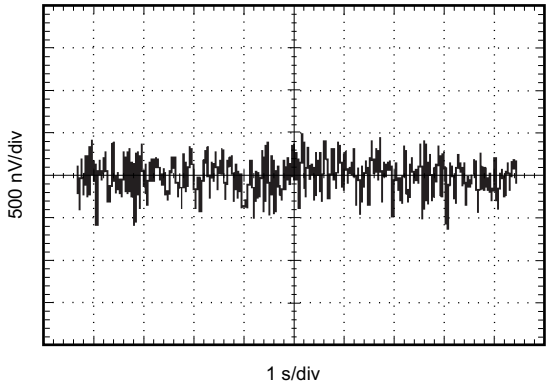


Table of Contents

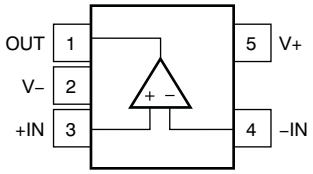
4 Revision History

Changes from Original (June 2010) to Revision A **Page**

- Changed part number references from *OPA333* to *OPA333-Q1* throughout text ... 1
- Added *Pin Configuration and Functions*, *ESD Ratings*, *Thermal Information*, *Feature Description* , *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout* , *Device and Documentation Support* , and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Deleted redundant *Ordering Information* table; same information already in the package option addendum ... 1
- Changed pinout drawing for accuracy; no change to pin names or pin numbers ... 3
- Deleted "one amplifier per package" from note 2 in *Absolute Maximum Ratings* table ... 4
- Changed the TYP and MAX values for the input offset voltage drift parameter in the *Electrical Characteristics* table ... 5
- Added text to Figure 3, *Open-Loop Gain vs Frequency*, for clarity ... 6
- Deleted *Single-Supply, Very-Low-Power ECG Circuit* (previously, Figure 9) ... 17

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN	3	I	Noninverting input
–IN	4	I	Inverting input
OUT	1	O	Output
V+	5	I	Positive (high) power supply
V–	2	I	Negative (low) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Supply voltage		7	V
	Signal input pins, voltage(2)	–0.3	(V+) + 0.3	V
	Output short circuit(3)	Continuous		
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150(4)	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current-limited to 10 mA or less.
(3) Short-circuit to ground.
(4) Long-term high-temperature storage, extended use at maximum recommended operating conditions, or both cases may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) Device HBM ESD classification level 3A	±4000	V
		Charged-device model (CDM), per AEC Q100-011 Device CDM ESD classification level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage	1.8	5.5	V
T_A	Specified temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA333-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	220.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	97.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at V_S = 1.8 V to 5.5 V, T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, V_O = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		2	10	µV
dV_{OS}/d_T	Input offset voltage drift	V_S = 5 V, T_A = –40°C to +125°C		0.02	0.05	µV/°C
PSRR	Power supply rejection ratio	V_S = 1.8 V to 5.5 V, T_A = –40°C to +125°C		1	6	µV/V
	Long-term stability(1)			See (1)		
	Channel separation, dc			0.1		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current			±70	±200	pA
		T_A = –40°C to +125°C		±200		pA
I_{OS}	Input offset current			±140	±400	pA
NOISE						
	Input voltage noise	f = 0.01 Hz to 1 Hz		0.3		$µV_{PP}$
		f = 0.1 Hz to 10 Hz		1.1		$µV_{PP}$
i_n	Input current noise	f = 10 Hz		100		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V , T_A = –40°C to +125°C	106	130		dB
INPUT CAPACITANCE						
	Differential			2		pF
	Common mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 100 mV < V_O < (V+) – 100 mV, R_L = 10 kΩ, T_A = –40°C to +125°C	106	130		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	C_L = 100 pF		350		kHz
SR	Slew rate	G = 1		0.16		V/µs
OUTPUT						
	Voltage output swing from rail	R_L = 10 kΩ		30	50	mV
		R_L = 10 kΩ, T_A = –40°C to +125°C			85	mV
I_{SC}	Short-circuit current			±5		mA
C_L	Capacitive load drive			See *Typical Characteristics*		
	Open-loop output impedance	f = 350 kHz, I_O = 0 A		2		kΩ
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 A		17	25	µA
	Quiescent current per amplifier over temperature	T_A = –40°C to +125°C			30	µA
	Turn-on time	V_S = 5 V		100		µs

(1) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 µV.

6.6 Typical Characteristics

at T_A = 25°C, V_S = 5 V, and C_L = 0 pF (unless otherwise noted)

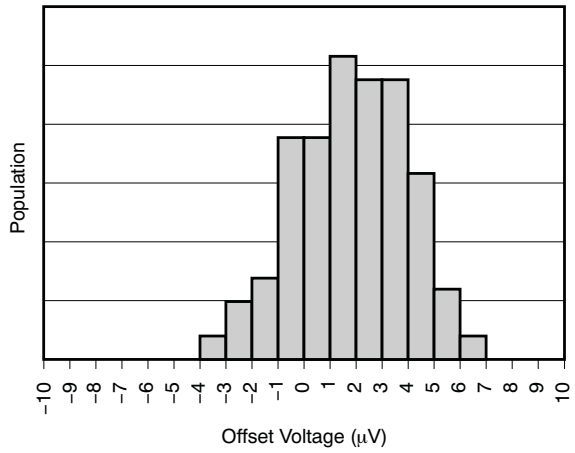


Figure 1. Offset Voltage Production Distribution

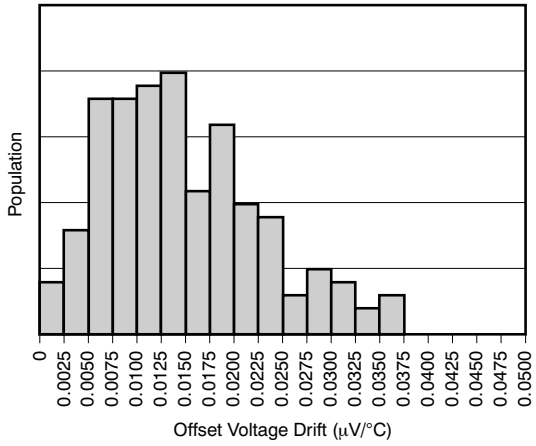


Figure 2. Offset Voltage Production Distribution

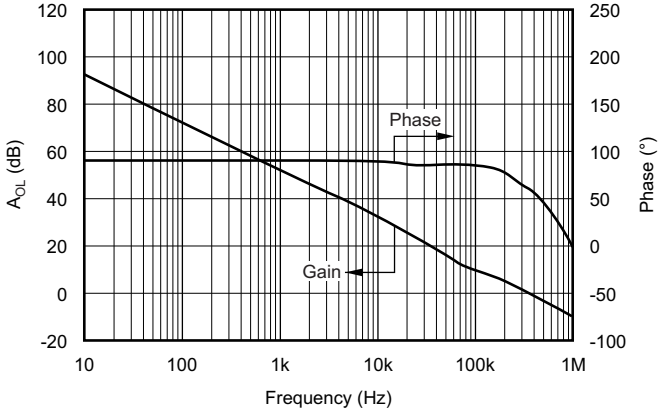


Figure 3. Open-Loop Gain vs Frequency

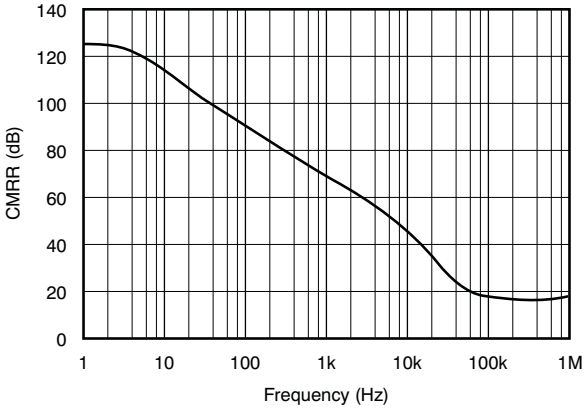


Figure 4. Common-Mode Rejection Ratio vs Frequency

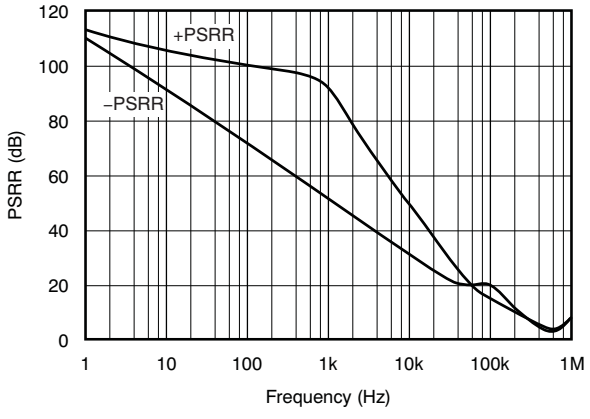


Figure 5. Power-Supply Rejection Ratio vs Frequency

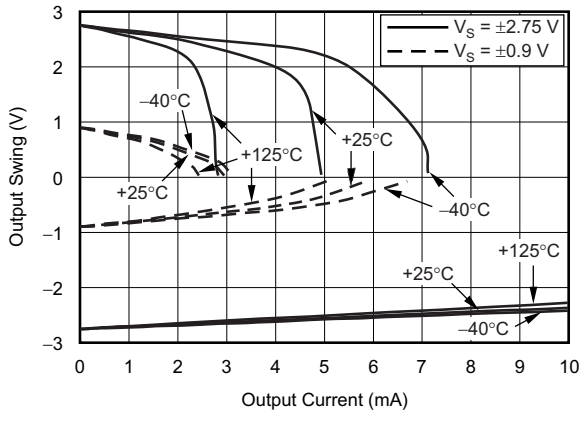


Figure 6. Output Voltage Swing vs Output Current

Typical Characteristics (continued)

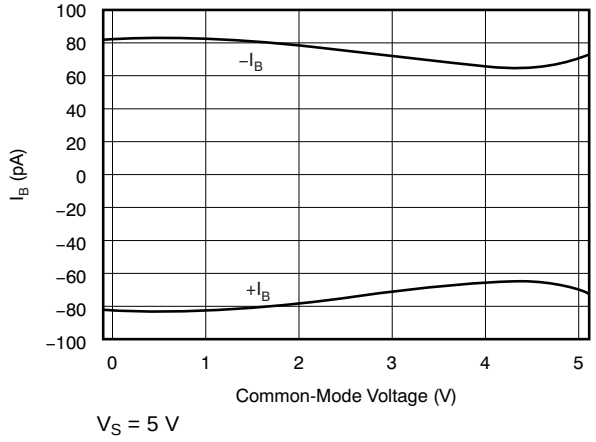


Figure 7. Input Bias Current vs Common-Mode Voltage

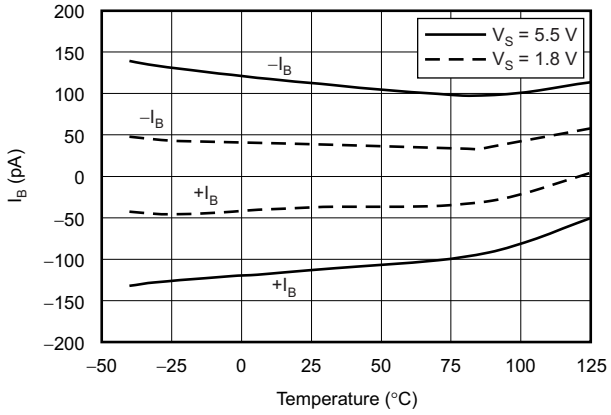


Figure 8. Input Bias Current vs Temperature

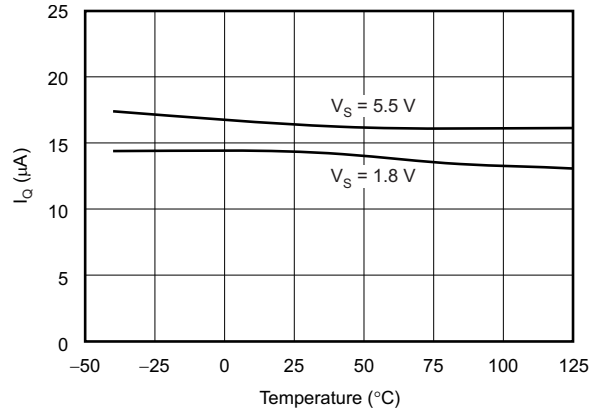


Figure 9. Quiescent Current vs Temperature

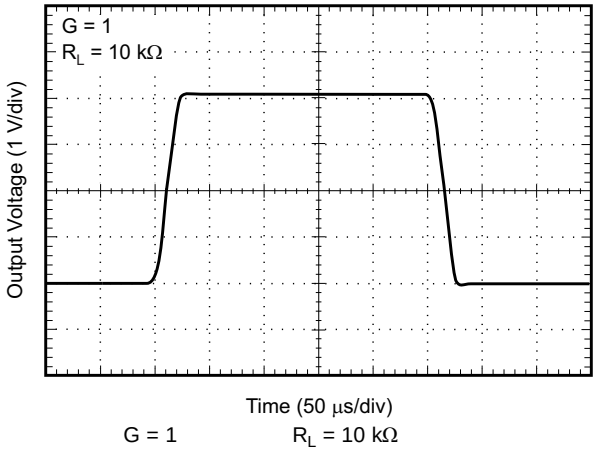


Figure 10. Large-Signal Step Response

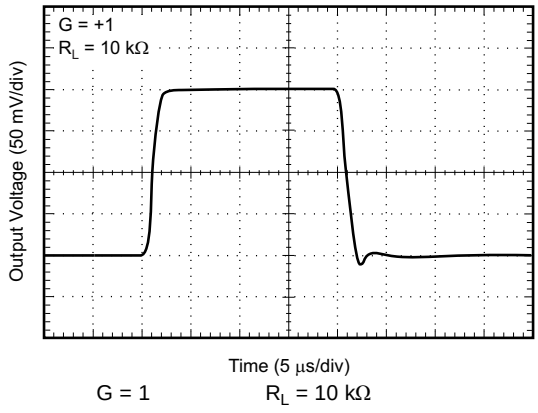


Figure 11. Small-Signal Step Response

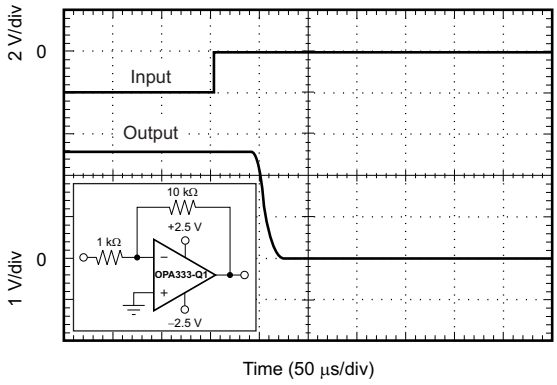


Figure 12. Positive Overvoltage Recovery

Typical Characteristics (continued)

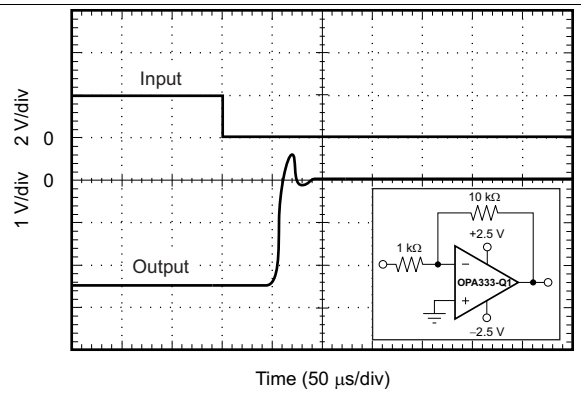


Figure 13. Negative Overvoltage Recovery

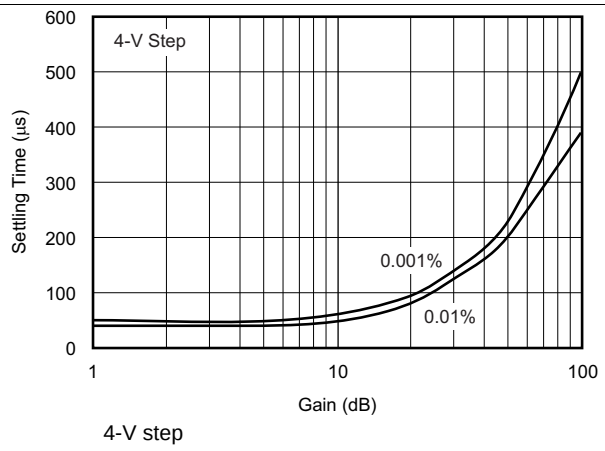


Figure 14. Settling Time vs Closed-Loop Gain

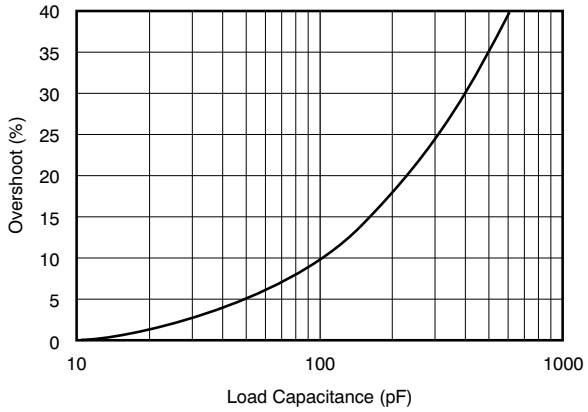


Figure 15. Small-Signal Overshoot vs Load Capacitance

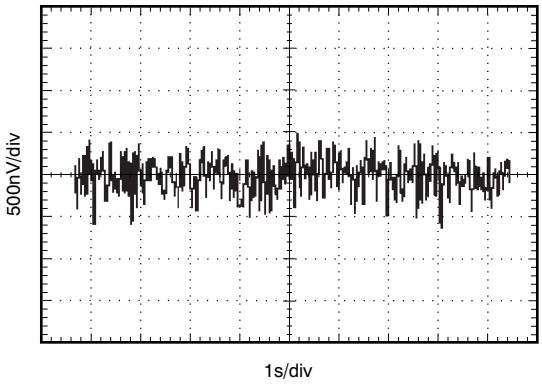


Figure 16. 0.1-Hz to 10-Hz Noise

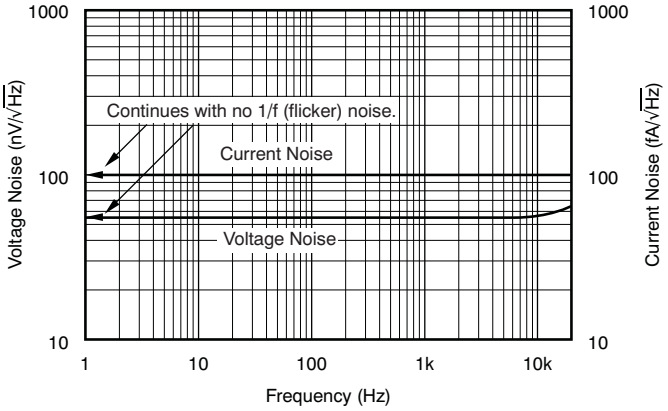


Figure 17. Current and Voltage Noise Spectral Density vs Frequency

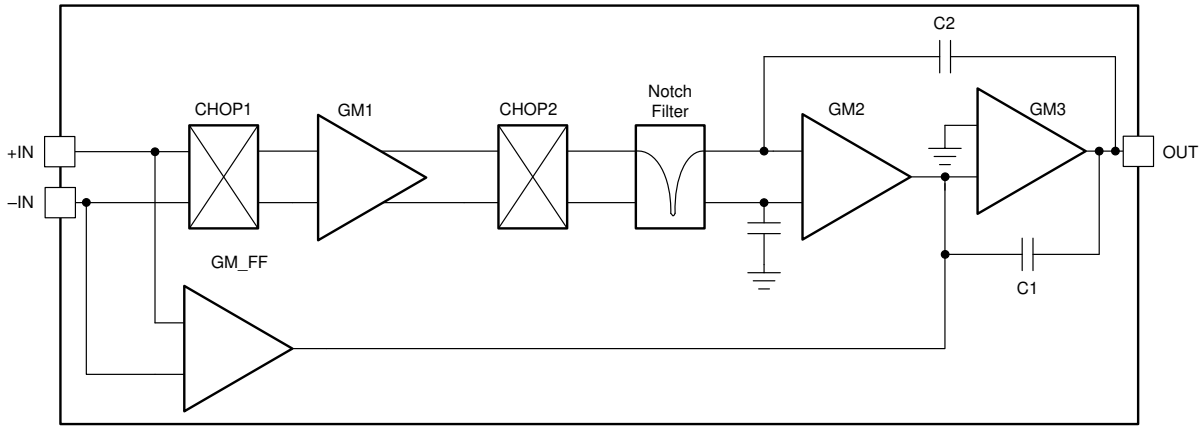
7 Detailed Description

7.1 Overview

The OPA333-Q1 device is a zero-drift, low-power, rail-to-rail input and output operational amplifier. The device operates from 1.8 V to 5.5 V, is unity-gain stable, and is designed for a wide range of general-purpose applications. The zero-drift architecture provides ultra-low offset voltage and near-zero offset voltage drift.

The OPA333-Q1 device is unity-gain stable and free from unexpected output phase reversal. The device uses a proprietary auto-calibration technique to provide low offset voltage and very-low drift over time and temperature.

7.2 Functional Block Diagram

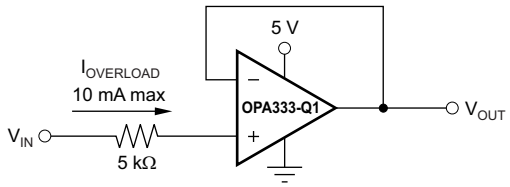


7.3 Feature Description

7.3.1 Rail-to-Rail Input Voltage

The OPA333-Q1 input common-mode voltage range extends 0.1 V beyond the supply rails. The OPA333-Q1 device is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Normally, input bias current is approximately 70 pA; however, input voltages exceeding the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor (see Figure 18).



(1) Current-limiting resistor required if input voltage exceeds supply rails by ≥0.5 V.

Figure 18. Input Current Protection

7.3.2 Internal Offset Correction

The OPA333-Q1 op amp uses an auto-calibration technique with a time-continuous 350-kHz op amp in the signal path. This amplifier is zero corrected every 8 μs using a proprietary technique. At power up, the amplifier requires approximately 100 μs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

7.4 Device Functional Modes

The OPA333-Q1 device has a single functional mode. The device is powered on as long as the power supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA333-Q1 is a unity-gain stable, precision operational amplifier with very low offset voltage drift. The device is also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins. In most cases, 0.1-μF capacitors are adequate.

8.1.1 Achieving Output Swing to the Op Amp Negative Rail

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp may swing close to single-supply ground, but will not reach ground. The output of the OPA333-Q1 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires the use of another resistor and an additional, more negative, power supply than the op amp negative supply. A pulldown resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve (see Figure 19).

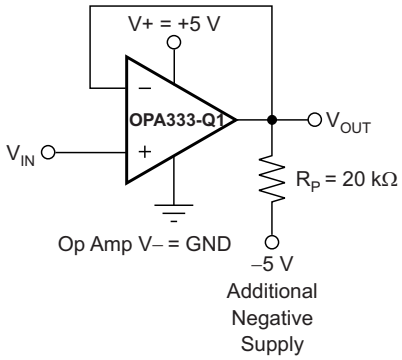


Figure 19. V_{OUT} Range to Ground

The OPA333-Q1 has an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The OPA333-Q1 has been characterized to perform with this technique; however, the recommended resistor value is approximately 20 kΩ.

NOTE

This configuration increases the current consumption by several hundreds of microamps.

Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occur below –2 mV, but excellent accuracy returns when the output is again driven above –2 mV. Lowering the resistance of the pulldown resistor allows the op amp to swing even further below the negative rail. Resistors as low as 10 kΩ can be used to achieve excellent accuracy down to –10 mV.

8.2 Typical Applications

8.2.1 High-Side Voltage-to-Current (V-I) Converter

The circuit shown in Figure 20 is a high-side voltage-to-current (V-I) converter. It translates in input voltage of 0 V to 2 V to and output current of 0 mA to 100 mA. Figure 21 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA333-Q1 device facilitate excellent dc accuracy for the circuit.

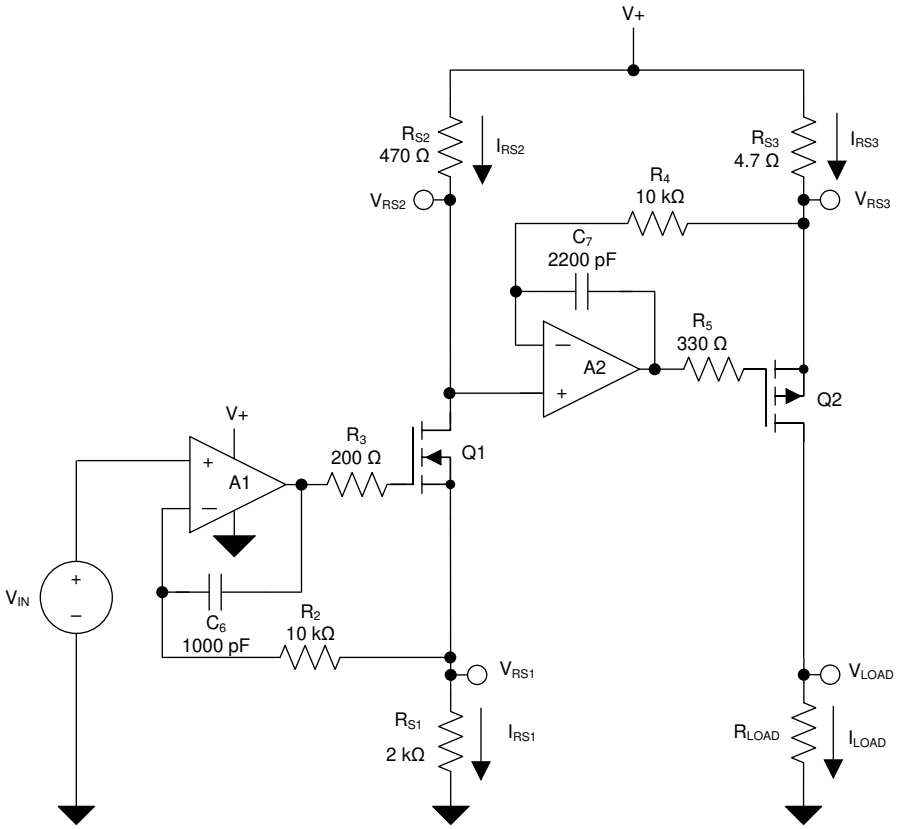


Figure 20. High-Side Voltage-to-Current (V-I) Converter

Typical Applications (continued)

8.2.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 5 V dc
- Input: 0 V to 2 V dc
- Output: 0 mA to 100 mA dc

8.2.1.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, and the three current sensing resistors, R_{S1}, R_{S2}, and R_{S3}. The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3}.

For a successful design, pay close attention to the dc characteristics of the operational amplifier chosen for the application. To meet the performance goals, this application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The OPA2333-Q1 CMOS operational amplifier is a high-precision, 5-µV offset, 0.05-µV/°C drift amplifier optimized for low-voltage, single-supply operation with an output swing to within 50 mV of the positive rail. The OPA2333-Q1 uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making these devices appropriate for precise dc control. The rail-to-rail output stage of the OPA2333-Q1 makes sure that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

A detailed error analysis, design procedure, and additional measured results are given in the *High-Side V-I Converter* reference design.

8.2.1.3 Application Curve

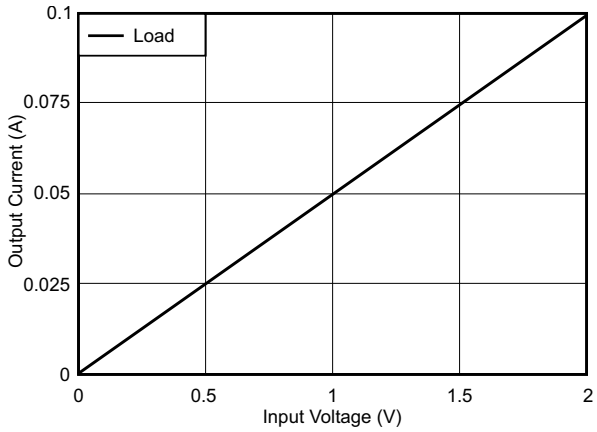


Figure 21. Measured Transfer Function for High-Side V-I Converter

Typical Applications (continued)

8.2.2 Precision, Low-Level Voltage-to-Current (V-I) Converter

The circuit shown in Figure 22 is a precision, low-level voltage-to-current (V-I) converter. The converter translates in input voltage of 0 V to 5 V and output current of 0 µA to 5 µA. Figure 23 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA333-Q1 facilitate excellent dc accuracy for the circuit. Figure 24 shows the calibrated error for the entire range of the circuit.

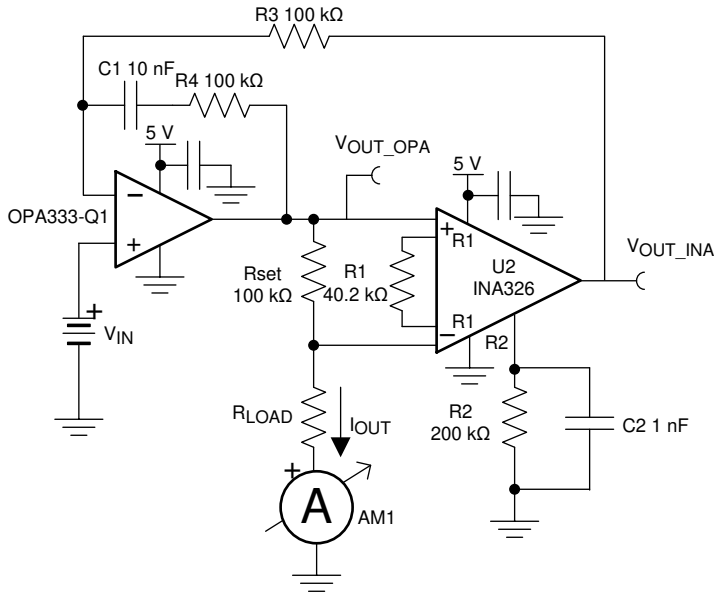


Figure 22. Low-Level, Precision V-I Converter

8.2.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 5 V dc
- Input: 0 V to 5 V dc
- Output: 0 µA to 5 µA dc

8.2.2.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, R_{SET}, and the instrumentation amplifier (INA) gain. During operation, the input voltage divided by the INA gain appears across the set resistor in Equation 1:

$$V_{SET} = V_{IN} / G_{INA} \quad (1)$$

The current through R_{SET} must flow through the load, so I_{OUT} is V_{SET} / R_{SET} × I_{OUT} remains a well-regulated current as long as the total voltage across R_{SET} and R_{LOAD} does not violate the output limits of the operational amplifier or the input common-mode limits of the INA. The voltage across the set resistor (V_{SET}) is the input voltage divided by the INA gain (that is, V_{SET} = 1 V / 10 = 0.1 V). The current is determined by V_{SET} and R_{SET} shown in Equation 2:

$$I_{OUT} = V_{SET} / R_{SET} = 0.1 \text{ V} / 100 \text{ k}\Omega = 1 \text{ µA} \quad (2)$$

A detailed error analysis, design procedure, and additional measured results are given in the *Low-Level V-to-I Converter* reference design.

Typical Applications (continued)

8.2.2.3 Application Curves

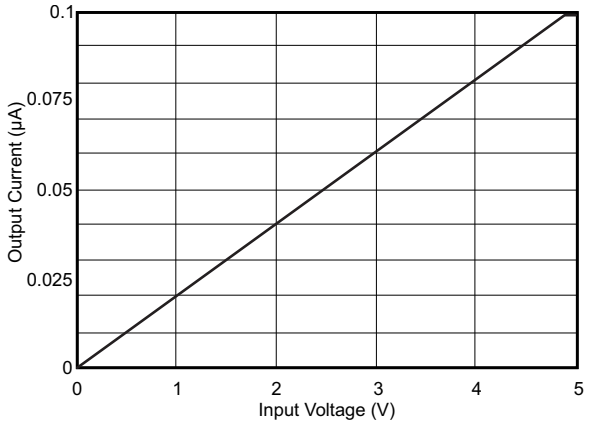


Figure 23. Measured Transfer Function for Low-Level Precision V-I

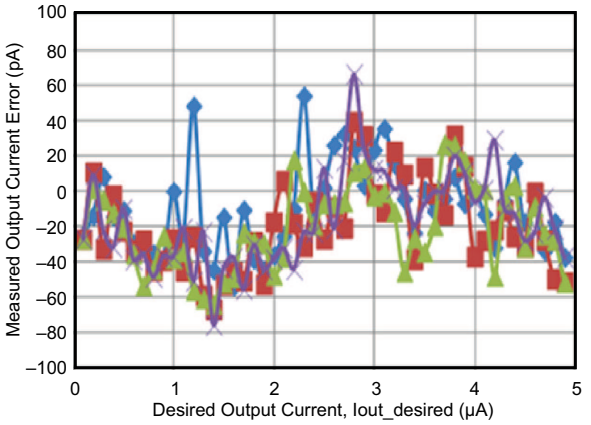


Figure 24. Calibrated Output Error for Low-Level V-I

8.2.3 Composite Amplifier

The circuit shown in Figure 25 is a composite amplifier used to drive the reference on the ADS8881. The OPA333-Q1 provides excellent dc accuracy, and the THS4281 allows the output of the circuit to respond quickly to the transient current requirements of a typical successive approximation register (SAR) data-converter reference input. The ADS8881 system was optimized for THD and achieved a measured performance of –110 dB. The linearity of the ADC is shown Figure 26.

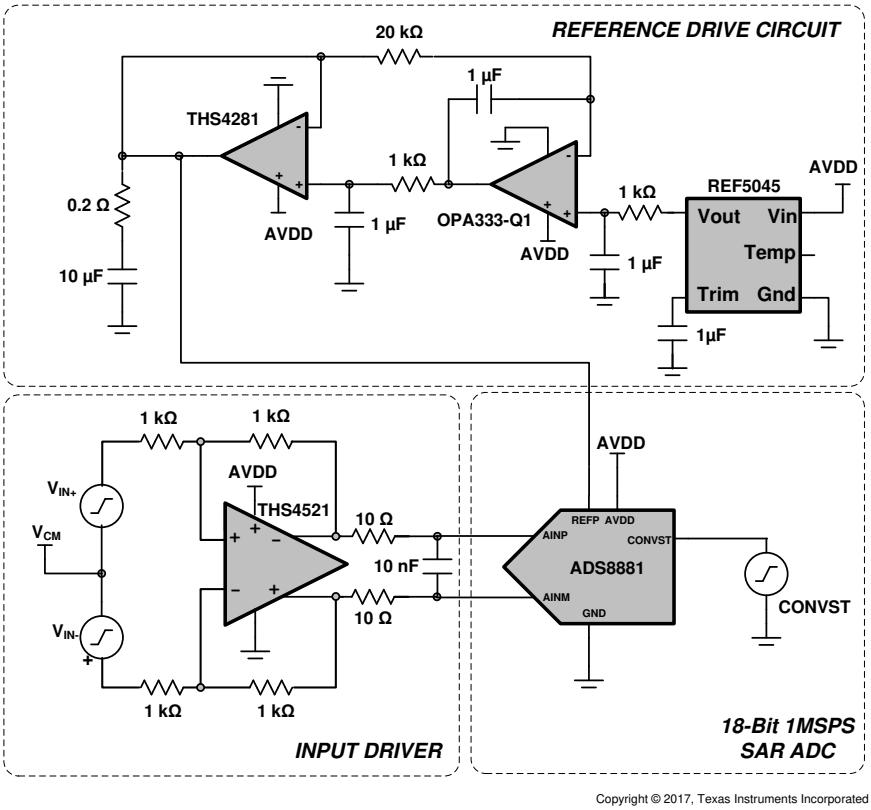


Figure 25. Composite Amplifier Reference Driver Circuit

Typical Applications (continued)

8.2.3.1 Design Requirements

The design requirements for this block design are:

- System supply voltage: 5 V dc
- ADC supply voltage: 3.3 V dc
- ADC sampling rate: 1 MSPS
- ADC reference voltage (VREF): 4.5 V dc
- ADC input signal: A differential input signal with amplitude of V_{pk} = 4.315 V (–0.4 dBFS to avoid clipping) and frequency of f_{IN} = 10 kHz are applied to each differential input of the ADC

8.2.3.2 Detailed Design Procedure

The two primary design considerations to maximize the performance of a high-resolution SAR ADC are the input driver and the reference driver design. The circuit comprises the critical analog circuit blocks, the input driver, antialiasing filter, and the reference driver. Each analog circuit block should be carefully designed based on the ADC performance specifications to maximize the distortion and noise performance of the data acquisition system while consuming low power. The diagram includes the most important specifications for each individual analog block. This design systematically approaches the design of each analog circuit block to achieve a 16-bit, low-noise and low-distortion data acquisition system for a 10-kHz sinusoidal input signal. The first step in the design requires an understanding of the requirements for an extremely low-distortion input-driver amplifier. This understanding helps in the decision of an appropriate input driver configuration and selection of an input amplifier to meet the system requirements. The next important step is the design of the antialiasing RC filter to attenuate ADC kickback noise while maintaining amplifier stability. The final design challenge is to design a high-precision reference driver circuit that provides the required-value V_{REF} with low offset, drift, and noise contributions.

When designing a very low-distortion data-acquisition block, make sure to understand the sources of nonlinearity. Both the ADC and the input driver introduce nonlinearity in a data-acquisition block. To achieve the lowest distortion, the input driver for a high-performance SAR ADC must have a distortion that is negligible against the ADC distortion. This parameter requires the input driver distortion to be 10 dB less than the ADC THD. This stringent requirement makes sure that the overall THD of the system is not degraded by more than –0.5 dB.

$$THD_{AMP} < THD_{ADC} - 10\ dB \quad (3)$$

Therefore, make sure to choose an amplifier that meets the previous criteria to avoid the system THD from being limited by the input driver. The amplifier nonlinearity in a feedback system depends on the available loop gain. A detailed error analysis, design procedure, and additional measured results are given in the *Data Acquisition Optimized for Lowest Distortion, Lowest Noise* reference design.

8.2.3.3 Application Curve

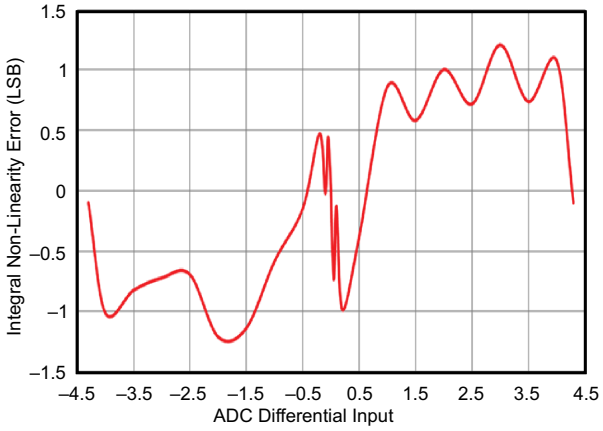


Figure 26. Linearity of the ADS8881 System

Typical Applications (continued)

8.2.4 Temperature Measurement

Figure 27 shows a temperature measurement application.

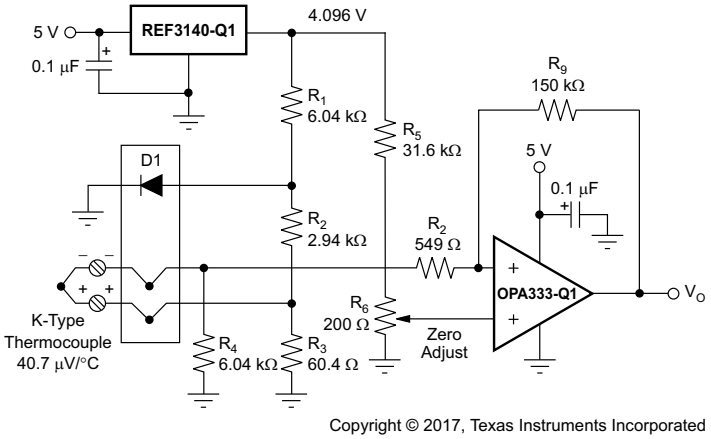


Figure 27. Temperature Measurement

8.2.5 Single Op-Amp Bridge-Amplifier

Figure 28 shows the basic configuration for a bridge amplifier.

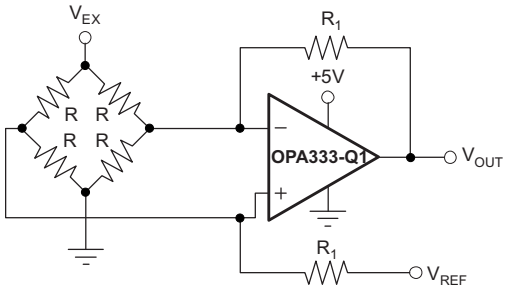
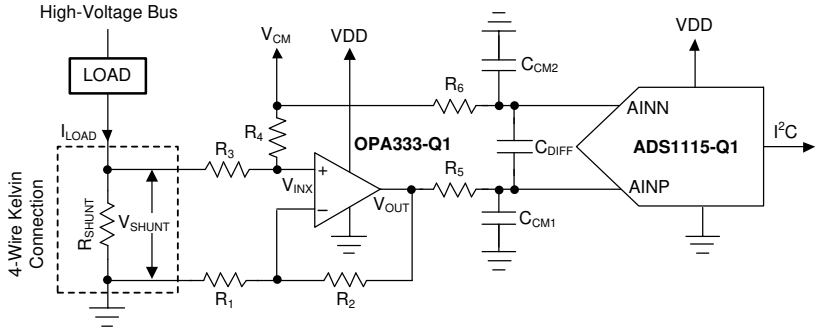


Figure 28. Single Op-Amp Bridge-Amplifier

8.2.6 Low-Side Current-Monitor

A low-side current shunt monitor is shown in Figure 29. The R_1 through R_6 resistors are operational resistors used to isolate the 16-bit ADS1115-Q1 converter from the noise of the digital I^2C bus.

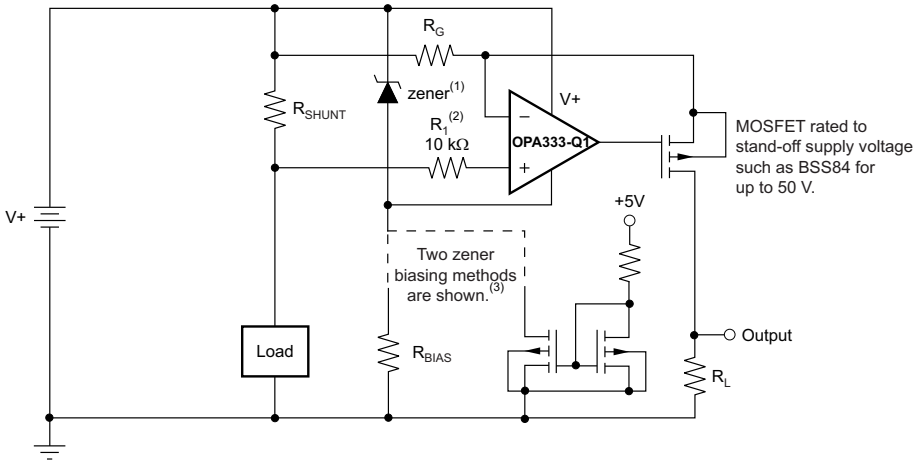


NOTE: 1% resistors provide adequate common-mode rejection at small ground-loop errors.

Figure 29. Low-Side Current-Monitor

Typical Applications (continued)

8.2.7 High-Side Current Monitor



(1) Zener rated for op amp supply capability (that is, 5.1 V for OPA333-Q1).

(2) Current-limiting resistor.

(3) Choose zener biasing resistor or dual N-MOSFETs (FDG6301N, NTJD4001N, or Si1034).

Figure 30. High-Side Current Monitor

8.2.8 Thermistor Measurement

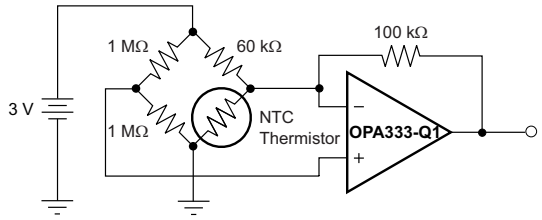


Figure 31. Thermistor Measurement

8.2.9 Precision Instrumentation Amplifier

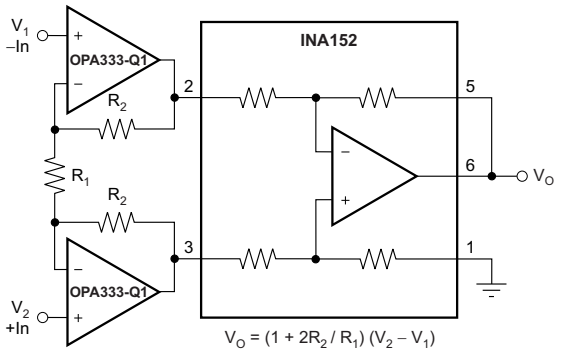


Figure 32. Precision Instrumentation Amplifier

9 Power Supply Recommendations

The OPA333-Q1 is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages greater than 7 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-μF bypass capacitors near the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more details on bypass capacitor placement, see the *Layout* section.

10 Layout

10.1 Layout Guidelines

Pay attention to good layout practices. Keep traces short and when possible, use a printed-circuit-board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-μF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Operational amplifiers vary in susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. The OPA333-Q1 is specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may still cause varying offset levels.

For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low-thermoelectric-coefficient connections (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 μV/°C or higher, depending on materials used.

10.2 Layout Example

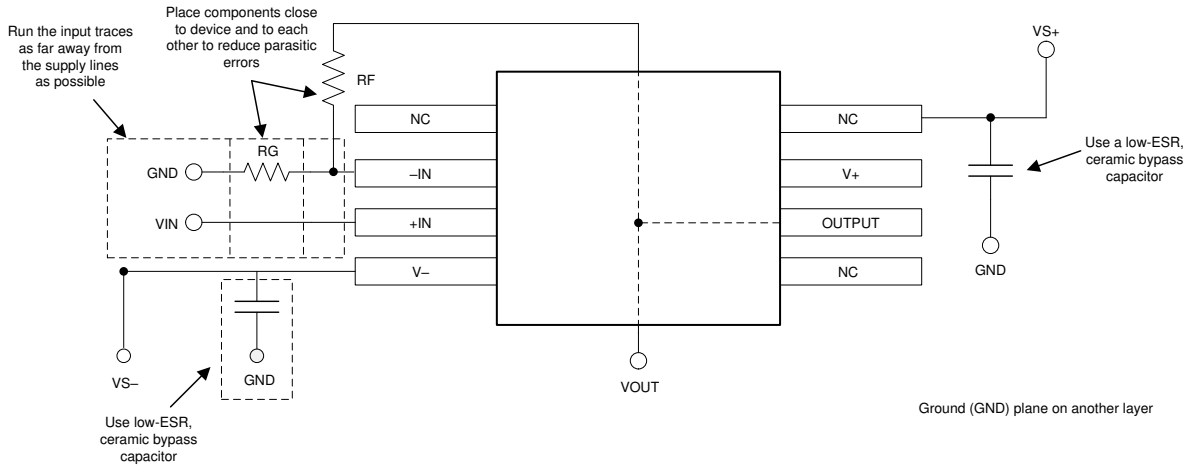


Figure 33. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise*
- Texas Instruments, ADS1100 *Self-Calibrating, 16-Bit Analog-to-Digital Converter*
- Texas Instruments, *ADS8881x 18-Bit, 1-MSPS, Serial Interface, microPower, Miniature, True-Differential Input, SAR Analog-to-Digital Converter*
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers (With OPA333 and OPA333-Q1 as an Example)*
- Texas Instruments, *High-Side Voltage-to-Current (V-I) Converter*
- Texas Instruments, INA152 *Single-Supply Difference Amplifier*
- Texas Instruments, *Low Level (5 μA) V-to-I Converter*
- Texas Instruments, *REF31xx-Q1 15 ppm/°C Maximum, 100-μA, SOT-23 Series Voltage Reference*
- Texas Instruments, *Single-Supply Operation Of Operational Amplifiers*
- Texas Instruments, *THS4281 Very Low-Power, High-Speed, Rail-to-Rail Input and Output Voltage-Feedback Operational Amplifier*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA333AQDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	QCNQ
OPA333AQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	QCNQ
OPA333AQDBVRQ1G4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QCNQ
OPA333AQDBVRQ1G4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QCNQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF OPA333-Q1 :

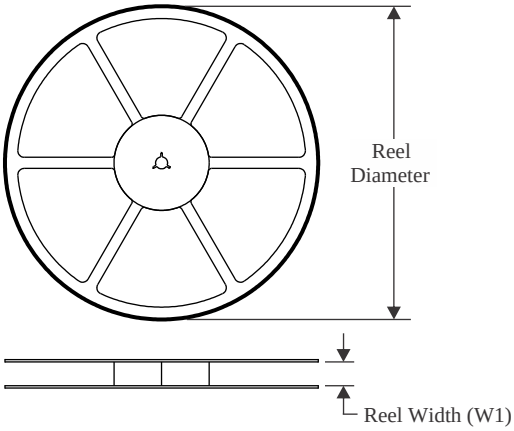
- Catalog : OPA333

NOTE: Qualified Version Definitions:

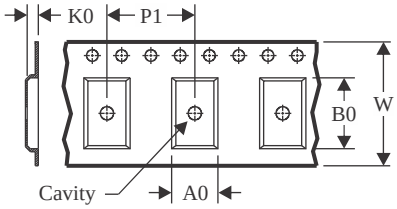
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

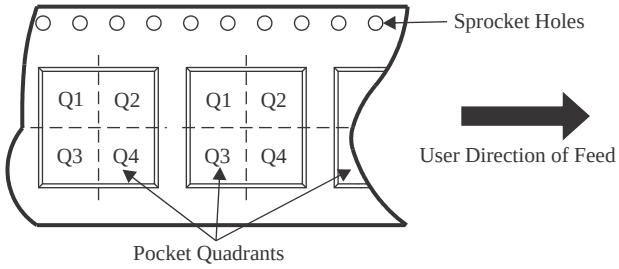


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

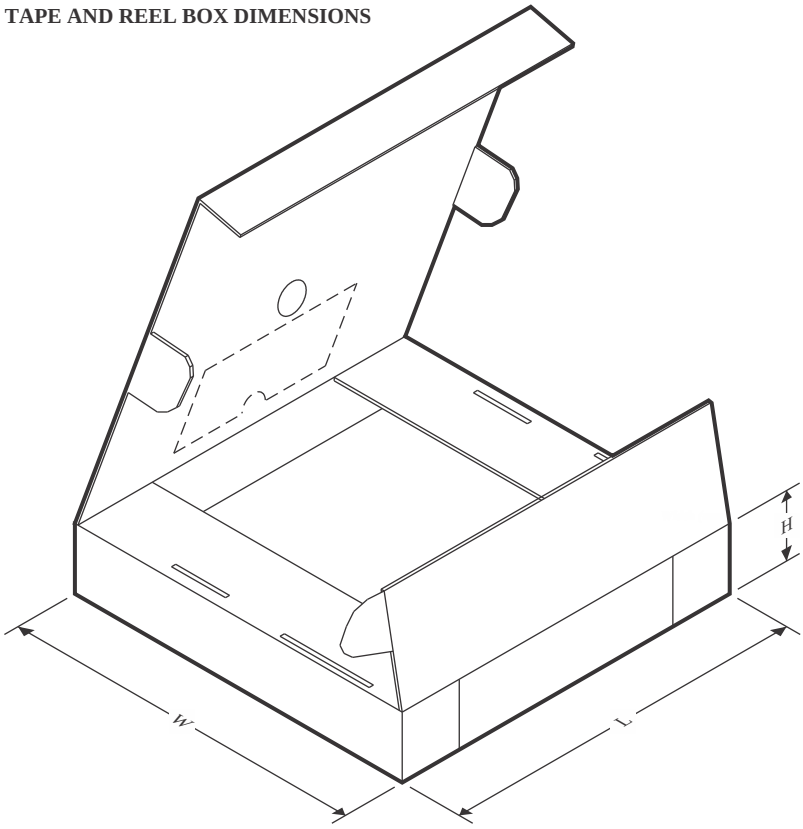
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA333AQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA333AQDBVRQ1G4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

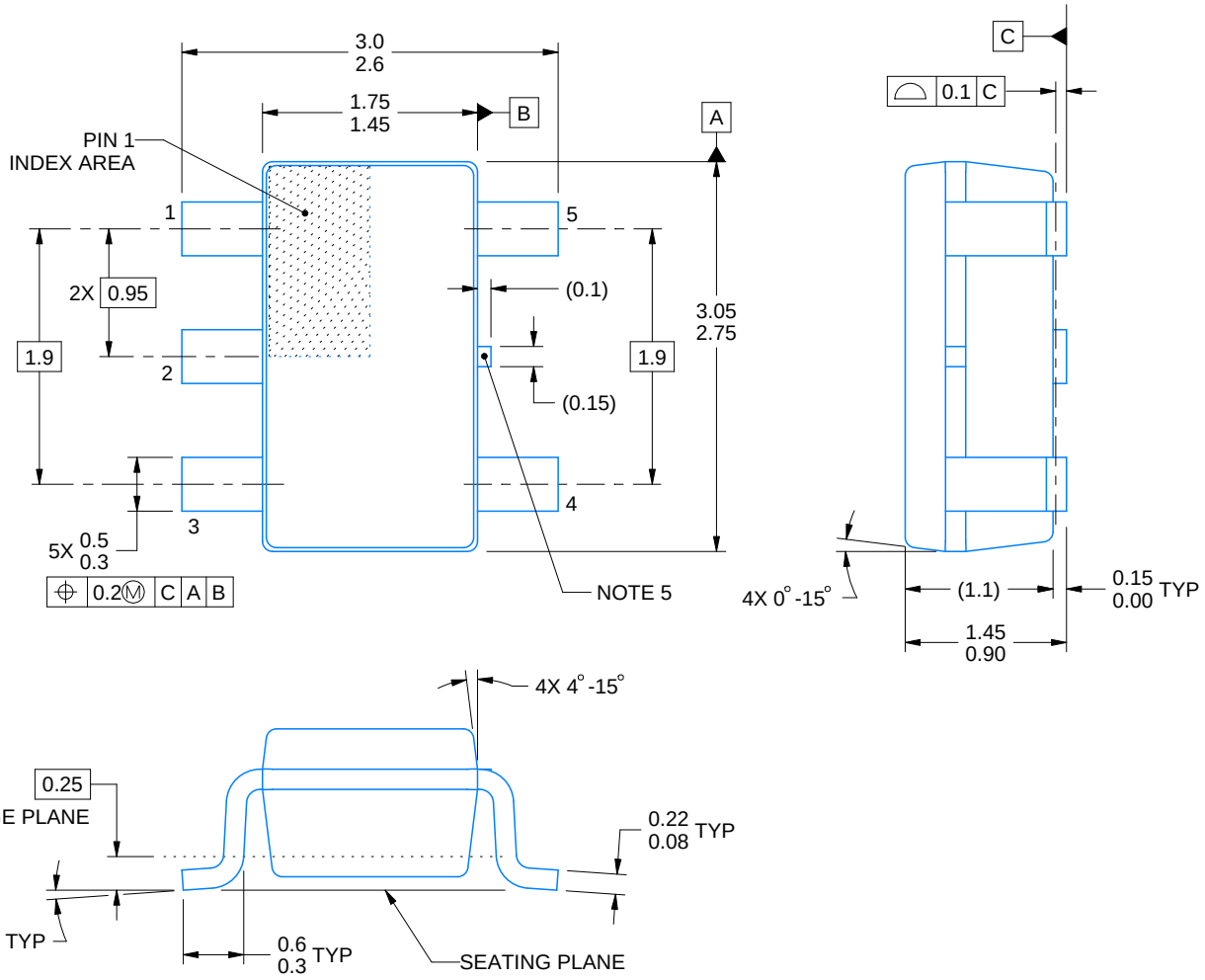
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA333AQDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
OPA333AQDBVRQ1G4	SOT-23	DBV	5	3000	200.0	183.0	25.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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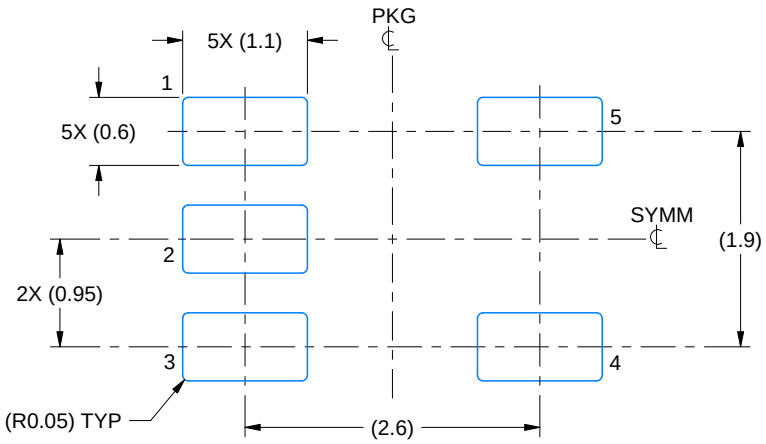
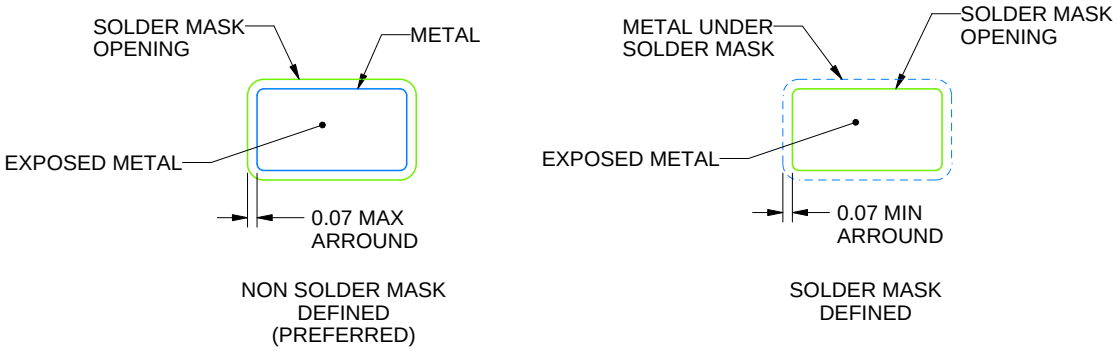
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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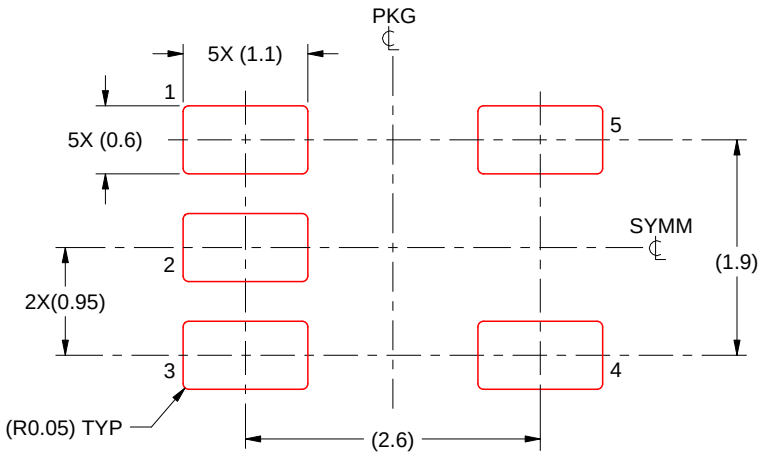
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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