Dual, Low-Power, High-Speed, Fixed-Gain Operational Amplifier

FEATURES

- HIGH BANDWIDTH: 75MHz (G = +2)
- LOW SUPPLY CURRENT: 7.8mA (V_S = +5V)
- FLEXIBLE SUPPLY RANGE:
  ±1.5V to ±5.5V Dual Supply
  +3V to +11V Single Supply
- INPUT RANGE INCLUDES GROUND ON SINGLE SUPPLY
- 4.9V_{PP} OUTPUT SWING ON +5V SUPPLY
- HIGH SLEW RATE: 350V/μs
- LOW INPUT VOLTAGE NOISE: 9.3nV/$\sqrt{Hz}$

APPLICATIONS

- SINGLE-SUPPLY VIDEO LINE DRIVERS
- CCD IMAGING CHANNELS
- LOW-POWER ULTRASOUND
- PORTABLE CONSUMER ELECTRONICS

DESCRIPTION

The OPA2832 is a dual, low-power, high-speed, fixed-gain amplifier designed to operate on a single +3V to +11V supply. Operation on ±1.5V to ±5.5V supplies is also supported. The input range extends below ground and to within 1.7V of the positive supply.

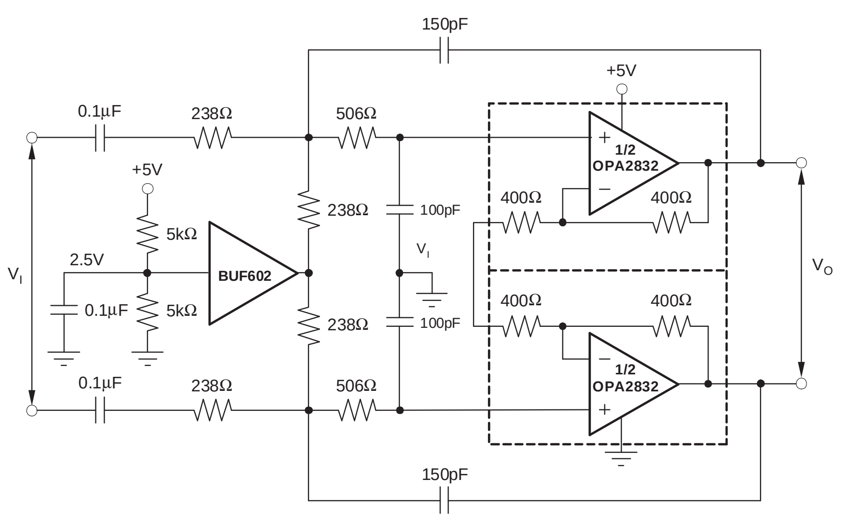
Using complementary common-emitter outputs provides an output swing to within 30mV of ground and 60mV of the positive supply. The high output drive current and low differential gain and phase errors also make it ideal for single-supply consumer video products.

Low distortion operation is ensured by high bandwidth product (75MHz) and slew rate (350V/μs), making the OPA2832 an ideal input buffer stage to 3V and 5V CMOS converters. Unlike earlier low-power, single-supply amplifiers, distortion performance improves as the signal swing is decreased. A low 9.3nV/$\sqrt{Hz}$ input voltage noise supports wide dynamic range operation.

The OPA2832 is available in an industry-standard SO-8 package or a small MSOP-8 package. For gains other than +1, –1, or +2, consider the OPA2830.

RELATED PRODUCTS

DESCRIPTION	SINGLES	DUALS	TRIPLES	QUADS
Rail-to-Rail Output	OPA830	OPA2830	—	OPA4830
Rail-to-Rail Fixed-Gain	OPA832	—	OPA3832	—
General-Purpose (1800V/μs slew rate)	OPA690	OPA2690	OPA3690	—
Low-Noise, High DC Precision	OPA820	OPA2822	—	OPA4820



Single-Supply, 3rd-Order, Differential Chebyshev Low-Pass Filter

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2832	SO-8 Surface-Mount	D	–40°C to +85°C	OPA2832	OPA2832ID	Rails, 100
					OPA2832IDR	Tape and Reel, 2500
OPA2832	MSOP-8	DGK	–40°C to +85°C	A61	OPA2832IDGK	Tape and Reel, 250
					OPA2832IDGKR	Tape and Reel, 2500

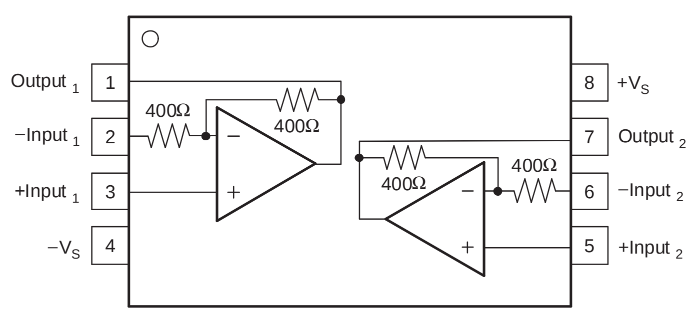
(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	$11V_{DC}$
Internal Power Dissipation	See Thermal Characteristics
Differential Input Voltage(2)	±1.2V
Input Voltage Range	–0.5V to $\pm V_S$ + 0.3V
Storage Voltage Range: D, DGK	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating:	
Human Body Model (HBM)	2000V
Charge Device Model (CDM)	1000V
Machine Model (MM)	200V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Noninverting input to internal inverting mode.

Top View **SO, MSOP**



ELECTRICAL CHARACTERISTICS: V_S = ±5V

Boldface limits are tested at **+25C**.

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to GND, unless otherwise noted (see Figure 63).

PARAMETER	CONDITIONS	OPA2832ID, IDGK +25°C	+25°C[1]	0°C to +70°C[2]	–40°C to +85°C[2]	UNITS	MIN/ MAX	TEST LEVEL[3]
AC PERFORMANCE (see Figure 63)								
Small-Signal Bandwidth	G = +1, V_O ≤ 0.5V_{PP}	250				MHz	typ	V
	G = +2, V_O ≤ 0.5V_{PP}	70	55	54	54	MHz	min	B
	G = –1, V_O ≤ 0.5V_{PP}	85	57	56	55	MHz	min	B
Peaking at a Gain of +1	V_O ≤ 0.5V_{PP}	6				dB	typ	C
Slew Rate	G = +2, 2V Step	300	220	210	200	V/µs	min	B
Rise Time	0.5V Step	5.6	5.8	6.0	6.0	ns	max	B
Fall Time	0.5V Step	5.6	5.8	6.0	6.0	ns	max	B
Settling Time to 0.1%	G = +2, 1V Step	45	63	65	66	ns	max	B
Harmonic Distortion	V_O = 2V_{PP}, 5MHz							
2nd-Harmonic	R_L = 150Ω	–64	–60	–58	–58	dBc	max	B
	R_L = 500Ω	–66	–63	–61	–61	dBc	max	B
3rd-Harmonic	R_L = 150Ω	–57	–50	–49	–48	dBc	max	B
	R_L = 500Ω	–73	–64	–60	–57	dBc	max	B
Input Voltage Noise	f > 1MHz	9.2				nV/√Hz	typ	C
Input Current Noise	f > 1MHz	2.2				pA/√Hz	typ	C
NTSC Differential Gain	R_L = 150Ω	0.10				%	typ	C
NTSC Differential Phase	R_L = 150Ω	0.16				°	typ	C
DC PERFORMANCE[4]								
Gain Error	G = +2	±0.3	**±1.5**	±1.6	±1.7	%	min	A
	G = –1	±0.2	±1.5	±1.6	±1.7	%	max	B
Internal R_F and R_G								
Maximum		400	**455**	460	462	Ω	max	A
Minimum		400	**345**	340	338	Ω	max	A
Average Drift				±0.1	±0.1	%/°C	max	B
Input Offset Voltage		±1.4	**±7.5**	±8.7	±9.3	mV	max	A
Average Offset Voltage Drift		—		±27	±27	µV/°C	max	B
Input Bias Current		+5.5	**+10**	+12	+13	µA	max	A
Input Bias Current Drift		—		±45	±45	nA/°C	max	B
Input Offset Current		±0.1	**±1.5**	±2	±2.5	µA	max	A
Input Offset Current Drift		—		±10	±10	nA/°C	max	B
INPUT								
Negative Input Voltage Range		–5.4	–5.2	–5.0	–4.9	V	max	B
Positive Input Voltage Range		3.2	3.1	3.0	2.9	V	min	B
Input Impedance								
Differential Mode		10 || 2.1				kΩ || pF	typ	C
Common-Mode		400 || 1.2				kΩ || pF	typ	C
OUTPUT								
Output Voltage Swing	R_L = 1kΩ to GND	±4.9	**±4.8**	±4.75	±4.75	V	max	A
	R_L = 150Ω to GND	±4.6	**±4.5**	±4.45	±4.4	V	max	A
Current Output, Sinking and Sourcing		±82	**±63**	±58	±53	mA	min	A
Short-Circuit Current	Output Shorted to Either Supply	120				mA	typ	C
Closed-Loop Output Impedance	G = +2, f ≤ 100kHz	0.2				Ω	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +5°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of node.

ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

Boldface limits are tested at **+25C**.
At T_A = +25°C, G = +2V/V, and R_L = 150Ω to GND, unless otherwise noted (see Figure 63).

PARAMETER	CONDITIONS	OPA2832ID, IDGK +25°C	+25°C (1)	0°C to +70°C (2)	–40°C to +85°C (2)	UNITS	MIN/ MAX	TEST LEVEL (3)
POWER SUPPLY								
Minimum Operating Voltage		±1.4				V	min	B
Maximum Operating Voltage		—	**±5.5**	±5.5	±5.5	V	max	A
Maximum Quiescent Current	V_S = ±5V	8.5	**9.5**	10.7	11.9	mA	max	A
Minimum Quiescent Current	V_S = ±5V	8.5	**8.0**	7.2	6.6	mA	min	A
Power-Supply Rejection Ratio (PSRR)	Input-Referred	66	**61**	60	59	dB	min	A
THERMAL CHARACTERISTICS								
Specification: ID, IDGK		–40 to +85				°C	typ	C
Thermal Resistance								
D SO-8		125				°C/W	typ	C
DGK MSOP-8		150				°C/W	typ	C

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C**.

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_{CM} = 2V, unless otherwise noted (see Figure 61).

PARAMETER	CONDITIONS	OPA2832ID, IDGK +25°C	+25°C(1)	0°C to +70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	TEST LEVEL(3)
AC PERFORMANCE (see Figure 61)								
Small-Signal Bandwidth	G = +1, V_O ≤ 0.5V_{PP}	210				MHz	typ	C
	G = +2, V_O ≤ 0.5V_{PP}	75	56	55	55	MHz	min	B
	G = –1, V_O ≤ 0.5V_{PP}	95	60	58	58	MHz	min	B
Peaking at a Gain of +1	V_O ≤ 0.5V_{PP}	7				dB	typ	C
Slew Rate	G = +2, 2V Step	320	230	220	220	V/µs	min	B
Rise Time	0.5V Step	4.8	5.8	5.8	5.9	ns	max	B
Fall Time	0.5V Step	4.8	5.8	5.8	5.9	ns	max	B
Settling Time to 0.1%	G = +2, 1V Step	46	64	66	67	ns	max	B
Harmonic Distortion	V_O = 2V_{PP}, 5MHz							
2nd-Harmonic	R_L = 150Ω	–59	–56	–54	–53	dBc	max	B
	R_L = 500Ω	–62	–59	–57	–57	dBc	max	B
3rd-Harmonic	R_L = 150Ω	–56	–50	–49	–47	dBc	max	B
	R_L = 500Ω	–72	–65	–62	–58	dBc	max	B
Input Voltage Noise	f > 1MHz	9.3				nV/√Hz	typ	C
Input Current Noise	f > 1MHz	2.3				pA/√Hz	typ	C
NTSC Differential Gain	R_L = 150Ω	0.11				%	typ	C
NTSC Differential Phase	R_L = 150Ω	0.14				°	typ	C
DC PERFORMANCE(4)								
Gain Error	G = +2	±0.3	**±1.5**	±1.6	±1.7	%	min	A
	G = –1	±0.2	±1.5	±1.6	±1.7	%	max	B
Internal R_F and R_G, Maximum		400	**455**	460	462	Ω	max	A
Minimum		400	**345**	340	338	Ω	max	A
Average Drift				±0.1	±0.1	%/°C	max	B
Input Offset Voltage		±1.5	**±6**	±7	±7.5	mV	max	A
Average Offset Voltage Drift		—		±20	±20	µV/°C	max	B
Input Bias Current	V_{CM} = 2.0V	+5.5	**+10**	+12	+13	µA	max	A
Input Bias Current Drift		—		±45	±45	nA/°C	max	B
Input Offset Current	V_{CM} = 2.0V	±0.1	**±1.5**	±2	±2.5	µA	max	A
Input Offset Current Drift		—		±10	±10	nA/°C	max	B
INPUT								
Least Positive Input Voltage		–0.5	–0.2	0	+0.1	V	max	B
Most Positive Input Voltage		3.3	3.2	3.1	3.0	V	min	B
Input Impedance, Differential Mode		10 || 2.1				kΩ || pF	typ	C
Common-Mode		400 || 1.2				kΩ || pF	typ	C
OUTPUT								
Least Positive Output Voltage	R_L = 1kΩ to 2.0V	0.03	**0.16**	0.18	0.20	V	max	A
	R_L = 150Ω to 2.0V	0.18	**0.3**	0.35	0.40	V	max	A
Most Positive Output Voltage	R_L = 1kΩ to 2.0V	4.94	**4.8**	4.6	4.4	V	min	A
	R_L = 150Ω to 2.0V	4.86	**4.6**	4.5	4.4	V	min	A
Current Output, Sinking and Sourcing		±75	**±58**	±53	±50	mA	min	A
Short-Circuit Output Current	Output Shorted to Either Supply	100				mA	typ	C
Closed-Loop Output Impedance	G = +2, f ≤ 100kHz	0.2				Ω	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +5°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of node.

ELECTRICAL CHARACTERISTICS: V_S = +5V (continued)

Boldface limits are tested at **+25°C**.
At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_{CM} = 2V, unless otherwise noted (see Figure 61).

		OPA2832ID, IDGK						
PARAMETER	CONDITIONS	+25°C	+25°C (1)	0°C to +70°C (2)	–40°C to +85°C (2)	UNITS	MIN/ MAX	TEST LEVEL (3)
POWER SUPPLY								
Minimum Operating Voltage		+2.8				V	typ	C
Maximum Operating Voltage		—	**+11**	+11	+11	V	max	A
Maximum Quiescent Current	V_S = +5V	7.8	**8.4**	9.8	11.2	mA	max	A
Minimum Quiescent Current	V_S = +5V	7.8	**7.4**	7.0	6.4	mA	min	A
Power-Supply Rejection Ratio (PSRR)	Input-Referred	66	**61**	60	59	dB	min	A
THERMAL CHARACTERISTICS								
Specification: ID, IDGK		–40 to +85				°C	typ	C
Thermal Resistance								
D SO-8		125				°C/W	typ	C
DGK MSOP-8		150				°C/W	typ	C

ELECTRICAL CHARACTERISTICS: V_S = +3.3V

Boldface limits are tested at **+25°C**.

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_{CM} = 0.75V, unless otherwise noted (see Figure 62).

PARAMETER	CONDITIONS	OPA2832ID, IDGK +25°C	+25°C(1)	0°C to +70°C(2)	UNITS	MIN/ MAX	TEST LEVEL(3)
AC PERFORMANCE (see Figure 62)							
Small-Signal Bandwidth	G = +1, V_O ≤ 0.5V_{PP}	180			MHz	typ	C
	G = +2, V_O ≤ 0.5V_{PP}	85	59	57	MHz	min	B
	G = –1, V_O ≤ 0.5V_{PP}	100	63	61	MHz	min	B
Peaking at a Gain of +1	V_O ≤ 0.5V_{PP}	8			dB	typ	C
Slew Rate	1V Step	130	110	100	V/μs	min	B
Rise Time	0.5V Step	4.6	5.6	5.7	ns	max	B
Fall Time	0.5V Step	4.6	5.6	5.7	ns	max	B
Settling Time to 0.1%	1V Step	48	70	80	ns	max	B
Harmonic Distortion	5MHz						
2nd-Harmonic	R_L = 150Ω	–71	–64	–61	dBc	max	B
	R_L = 500Ω	–74	–70	–64	dBc	max	B
3rd-Harmonic	R_L = 150Ω	–66	–60	–55	dBc	max	B
	R_L = 500Ω	–69	–66	–62	dBc	max	B
Input Voltage Noise	f > 1MHz	9.4			nV/√Hz	typ	C
Input Current Noise	f > 1MHz	2.4			pA/√Hz	typ	C
DC PERFORMANCE(4)							
Gain Error	G = +2	±0.3	**±1.5**	±1.6	%	min	A
	G = –1	±0.2	±1.5	±1.6	%	max	B
Internal R_F and R_G							
Maximum		400	**455**	460	Ω	max	A
Minimum		400	**345**	340	Ω	max	A
Average Drift				±0.1	%/°C	max	B
Input Offset Voltage		±1.4	**±7.5**	±8.7	mV	max	A
Average Offset Voltage Drift		—		±27	μV/°C	max	B
Input Bias Current	V_{CM} = 0.75V	+5.5	**+10**	+12	μA	max	A
Input Bias Current Drift		—		±45	nA/°C	max	B
Input Offset Current	V_{CM} = 0.75V	±0.1	**±1.5**	±2	μA	max	A
Input Offset Current Drift		—		±10	nA/°C	max	B
INPUT							
Least Positive Input Voltage		–0.5	–0.3	–0.2	V	max	B
Most Positive Input Voltage		1.5	1.4	1.3	V	min	B
Input Impedance							
Differential Mode		10 || 2.1			kΩ || pF	typ	C
Common-Mode		400 || 1.2			kΩ || pF	typ	C
OUTPUT							
Least Positive Output Voltage	R_L = 1kΩ to 0.75V	0.03	0.16	0.18	V	max	B
	R_L = 150Ω to 0.75V	0.1	0.3	0.35	V	max	B
Most Positive Output Voltage	R_L = 1kΩ to 0.75V	3	2.8	2.6	V	min	B
	R_L = 150Ω to 0.75V	3	2.8	2.6	V	min	B
Current Output, Sinking and Sourcing		±35	**±25**	±20	mA	min	A
Short-Circuit Output Current	Output Shorted to Either Supply	80			mA	typ	C
Closed-Loop Output Impedance	See Figure 2, f < 100kHz	0.2			Ω	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +5°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of node.

ELECTRICAL CHARACTERISTICS: V_S = +3.3V (continued)

Boldface limits are tested at **+25°C**.
At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_{CM} = 0.75V, unless otherwise noted (see Figure 62).

PARAMETER	CONDITIONS	OPA2832ID, IDGK +25°C	+25°C (1)	0°C to +70°C (2)	UNITS	MIN/ MAX	TEST LEVEL (3)
POWER SUPPLY							
Minimum Operating Voltage		+2.8			V	typ	C
Maximum Operating Voltage		–	**+11**	+11	V	max	A
Maximum Quiescent Current	V_S = +3.3V	7.6	**8.1**	9.5	mA	max	A
Minimum Quiescent Current	V_S = +3.3V	7.6	**6.8**	6.2	mA	min	A
Power-Supply Rejection Ratio (PSRR)	Input-Referred	60			dB	typ	C
THERMAL CHARACTERISTICS							
Specification: ID, IDGK		–40 to +85			°C	typ	C
Thermal Resistance							
D SO-8		125			°C/W	typ	C
DGK MSOP-8		150			°C/W	typ	C

TYPICAL CHARACTERISTICS: V_S = ±5V

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to GND, unless otherwise noted (see Figure 63).

SMALL-SIGNAL FREQUENCY RESPONSE

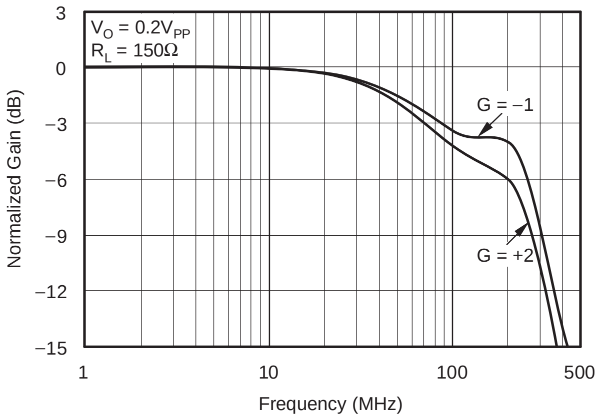


Figure 1.

LARGE-SIGNAL FREQUENCY RESPONSE

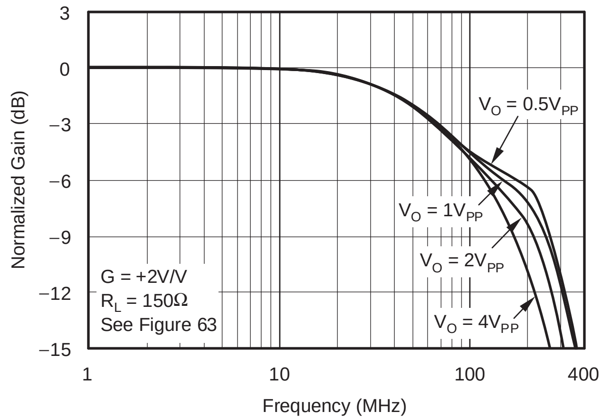


Figure 2.

SMALL-SIGNAL PULSE RESPONSE

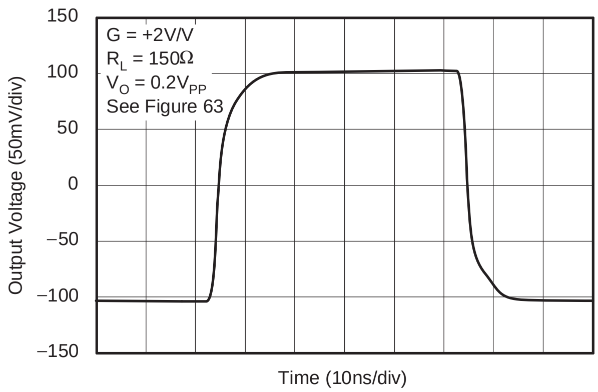


Figure 3.

LARGE-SIGNAL PULSE RESPONSE

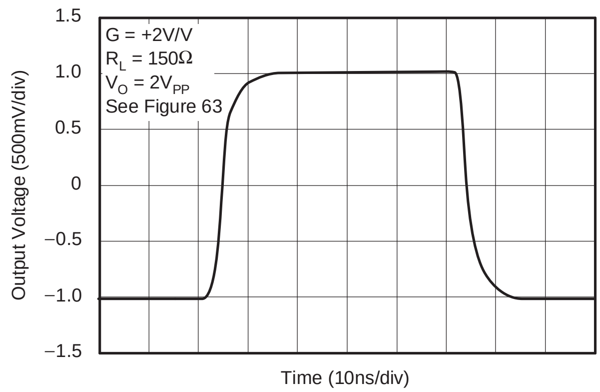


Figure 4.

REQUIRED R_S vs CAPACITIVE LOAD

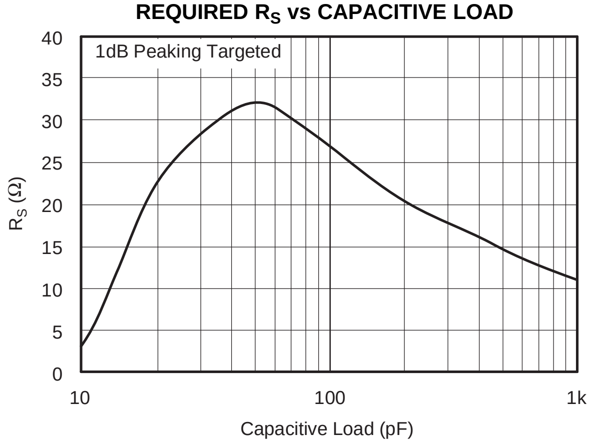


Figure 5.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

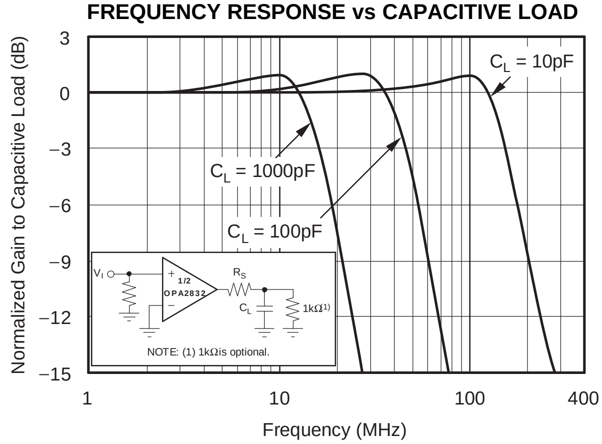


Figure 6.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to GND, unless otherwise noted (see Figure 63).

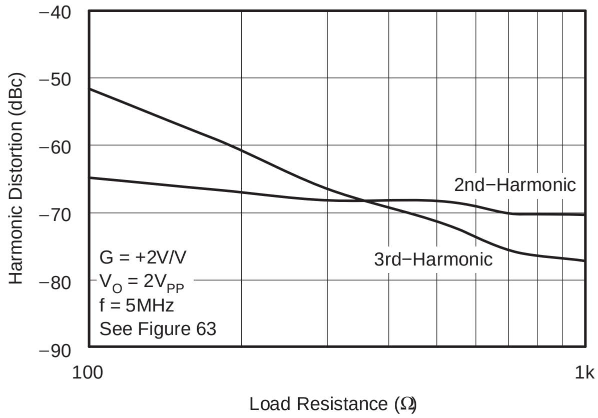


Figure 7.

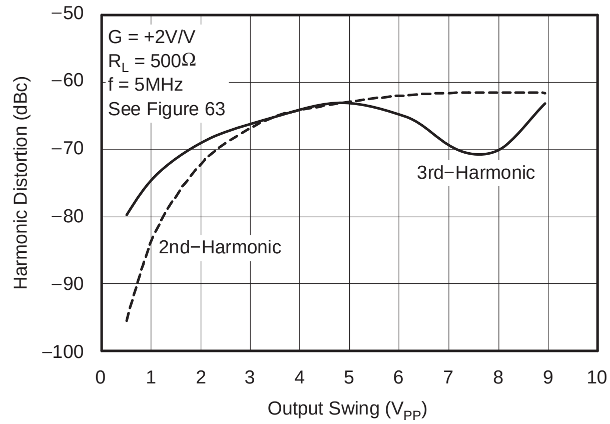


Figure 8.

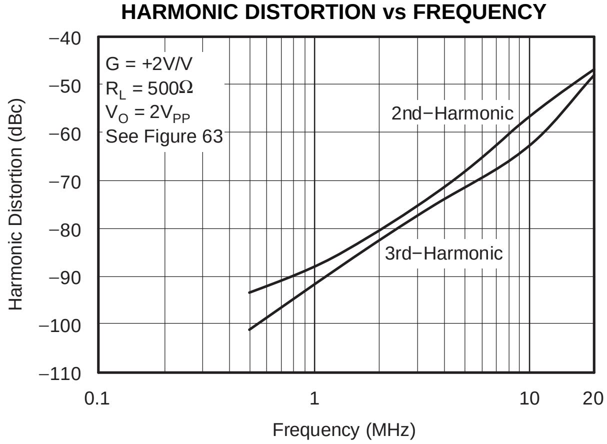


Figure 9.

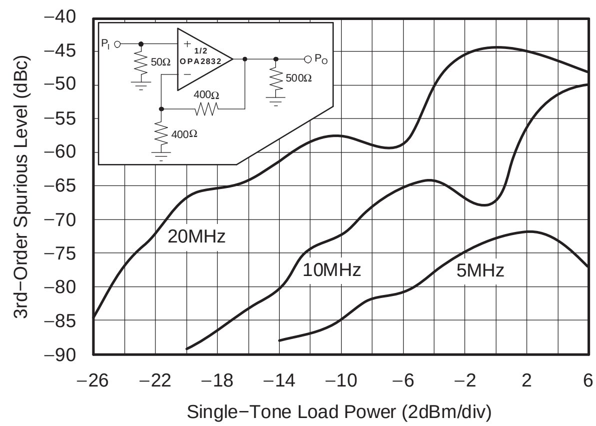


Figure 10.

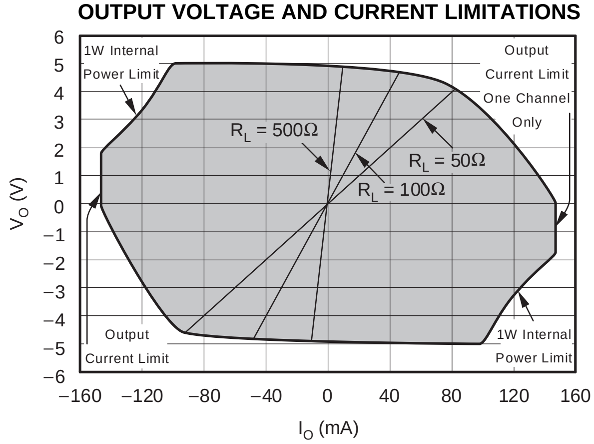


Figure 11.

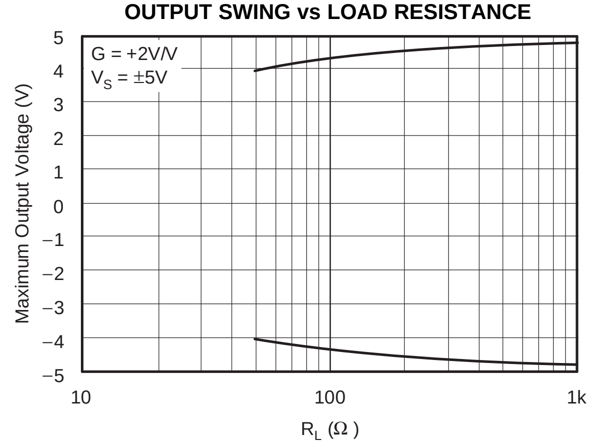


Figure 12.

TYPICAL CHARACTERISTICS: V_S = ±5V (Differential)

At T_A = +25°C, Differential Gain = +2V/V, and R_L = 500Ω, unless otherwise noted.

DIFFERENTIAL PERFORMANCE TEST CIRCUIT

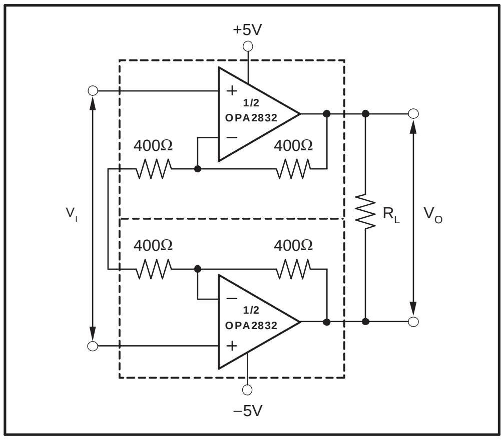


Figure 13.

SMALL-SIGNAL FREQUENCY RESPONSE

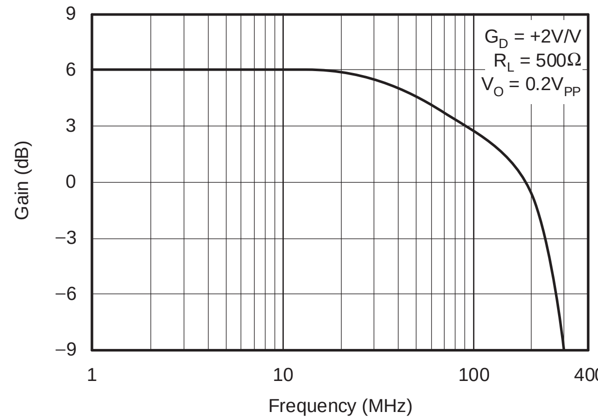


Figure 14.

LARGE-SIGNAL FREQUENCY RESPONSE

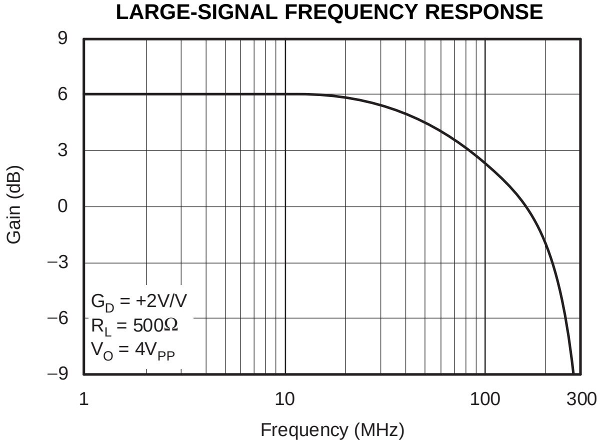


Figure 15.

HARMONIC DISTORTION vs FREQUENCY

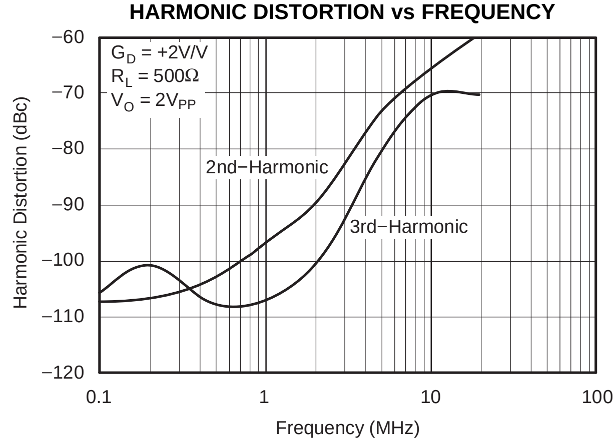


Figure 16.

HARMONIC DISTORTION vs OUTPUT SWING

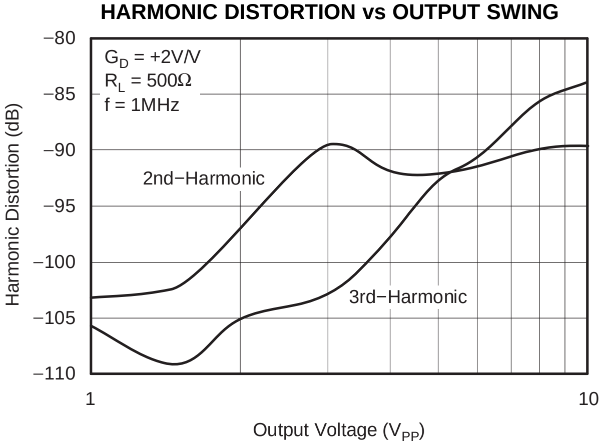


Figure 17.

HARMONIC DISTORTION vs LOAD RESISTANCE

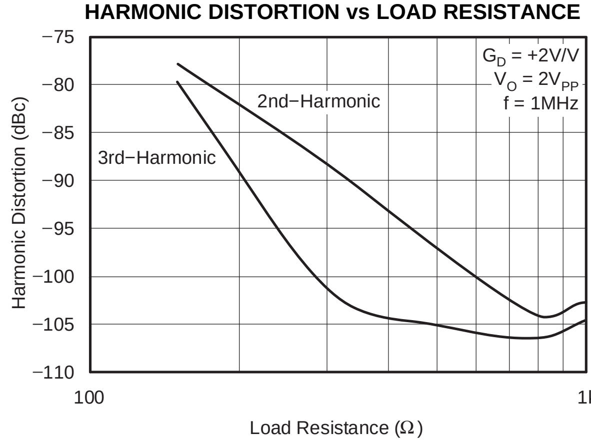


Figure 18.

TYPICAL CHARACTERISTICS: V_S = +5V

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_{CM} = 2V, unless otherwise noted (see Figure 61).

SMALL-SIGNAL FREQUENCY RESPONSE

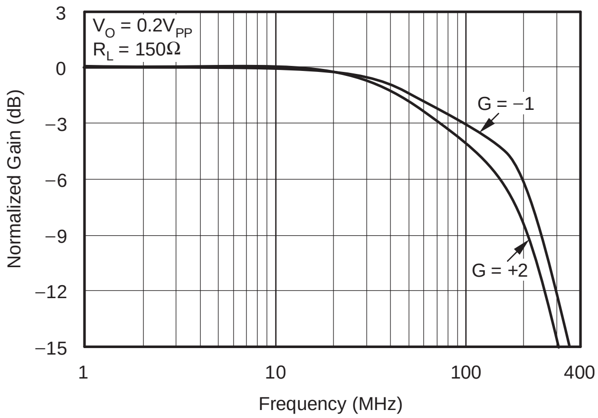


Figure 19.

LARGE-SIGNAL FREQUENCY RESPONSE

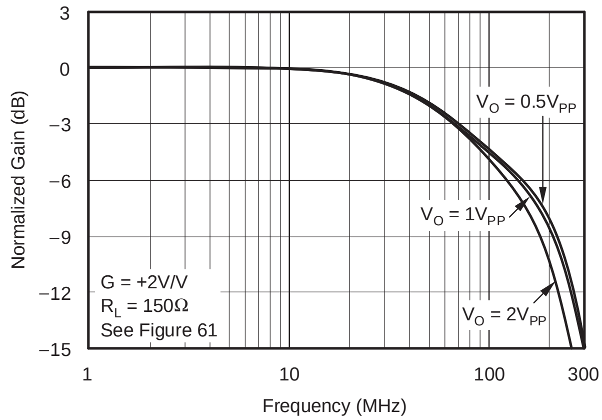


Figure 20.

SMALL-SIGNAL PULSE RESPONSE

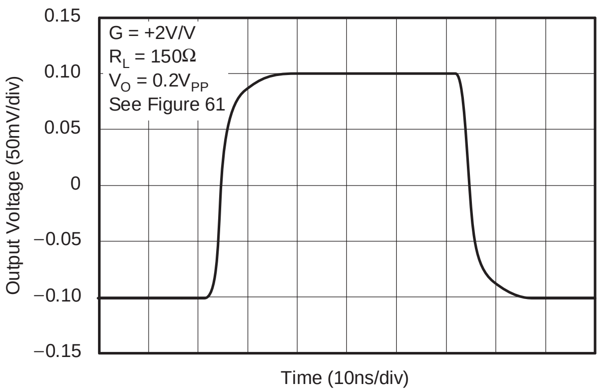


Figure 21.

LARGE-SIGNAL PULSE RESPONSE

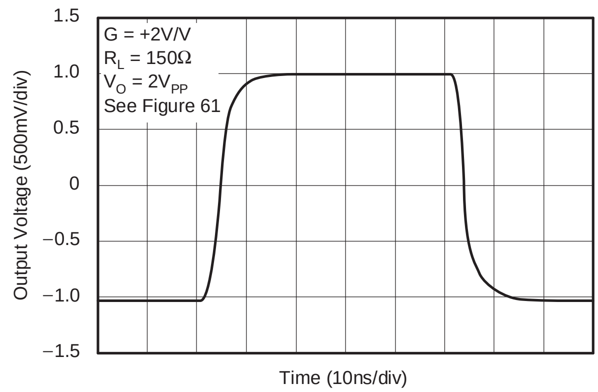


Figure 22.

REQUIRED R_S vs CAPACITIVE LOAD

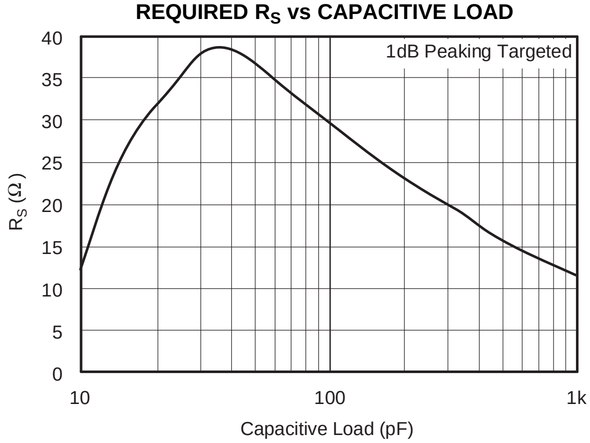


Figure 23.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

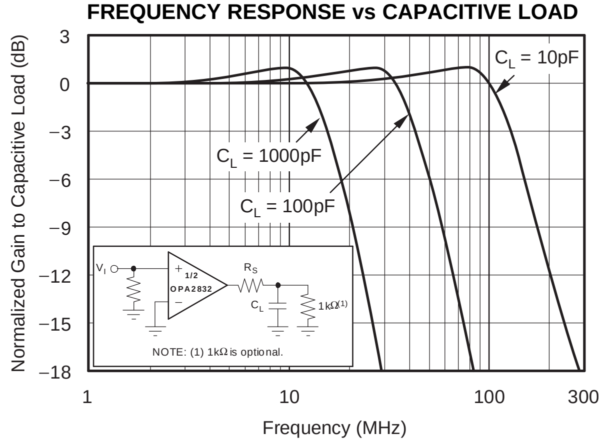


Figure 24.

TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_{CM} = 2V, unless otherwise noted (see Figure 61).

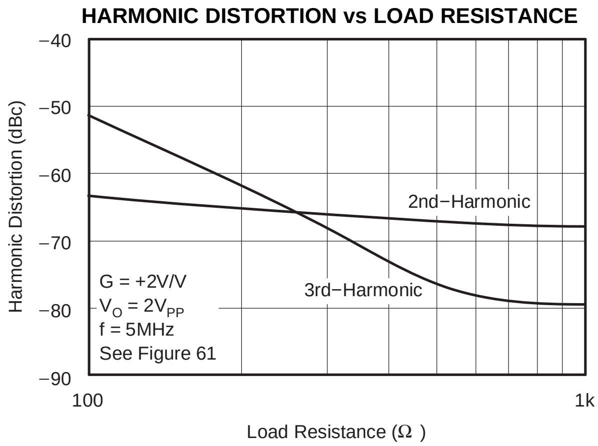


Figure 25.

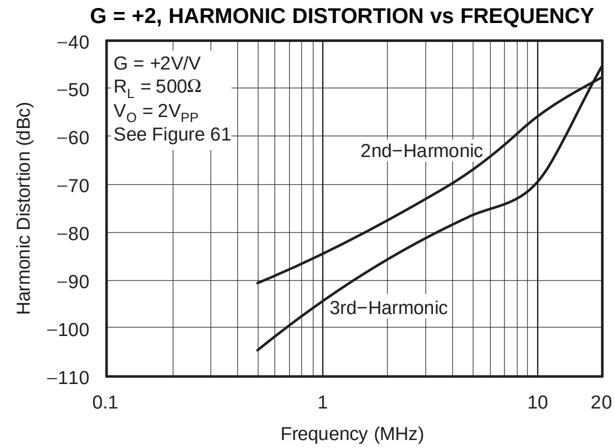


Figure 26.

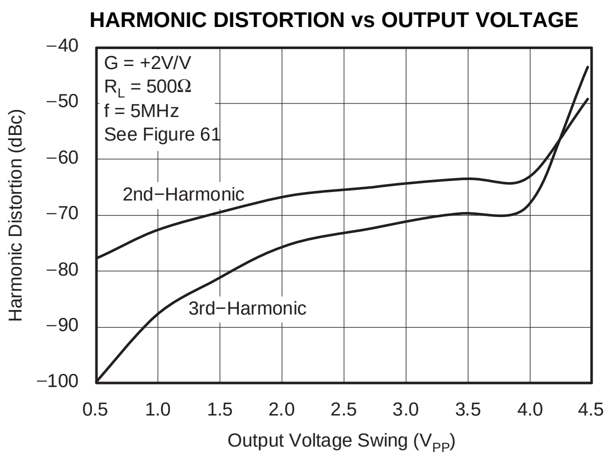


Figure 27.

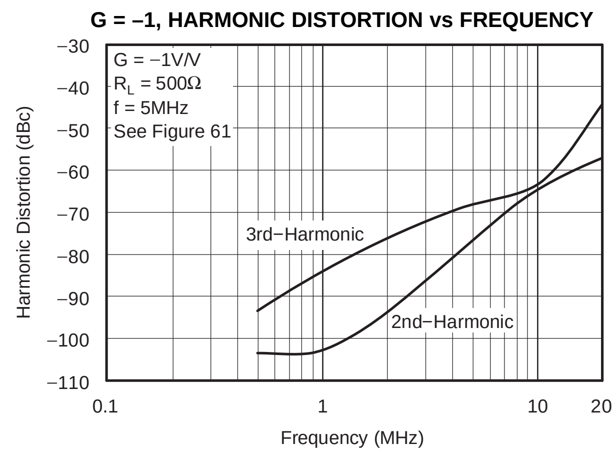


Figure 28.

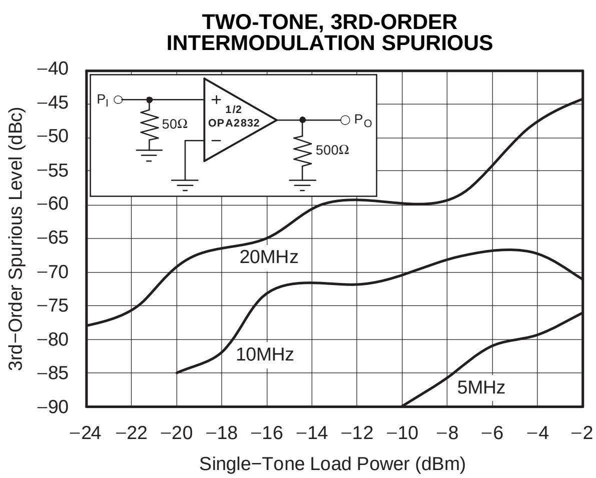


Figure 29.

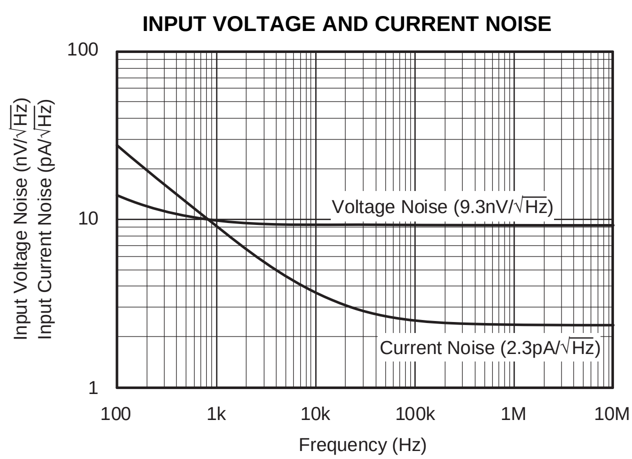


Figure 30.

TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_{CM} = 2V, unless otherwise noted (see Figure 61).

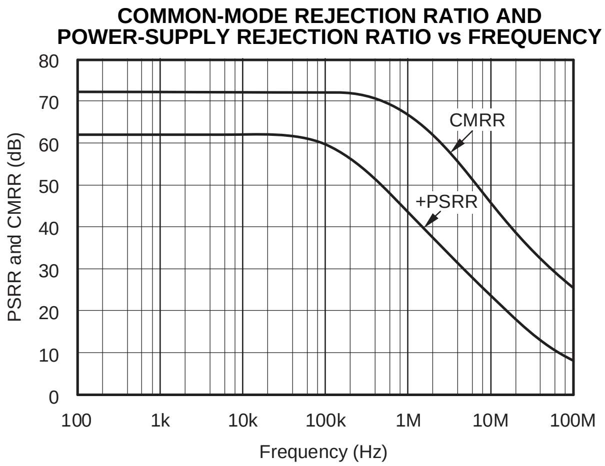


Figure 31.

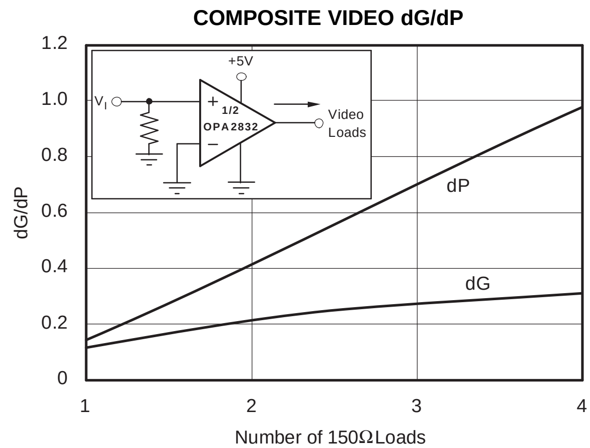


Figure 32.

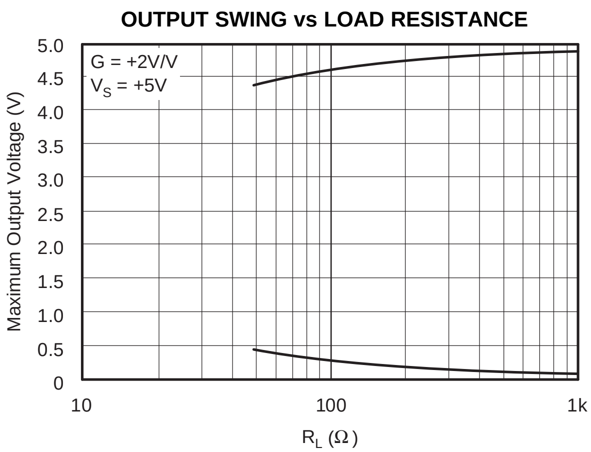


Figure 33.

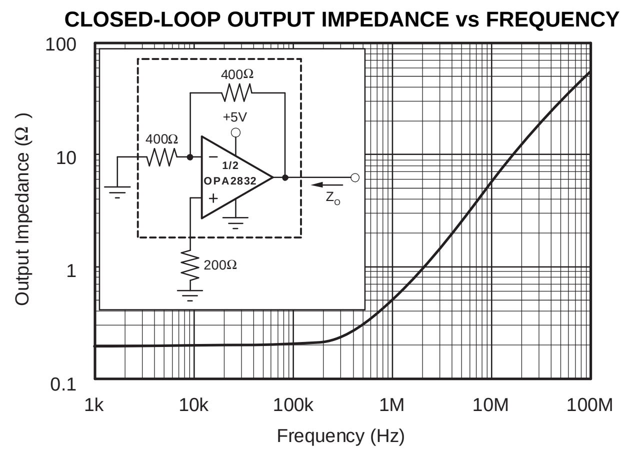


Figure 34.

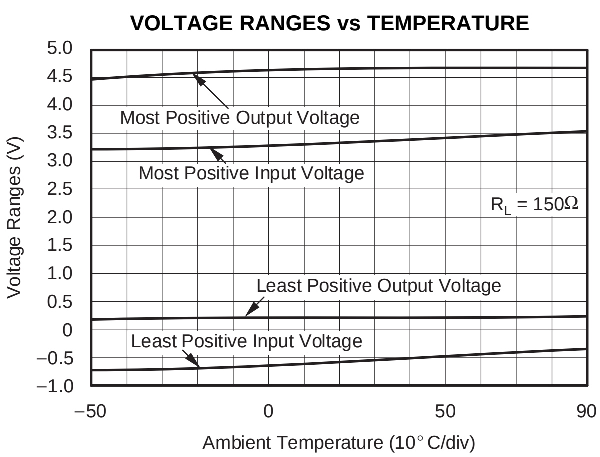


Figure 35.

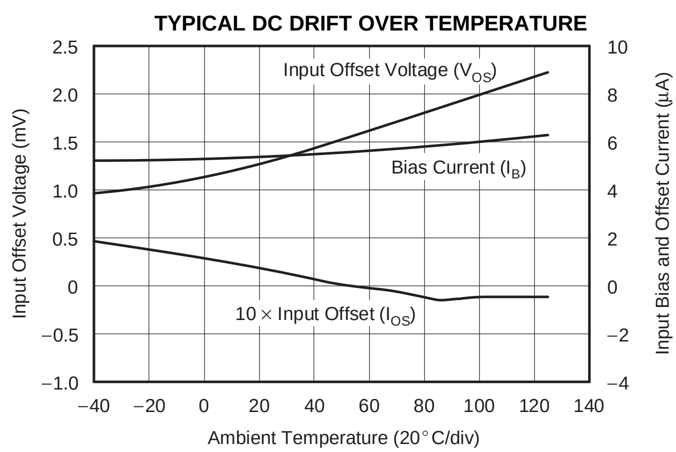


Figure 36.

TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_{CM} = 2V, unless otherwise noted (see Figure 61).

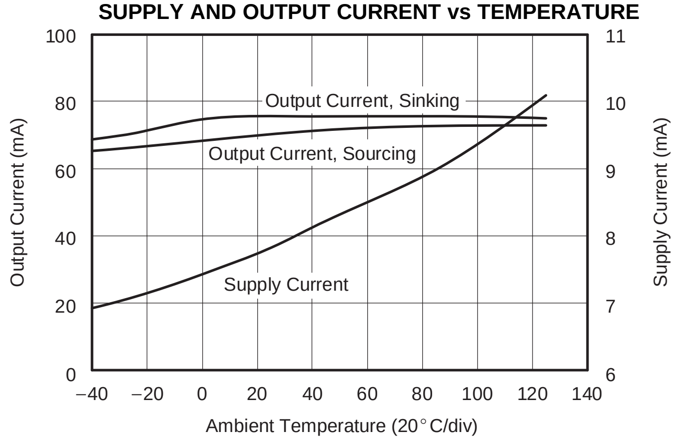


Figure 37.

TYPICAL CHARACTERISTICS: V_S = +5V (Differential)

At T_A = +25°C, Differential Gain = +2V/V, and R_L = 500Ω, unless otherwise noted.

DIFFERENTIAL PERFORMANCE TEST CIRCUIT

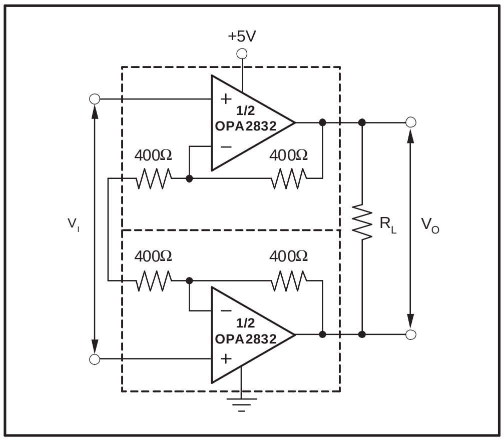


Figure 38.

SMALL-SIGNAL FREQUENCY RESPONSE

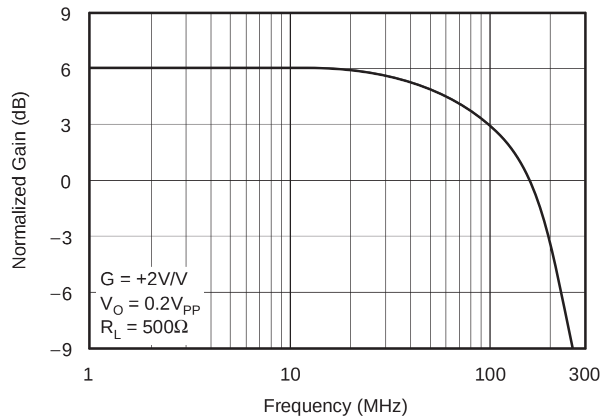


Figure 39.

LARGE-SIGNAL FREQUENCY RESPONSE

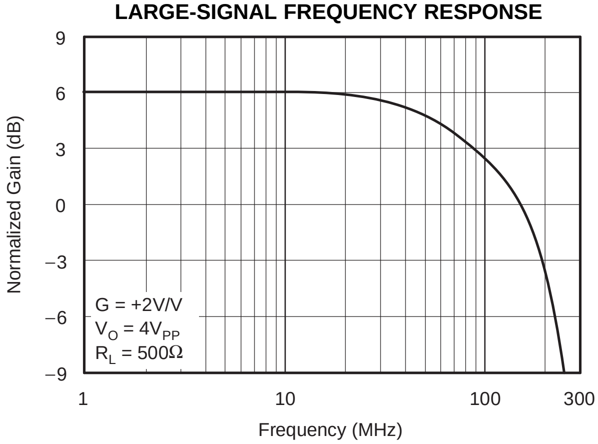


Figure 40.

HARMONIC DISTORTION vs FREQUENCY

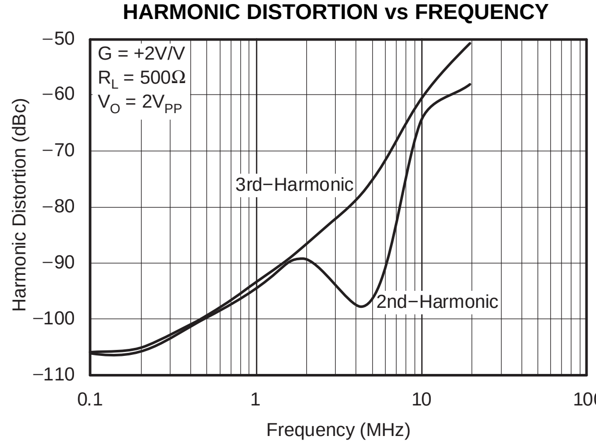


Figure 41.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

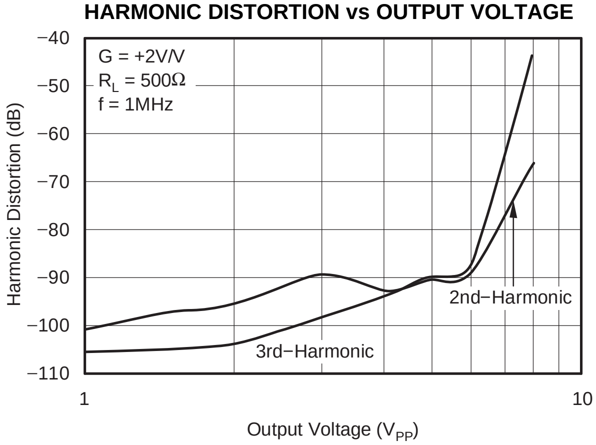


Figure 42.

HARMONIC DISTORTION vs LOAD RESISTANCE

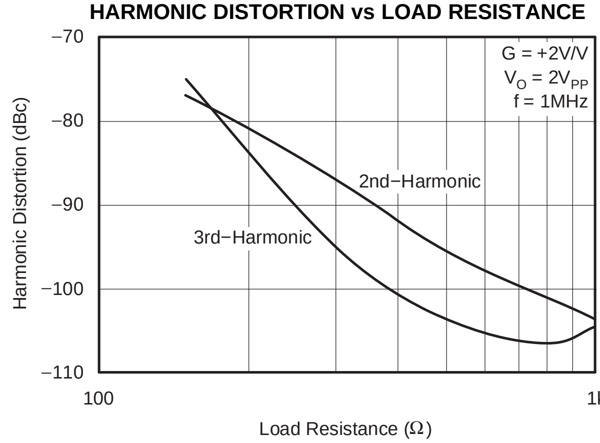


Figure 43.

TYPICAL CHARACTERISTICS: V_S = +3.3V

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_{CM} = 0.75V, unless otherwise noted (see Figure 62).

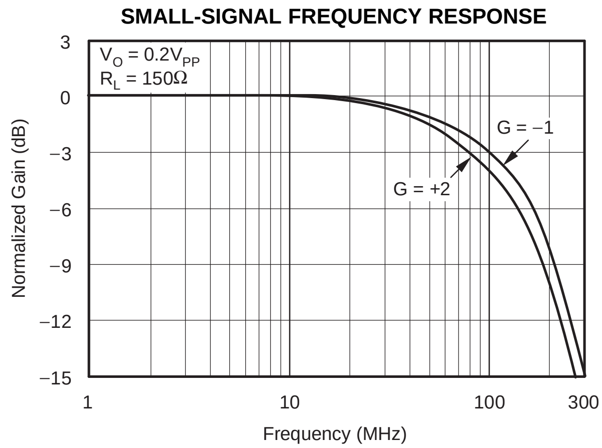


Figure 44.

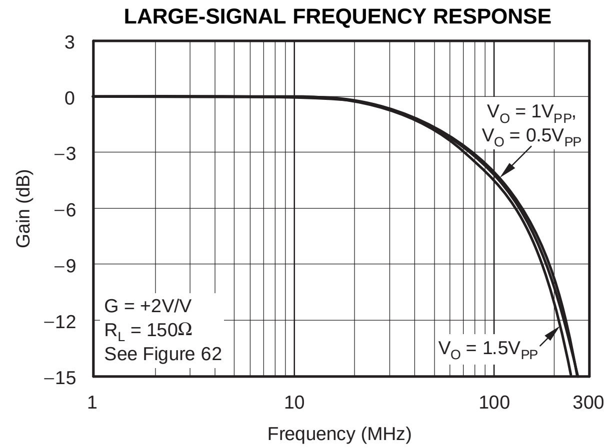


Figure 45.

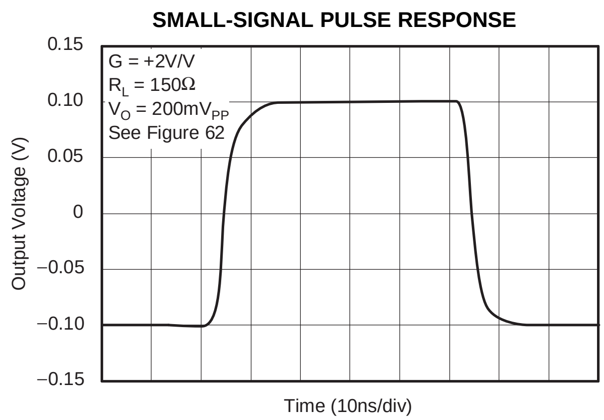


Figure 46.

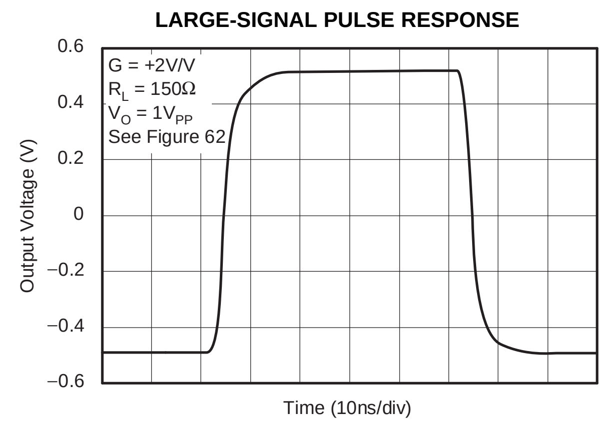


Figure 47.

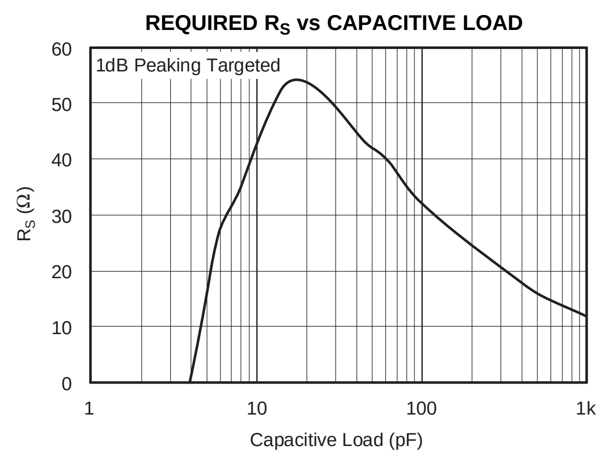


Figure 48.

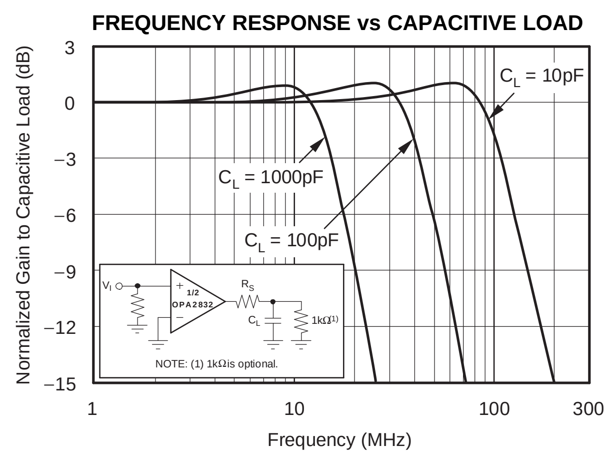


Figure 49.

TYPICAL CHARACTERISTICS: V_S = +3.3V (continued)

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_{CM} = 0.75V, unless otherwise noted (see Figure 62).

HARMONIC DISTORTION vs LOAD RESISTANCE

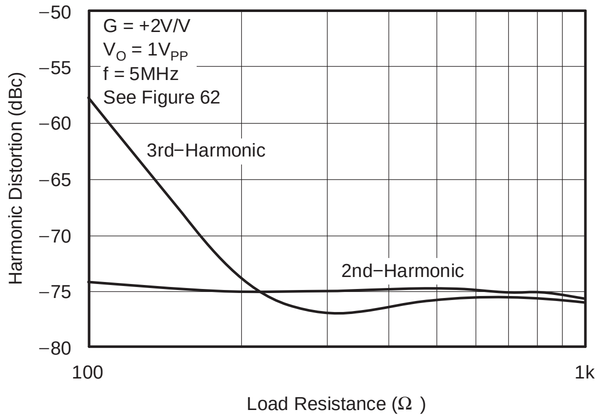


Figure 50.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

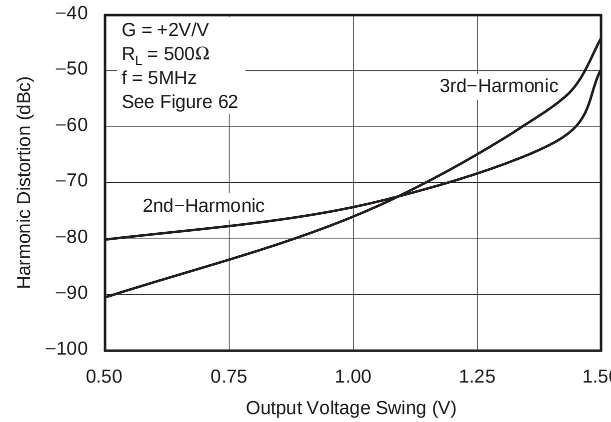


Figure 51.

HARMONIC DISTORTION vs FREQUENCY

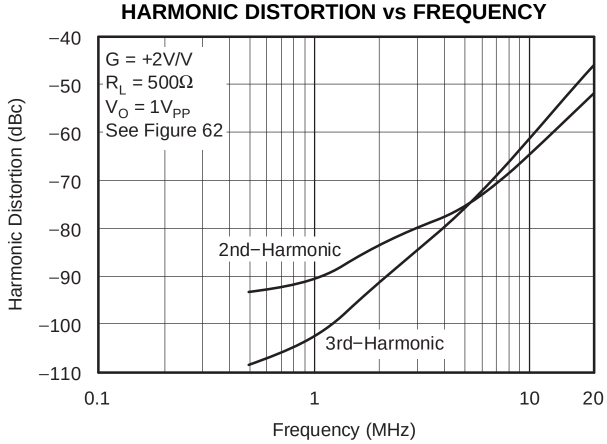


Figure 52.

TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS

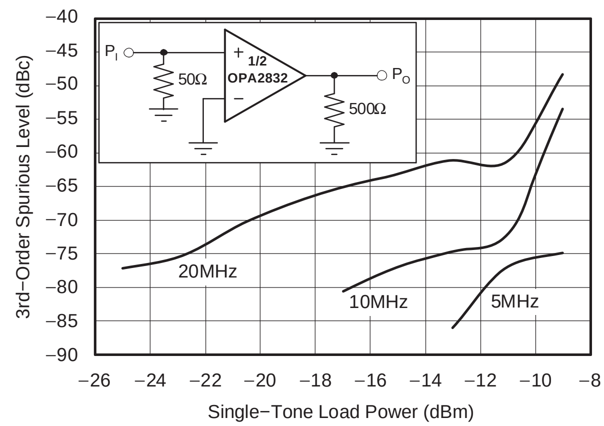


Figure 53.

OUTPUT SWING vs LOAD RESISTANCE

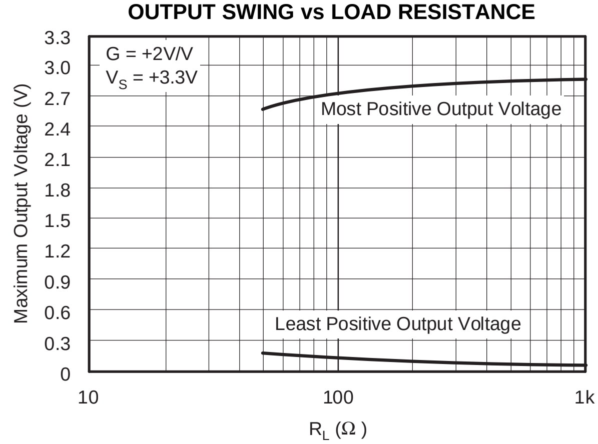


Figure 54.

TYPICAL CHARACTERISTICS: V_S = +3.3V (Differential)

At T_A = +25°C, Differential Gain = +2V/V, and R_L = 500Ω, unless otherwise noted.

DIFFERENTIAL PERFORMANCE TEST CIRCUIT

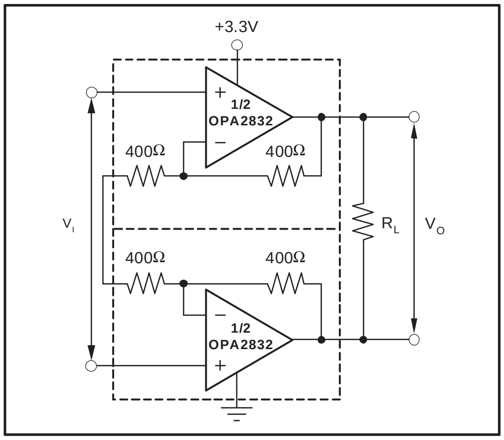


Figure 55.

SMALL-SIGNAL FREQUENCY RESPONSE

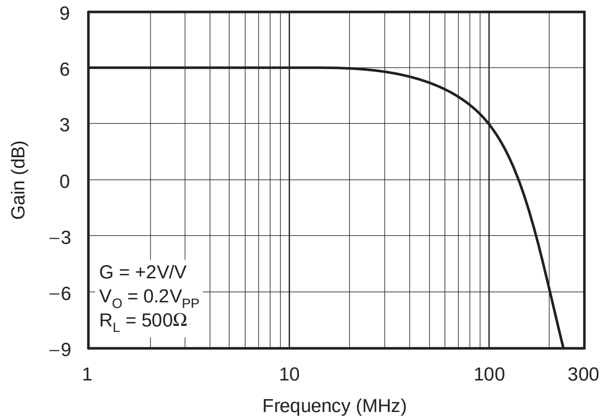


Figure 56.

LARGE-SIGNAL FREQUENCY RESPONSE

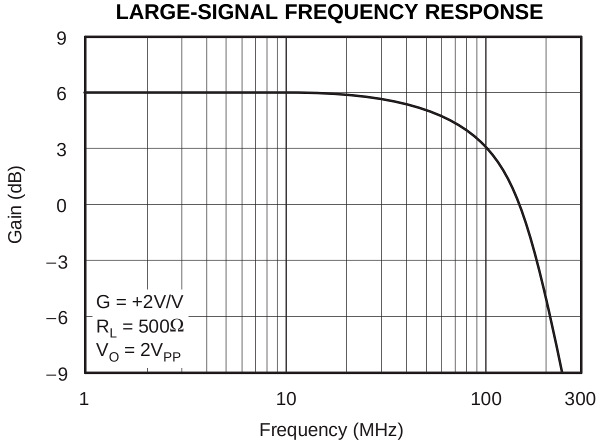


Figure 57.

HARMONIC DISTORTION vs FREQUENCY

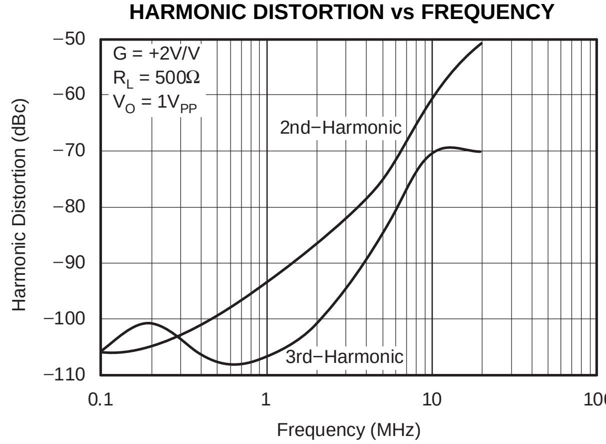


Figure 58.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

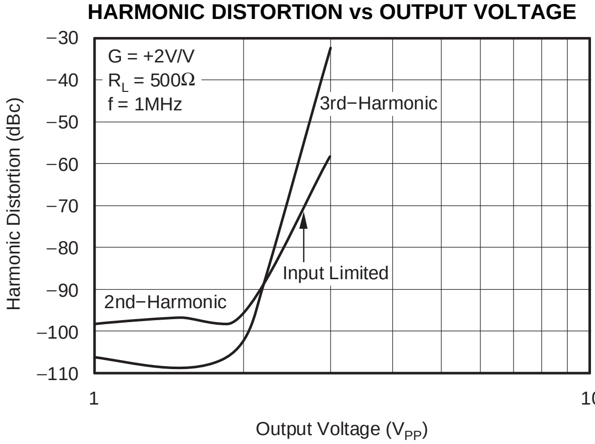


Figure 59.

HARMONIC DISTORTION vs LOAD RESISTANCE

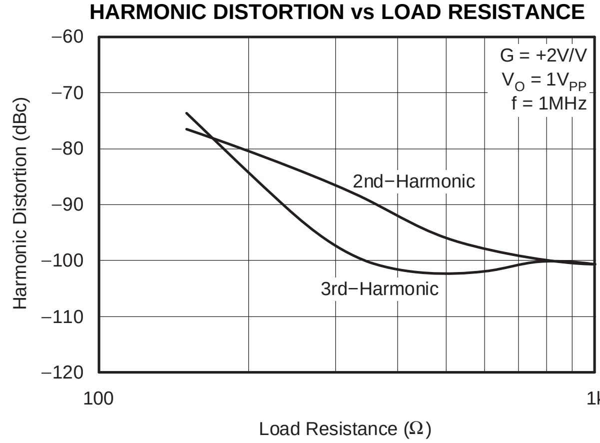


Figure 60.

APPLICATIONS INFORMATION

WIDEBAND VOLTAGE-FEEDBACK OPERATION

The OPA2832 is a unity-gain stable, very high-speed voltage-feedback op amp designed for single-supply operation (+3V to +11V). The input stage supports input voltages below ground and to within 1.7V of the positive supply. The complementary common-emitter output stage provides an output swing to within 25mV of ground and the positive supply. The OPA2832 is compensated to provide stable operation with a wide range of resistive loads.

Figure 61 shows the AC-coupled, gain of +2 configuration used for the +5V Specifications and Typical Characteristic Curves. For test purposes, the input impedance is set to 50Ω with the 66.7Ω resistor to ground in parallel with the 200Ω bias network. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins. For the circuit of Figure 61, the total effective load on the output at high frequencies is 150Ω || 800Ω. The 332Ω and 505Ω resistors at the noninverting input provide the common-mode bias voltage. Their parallel combination equals the DC resistance at the inverting input R_F), reducing the DC output offset due to input bias current.

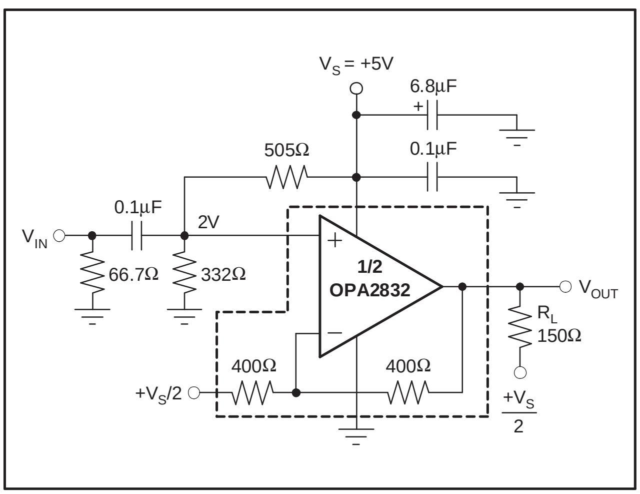


Figure 61. AC-Coupled, G = +2, +5V Single-Supply Specification and Test Circuit

Figure 62 shows the AC-coupled, gain of +2 configuration used for the +3.3V Specifications and Typical Characteristic Curves. For test purposes, the input impedance is set to 66.5Ω with a resistor to ground. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins. For the circuit of Figure 62, the total effective load on the output at high frequencies is 150Ω || 800Ω. The 255Ω and 1.13kΩ resistors at the noninverting input provide the common-mode bias voltage. Their parallel combination equals the DC resistance at the inverting input R_F), reducing the DC output offset due to input bias current.

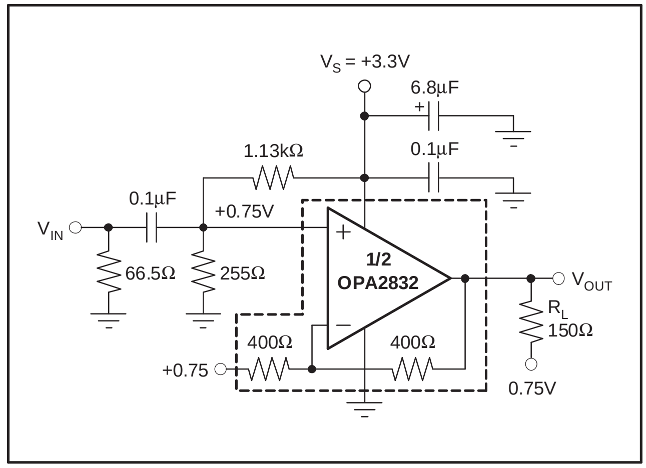


Figure 62. AC-Coupled, G = +2, +3V Single-Supply Specification and Test Circuit

Figure 63 shows the DC-coupled, gain of +2, dual power-supply circuit configuration used as the basis of the ±5V Electrical Characteristics and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 150Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins. For the circuit of Figure 63, the total effective load will be 150Ω || 800Ω. Two optional components are included in Figure 63. An additional resistor (175Ω) is included in series with the noninverting input. Combined with the 25Ω DC source resistance looking back towards the signal generator, this gives an input bias current cancelling resistance that matches the 200Ω source resistance seen at the inverting input (see the *DC Accuracy and Offset Control* section). In addition to the usual power-supply decoupling capacitors to ground, a 0.01µF capacitor is included between the two power-supply pins. In practical PC board layouts, this optional capacitor will typically improve the 2nd-harmonic distortion performance by 3dB to 6dB.

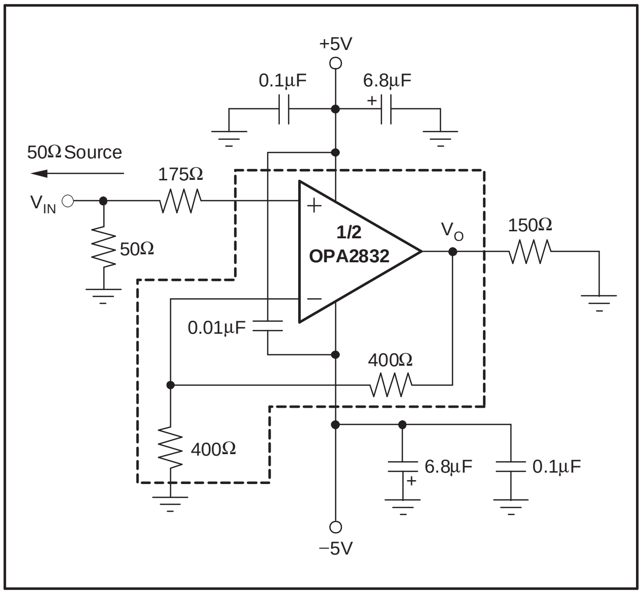


Figure 63. DC-Coupled, G = +2, Bipolar Supply Specification and Test Circuit

SINGLE-SUPPLY ADC INTERFACE

The ADC interface in Figure 64 shows a DC-coupled, single-supply ADC driver circuit. Many systems are now requiring +3.3V supply capability of both the ADC and its driver. The OPA2832 provides excellent performance in this demanding application. Its large input and output voltage ranges and low distortion support converters such as the ADS5203. The input level-shifting circuitry was designed so that V_{IN} can be between 0V and 0.5V, while delivering an output voltage of 1V to 2V for the ADS5203.

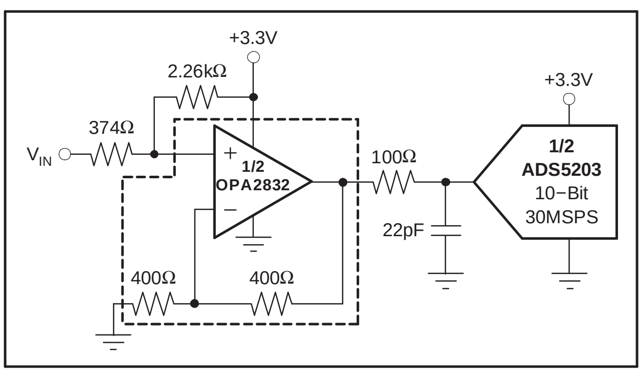


Figure 64. DC-Coupled, +3V ADC Driver

SINGLE-SUPPLY ACTIVE FILTER

The OPA2832, while operating on a single +3.3V or +5V supply, lends itself well to high-frequency active filter designs. Again, the key additional requirement is to establish the DC operating point of the signal near the supply midpoint for highest dynamic range. Figure 66 shows an example design of a 1MHz low-pass Butterworth filter using the Sallen-Key topology.

Both the input signal and the gain setting resistor are AC-coupled using 0.1μF blocking capacitors (actually giving bandpass response with the low-frequency pole set to 3.2kHz for the component values shown). As discussed for Figure 61, this allows the midpoint bias formed by one 2kΩ and one 3kΩ resistor to appear at both the input and output pins. The midband signal gain is set to +2 (6dB) in this case. The capacitor to ground on the noninverting input is intentionally set larger to dominate input parasitic terms. At a gain of +2, the OPA2832 on a single supply will show 75MHz small- and large-signal bandwidth. The resistor values have been slightly adjusted to account for this limited bandwidth in the amplifier stage. Tests of this circuit, shown in Figure 65, illustrate a precise 1MHz, –3dB point with a maximally-flat passband (above the 3.2kHz AC-coupling corner), and a maximum stop band attenuation of 36dB.

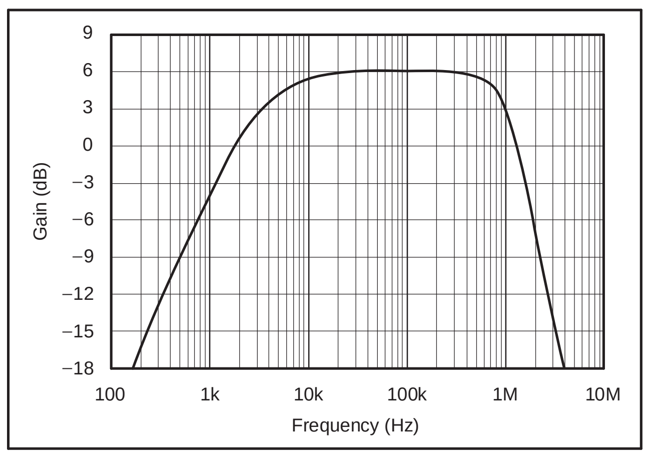


Figure 65. 1MHz, 2nd-Order, Butterworth Low-Pass Filter

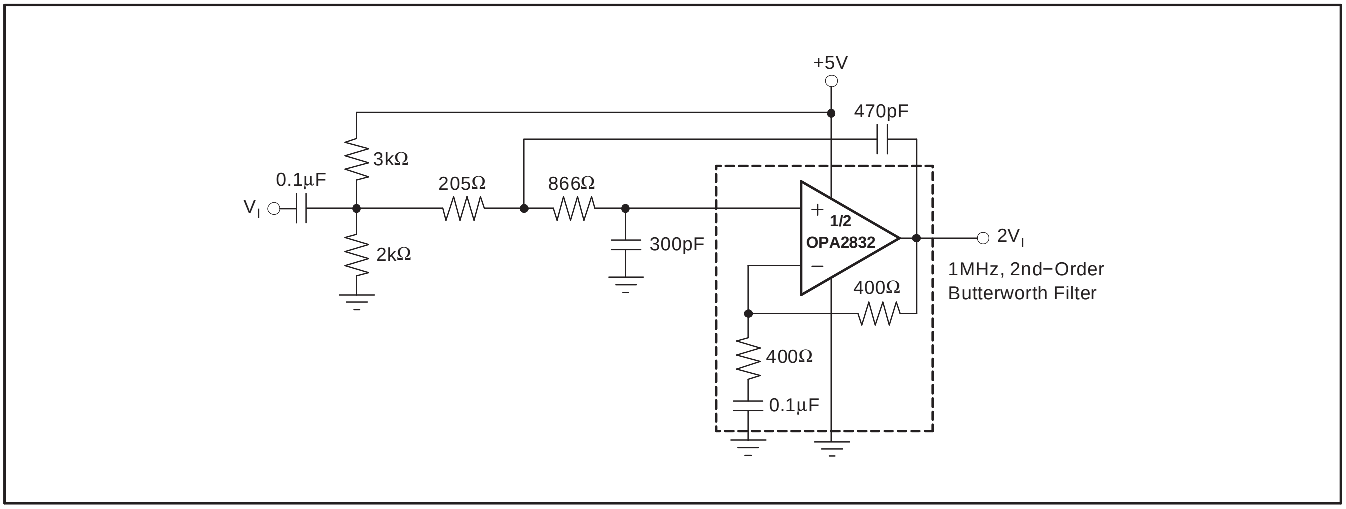


Figure 66. Single-Supply, High-Frequency Active Filter

DIFFERENTIAL LOW-PASS FILTERS

The dual OPA2832 offers an easy means to implement low-power differential active filters. On a single supply, one way to implement a 2nd-order, low-pass filter is shown in Figure 67. This circuit provides a net differential gain of 1 with a precise 5MHz Butterworth response. The signal is AC-coupled (giving a high-pass pole at low frequencies) with the DC operating point for the circuit set by the unity-gain buffer—the BUF602. This buffer gives a very low output impedance to high frequencies to maintain accurate filter characteristics. If the source is a DC-coupled signal already biased into the operating range of the OPA2832 input CMR, these capacitors and the midpoint bias may be removed. To get the desired 5MHz cutoff, the input resistors to the filter is actually 119Ω. This is implemented in Figure 67 as the parallel combination of the two 238Ω resistors on each half of the differential input as part of the DC biasing network. If the BUF602 is removed, these resistors should be collapsed back to a single 119Ω input resistor.

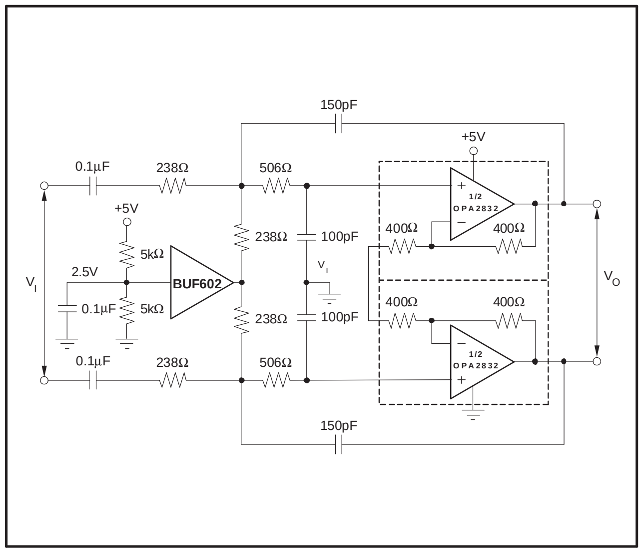


Figure 67. Single-Supply, 5MHz, 2nd-Order, Low-Pass Sallen-Key Filter

Implementing the DC bias in this way also attenuates the differential signal by half. This is recovered by setting the amplifier gain at 2V/V to get a net unity-gain filter characteristic from input to output. The filter design shown here has also adjusted the resistor values slightly from an ideal analysis to account for the 100MHz bandwidth in the amplifier stages. The filter capacitors at the noninverting inputs are shown as two separate capacitors to ground. While it is certainly correct to collapse these two capacitors into a single capacitor across the two inputs (which would be 50pF for this circuit) to get the same differential filtering characteristic, tests have shown two separate capacitors to a low impedance point act to attenuate the common-mode feedback present in this circuit giving more stable operation in actual implementation. Figure 68 shows the frequency response for the filter of Figure 67.

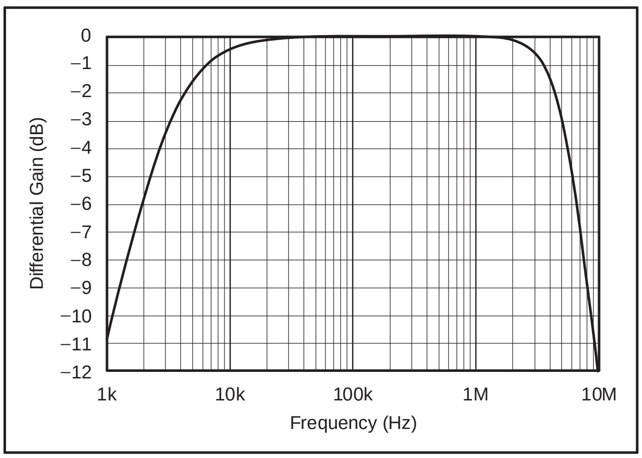


Figure 68. 5MHz, 2nd-Order, Butterworth Low-Pass Filter

HIGH-PASS FILTERS

Another approach to mid-supply biasing is shown in Figure 69. This method uses a bypassed divider network in place of the buffer used in Figure 67. The impedance is set by the parallel combination of the resistors forming the divider network, but as frequency increases it looks more and more like a short due to the capacitor. Generally, the capacitor value needs to be two to three orders of magnitude greater than the filter capacitors shown for the circuit to work properly.

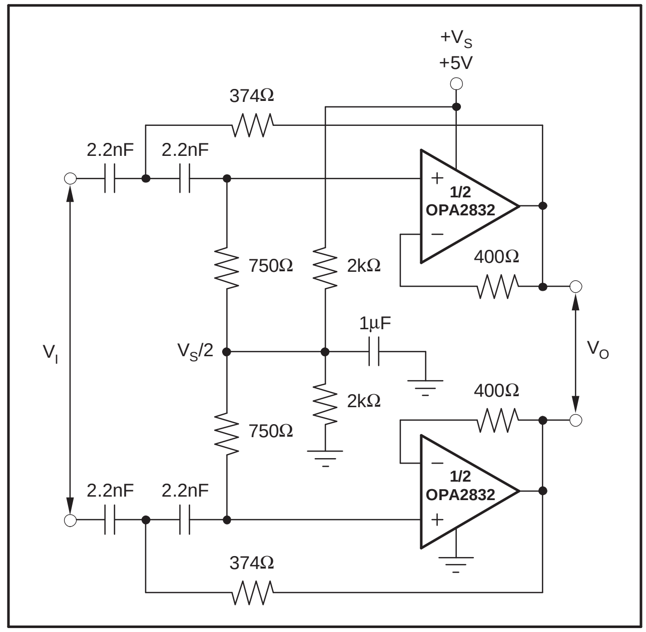


Figure 69. 138kHz, 2nd-Order, High-Pass Filter

Results showing the frequency response for the circuit of Figure 69 is shown in Figure 70.

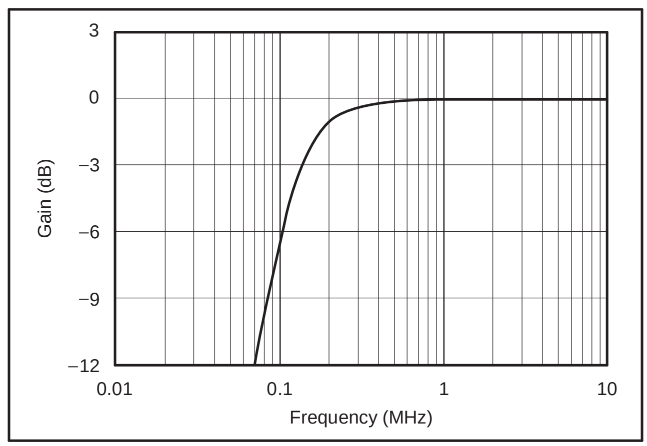


Figure 70. Frequency Response for the Filter of Figure 69

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA2832 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 1.

Table 1. Demonstration Fixtures by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA2832ID	SO-8	DEM-OPA-SO-2A	SBOU003
OPA2832IDGK	MSOP-8	DEM-OPA-MSOP-2A	SBOU004

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA2832 product folder.

MACROMODEL AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often a quick way to analyze the performance of the OPA2832 and its circuit designs. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role on circuit performance. A SPICE model for the OPA2832 is available through the TI web page (www.ti.com). The applications department is also available for design assistance. These models predict typical small signal AC, transient steps, DC performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of the data sheet. These models do not attempt to distinguish between the package types in their small-signal AC performance.

OPERATING SUGGESTIONS

OUTPUT CURRENT AND VOLTAGES

The OPA2832 provides outstanding output voltage capability. For the +5V supply, under no-load conditions at +25°C, the output voltage typically swings closer than 90mV to either supply rail.

The minimum specified output voltage and current specifications over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the ensured tables. As the output transistors deliver power, their junction temperatures will increase, decreasing their V_{BE}s (increasing the available output voltage swing) and increasing their current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications, since the output stage junction temperatures will be higher than the minimum specified operating ambient.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This will not normally be a problem, since most applications include a series matching resistor at the output that will limit the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power-supply pin (8-pin packages) will, in most cases, destroy the amplifier. If additional short-circuit protection is required, consider a small series resistor in the power-supply leads. This will reduce the available output voltage swing under heavy output loads.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance which may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA2832 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load.

The Typical Characteristic curves show the recommended R_S versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA2832. Long PC board traces, unmatched cables, and connections to multiple devices can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the output pin (see the *Board Layout Guidelines* section).

The criterion for setting this R_S resistor is a maximum bandwidth, flat frequency response at the load. For a gain of +2, the frequency response at the output pin is already slightly peaked without the capacitive load, requiring relatively high values of R_S to flatten the response at the load. Increasing the noise gain will also reduce the peaking (see Figure 24).

DISTORTION PERFORMANCE

The OPA2832 provides good distortion performance into a 150Ω load. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operating on a single +3.3V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic will dominate the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the noninverting configuration (see Figure 62) this is sum of R_F + R_G, while in the inverting configuration, only R_F needs to be included in parallel with the actual load. Running differential suppresses the 2nd-harmonic, as shown in the differential typical characteristic curves.

NOISE PERFORMANCE

High slew rate, unity-gain stable, voltage-feedback op amps usually achieve their slew rate at the expense of a higher input noise voltage. The 9.2nV/√Hz input voltage noise for the OPA2832, however, is much lower than comparable amplifiers. The input-referred voltage noise and the two input-referred current noise terms (2.8pA/√Hz) combine to give low output noise under a wide variety of operating conditions. Figure 71 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

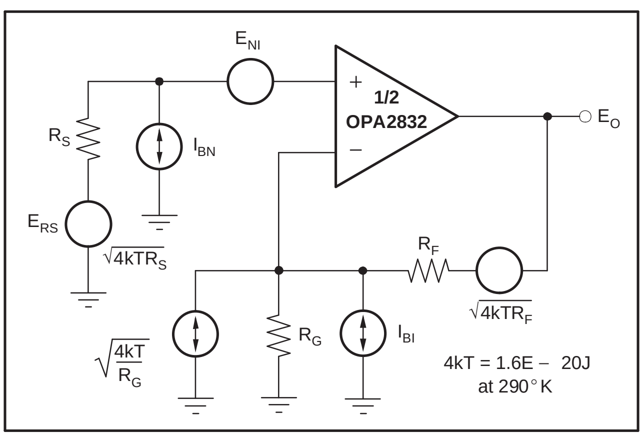


Figure 71. Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 1 shows the general form for the output noise voltage using the terms shown in Figure 71:

$$E_O = \sqrt{\left(E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right)NG^2 + (I_{BI}R_F)^2 + 4kTR_FNG} \quad (1)$$

Dividing this expression by the noise gain (NG = (1 + R_F/R_G)) will give the equivalent input-referred spot noise voltage at the noninverting input, as shown in Figure 71:

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (2)$$

Evaluating these two equations for the circuit and component values shown in Figure 61 will give a total output spot noise voltage of 19.3nV/√Hz and a total equivalent input spot noise voltage of 9.65nV/√Hz. This is including the noise added by the resistors. This total input-referred spot noise voltage is not much higher than the 9.2nV/√Hz specification for the op amp voltage noise alone.

DC ACCURACY AND OFFSET CONTROL

The balanced input stage of a wideband voltage-feedback op amp allows good output DC accuracy in a wide variety of applications. The power-supply current trim for the OPA2832 gives even tighter control than comparable products. Although the high-speed input stage does require relatively high input bias current (typically 5µA out of each input terminal), the close matching between them may be used to reduce the output DC error caused by this current. This is done by matching the DC source resistances appearing at the two inputs. Evaluating the configuration of Figure 63 (which has matched DC input resistances), using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to:

- (NG = noninverting signal gain at DC)
- ±(NG × $V_{OS(MAX)}$) + R_F × $I_{OS(MAX)}$)
- = ±(2 × 7.5mV) + (400Ω × 1.5µA)
- = –14.4mV to +15.6mV

A fine-scale output offset null, or DC operating point adjustment, is often required. Numerous techniques are available for introducing DC offset control into an op amp circuit. Most of these techniques are based on adding a DC current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input may be considered. Bring the DC offsetting current into the inverting input node through resistor values that are much larger than the signal path resistors. This will insure that the adjustment circuit has minimal effect on the loop gain and hence the frequency response.

THERMAL ANALYSIS

Maximum desired junction temperature will set the maximum allowed internal power dissipation, as described below. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load; though, for resistive loads connected to mid-supply ($V_S/2$), P_{DL} is at a maximum when the output is fixed at a voltage equal to $V_S/4$ or $3V_S/4$. Under this condition, $P_{DL} = V_S^2/(16 \times R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage, and not into the load, that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA2832 (MSOP-8 package) in the circuit of Figure 63 operating at the maximum specified ambient temperature of +85°C and driving both channels at a 150Ω load at mid-supply.

$$P_D = 10V \times 11.9mA + \frac{2 \times 5^2}{\left(16 \times \left(150\Omega \parallel 800\Omega\right)\right)} = 144mV$$

$$\text{Maximum } T_J = +85^oC + \left(0.144W \times 150^oC/W\right) = 107^oC$$

Although this is still well below the specified maximum junction temperature, system reliability considerations may require lower ensured junction temperatures. The highest possible internal dissipation will occur if the load requires current to be forced into the output at high output voltages or sourced from the output at low output voltages. This puts a high current through a large internal voltage drop in the output transistors.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA2832 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1μF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Each power-supply connection should always be decoupled with one of these capacitors. An optional supply decoupling capacitor (0.1μF) across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high-frequency performance. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PCB traces as short as possible. Never use wire-wound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the typical characteristic curve *Recommended R_S vs Capacitive Load*. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA2832 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary onboard, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA2832 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the typical characteristic curve *Recommended R_S vs Capacitive Load*. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2832 onto the board.

INPUT AND ESD PROTECTION

The OPA2832 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 72.

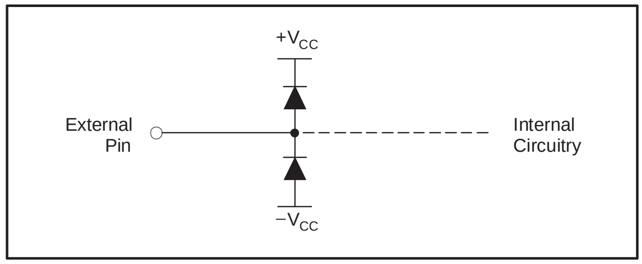


Figure 72. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (that is, in systems with ±15V supply parts driving into the OPA2832), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible, since high values degrade both noise performance and frequency response.

Revision History

Changes from Revision B (May 2006) to Revision C	Page
• Changed rating for storage voltage range in Absolute Maximum Ratings table from –40°C to +125°C to –65°C to +125°C	2

Changes from Revision A (April 2005) to Revision B	Page
• Changed Demonstration Boards title to Demonstration Fixtures.	24
• Changed OPA830 changed to OPA2832 of first paragraph of Demonstration Fixtures section.	24
• Changed Table 1 title and columns 3 and 4.	24

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2832ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2832
OPA2832ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2832
OPA2832IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A61
OPA2832IDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A61
OPA2832IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2832
OPA2832IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2832

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

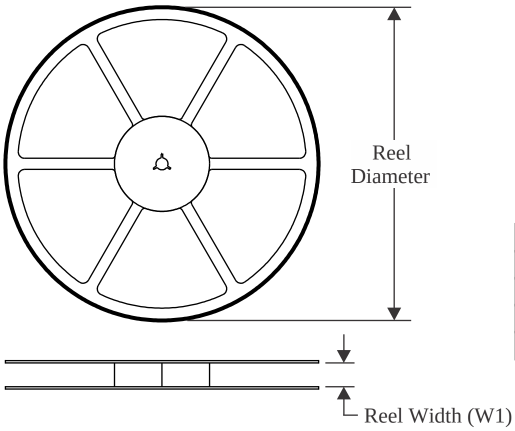
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

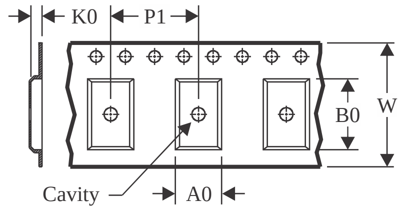
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

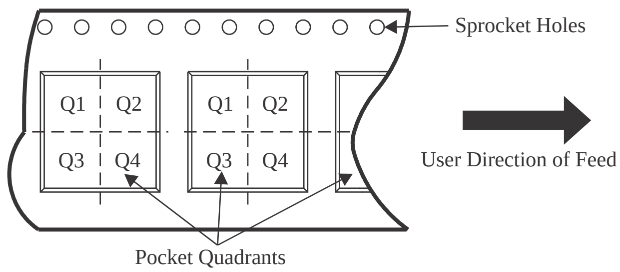


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

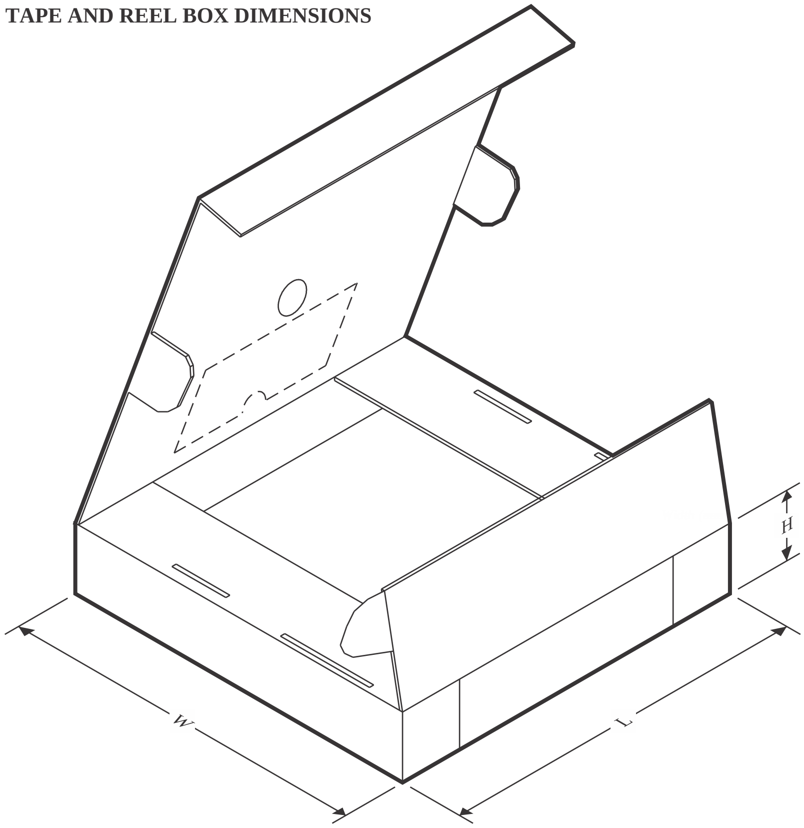
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2832IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

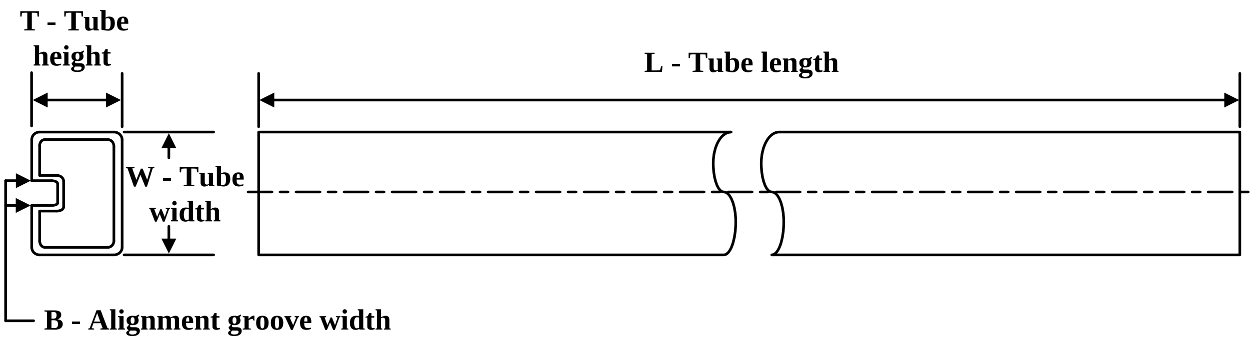
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

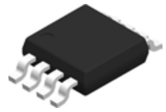
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2832IDR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE

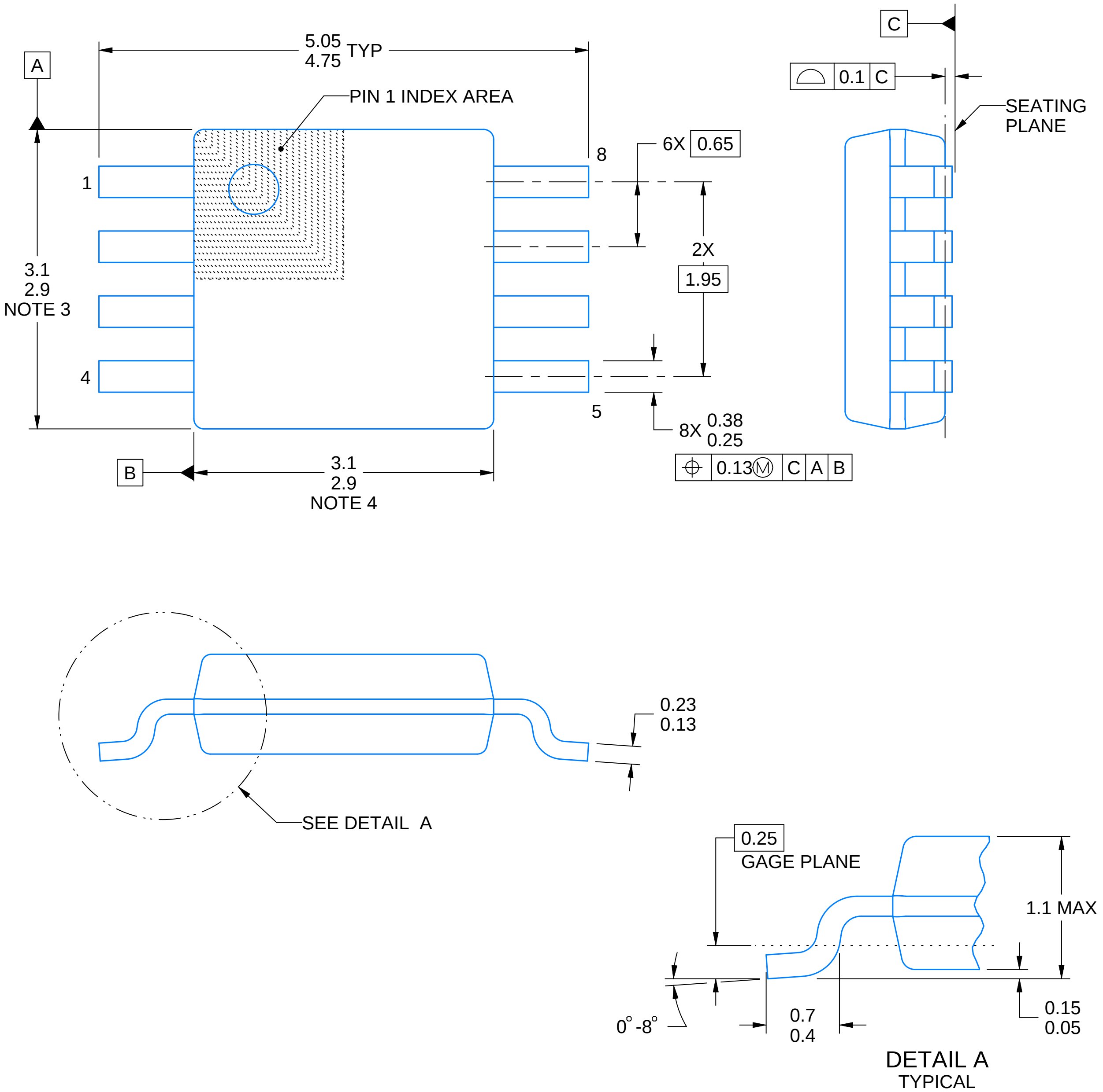


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2832ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2832ID.A	D	SOIC	8	75	506.6	8	3940	4.32



SMALL OUTLINE PACKAGE

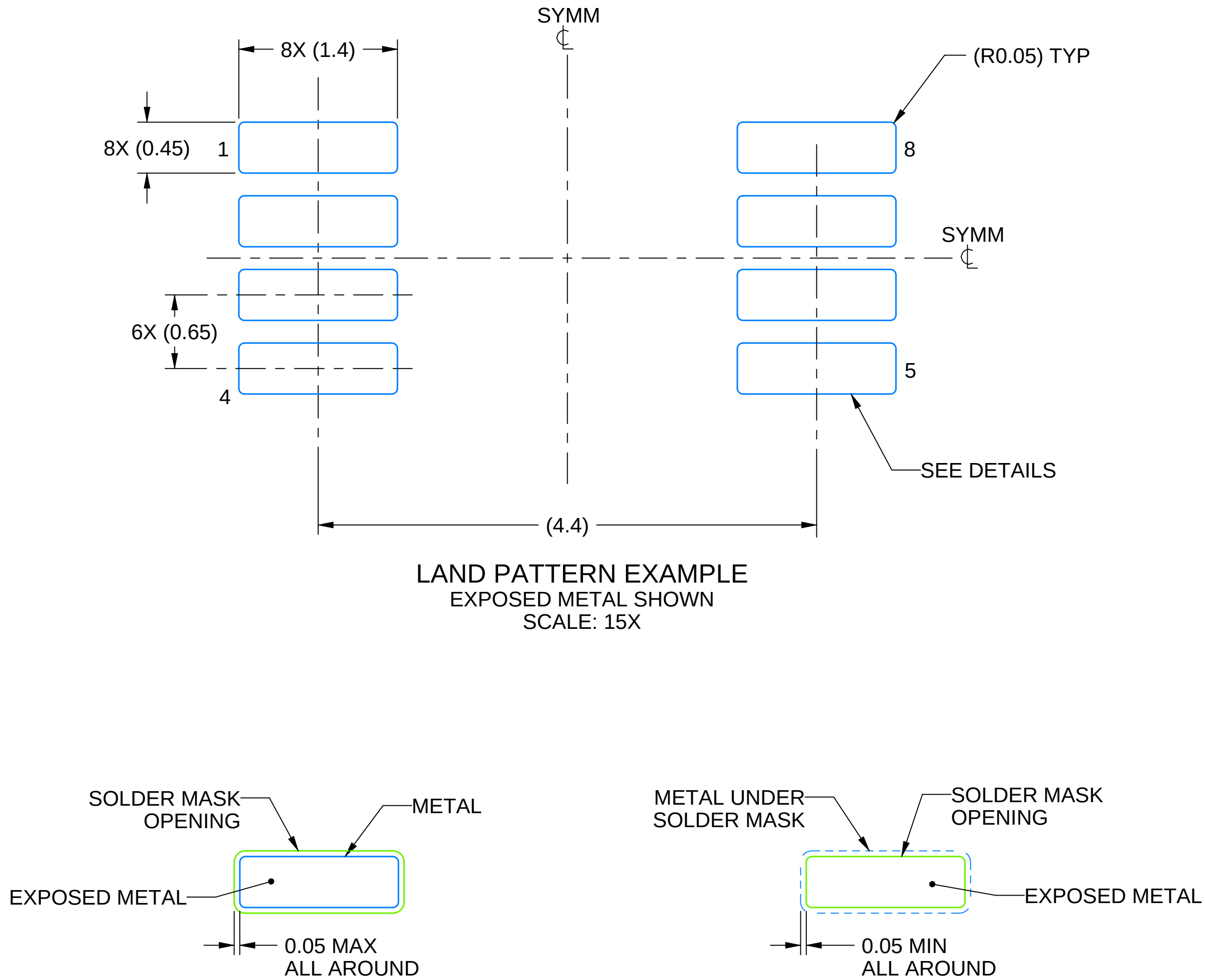


4214862/A 04/2023

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

NON-SOLDER MASK DEFINED (PREFERRED)

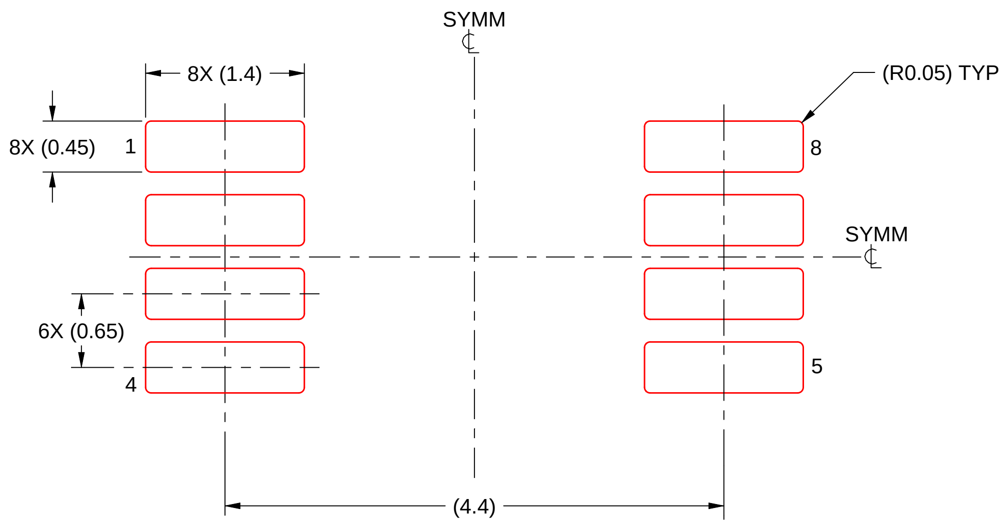
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

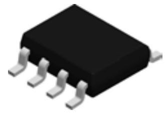


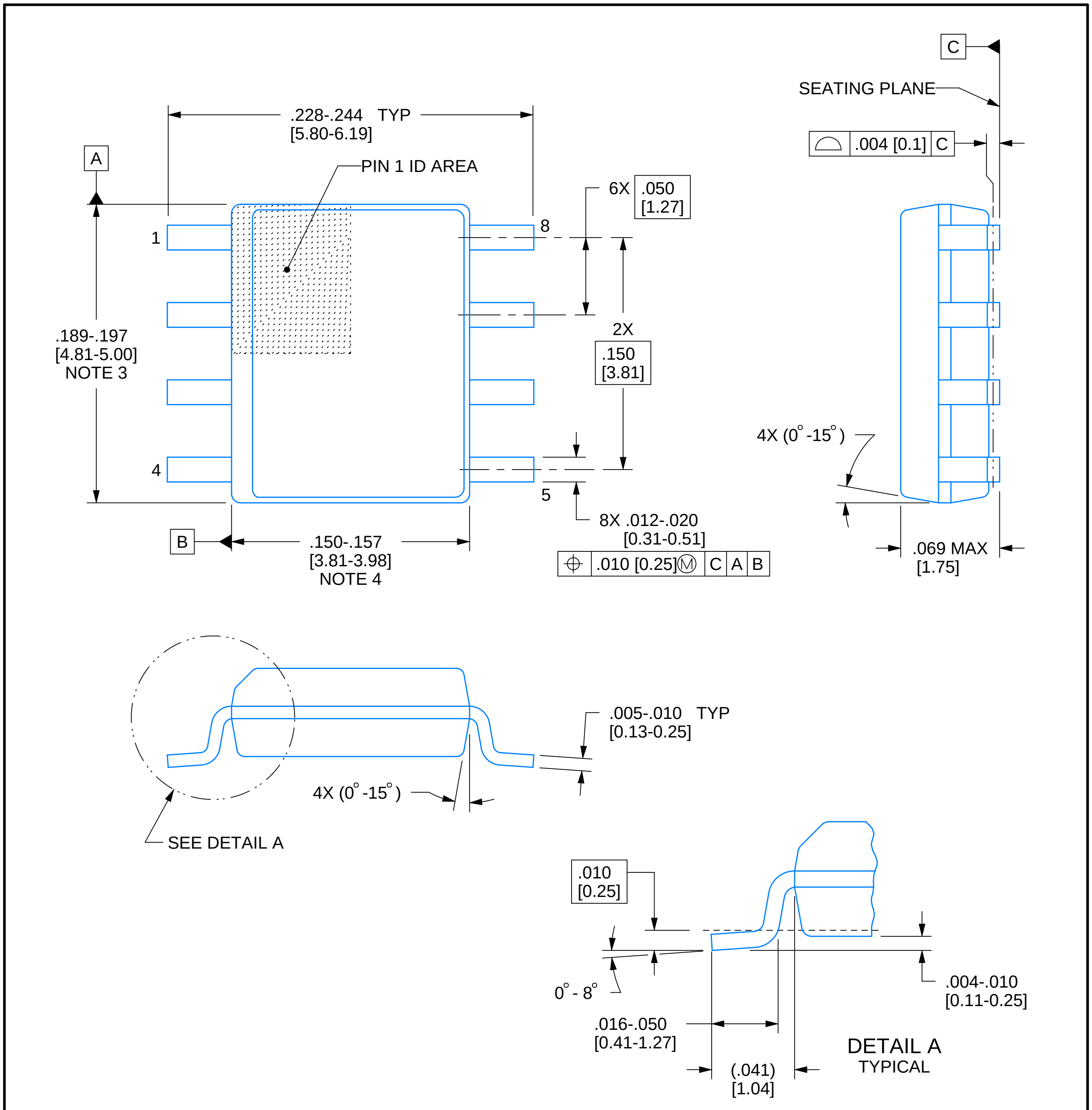
SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

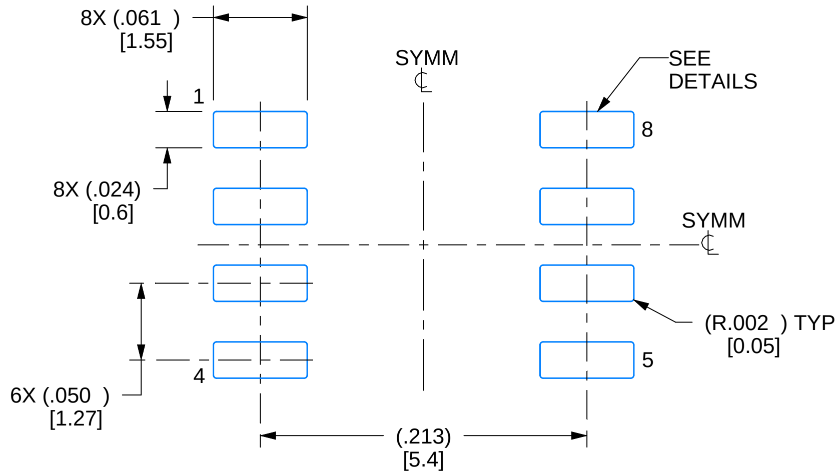




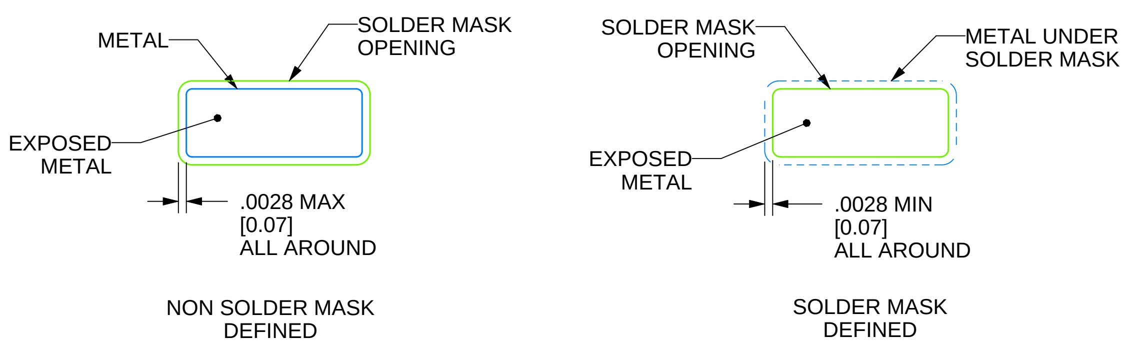
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

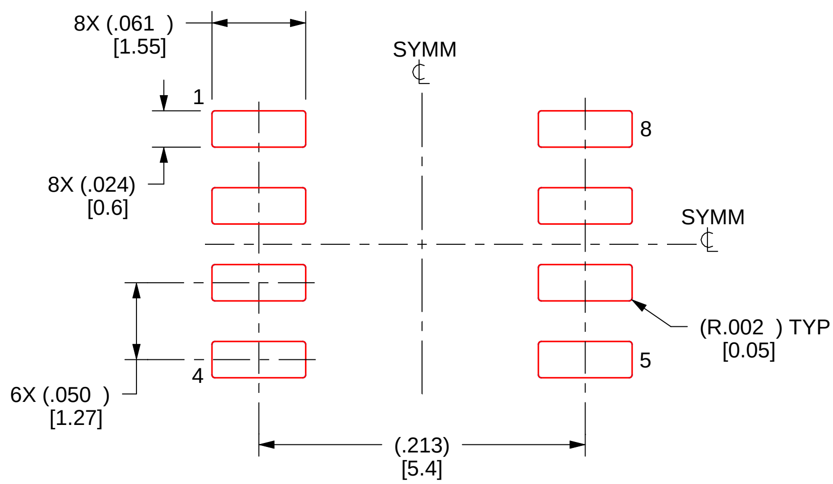


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.