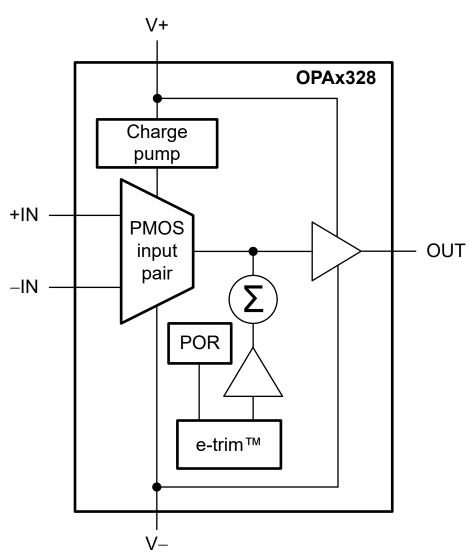
OPAx328 Precision, 40MHz, 1pA, Low-Noise, RRIO, CMOS Operational Amplifiers With Shutdown

1 Features

- Precision with zero-crossover distortion:
  - Low offset voltage: 50µV (maximum)
  - High CMRR: 120dB
  - Rail-to-rail I/O
- Wide bandwidth: 40MHz
- Low input bias current: 1pA (maximum)
- Low noise: 6.1nV/√Hz at 10kHz
- Slew rate: 30V/µs
- Fast 0.01% settling time: 180ns
- Single-supply voltage range: 2.2V to 5.5V
- Unity-gain stable

2 Applications

- Optical module
- Position sensor
- Multiparameter patient monitor
- CT and PET scanner
- Chemistry and gas analyzer
- Bidirectional 400-V and 800-V to LV
- Merchant network and server PSU
- String inverter
- Solar power optimizer



Block Diagram

3 Description

The single-channel OPA328 and dual-channel OPA2328 (OPAx328) are a new generation family of precision, low-voltage CMOS operational amplifiers optimized for very low noise and wide bandwidth.

The OPAx328 have a linear input stage with zero-crossover distortion that delivers excellent common-mode rejection ratio (CMRR) of 120dB (typical) over the full input range. The input common-mode voltage range extends 100mV beyond the negative and positive supply rails. The output voltage typically swings within 10mV of the rails.

The OPAx328 also use Texas Instrument's proprietary e-trim™ operational amplifier technology, enabling a unique combination of ultra-low offset and low input offset drift without the need for any input switching or auto-zero techniques.

Low-noise (6.1nV/√Hz) and high-speed operation (40MHz, 30V/µs) make these devices a great choice for driving sampling analog-to-digital converters (ADCs).

The OPAx328 are also a great choice for high-impedance-input, single-supply applications. Low input bias current and low input capacitance allows for high-frequency transimpedance gains at low photocurrent operation (< 1nA).

Device Information

PART NUMBER	CHANNELS / SHUTDOWN	PACKAGE[(1)]
OPA328	Single / No	DBV (SOT-23, 5)
OPA328S[(2)]	Single / Yes	DBV (SOT-23, 6)
OPA2328	Dual / No	D (SOIC, 8)
		DGK (VSSOP, 8)
		DRG (WSON, 8)
		YBJ (DSBGA, 24)
OPA4328[(2)]	Quad / No	PW (TSSOP, 14)
	Quad / Yes	RUM (WQFN, 16)

(1) For more information, see Section 10.
(2) Preview information (not Production Data).

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4 Pin Configuration and Functions

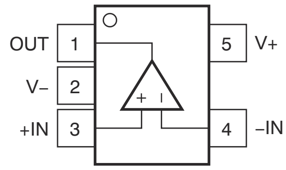


Figure 4-1. OPA328 DBV Package, 5-Pin SOT-23 (Top View)

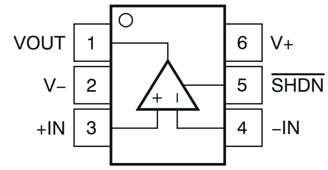


Figure 4-2. OPA328S DBV Package (Preview) 6-Pin SOT-23 (Top View)

Pin Functions: OPA328 and OPA328S

PIN			TYPE	DESCRIPTION
NAME	OPA328	OPA328S		
–IN	4	4	Input	Negative (inverting) input
+IN	3	3	Input	Positive (noninverting) input
OUT, VOUT	1	1	Output	Output
$\overline{\text{SHDN}}$	—	5	Input	Shutdown, active low
V–	2	2	Power	Negative (lowest) power supply
V+	5	6	Power	Positive (highest) power supply

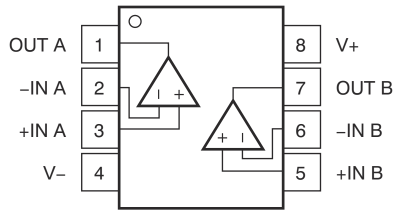


Figure 4-3. OPA2328 D Package, 8-pin SOIC and DGK Package, 8-Pin VSSOP (Top View)

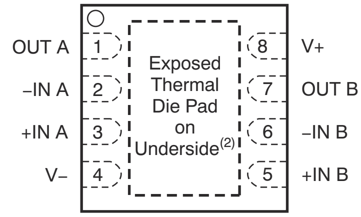


Figure 4-4. OPA2328 DRG Package, 8-Pin WSON (Top View)

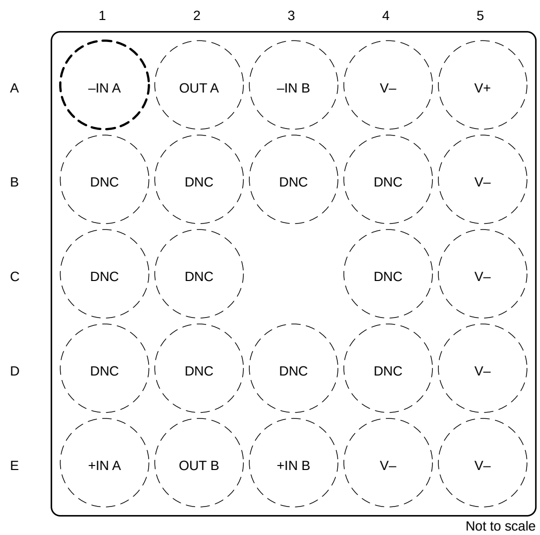


Figure 4-5. OPA2328 YBJ Package, 24-Pin DSBGA (Top View)

Pin Functions: OPA2328

PIN			TYPE	DESCRIPTION
NAME	D (SOIC), DGK (VSSOP), DRG (WSON)	YBJ (DSBGA)		
–IN A	2	A1	Input	Inverting input, channel A
+IN A	3	E1	Input	Noninverting input, channel A
–IN B	6	A3	Input	Inverting input, channel B
+IN B	5	E3	Input	Noninverting input, channel B
OUT A	1	A2	Output	Output, channel A
OUT B	7	E2	Output	Output, channel B
V–	4	A4, B5, C5, D5, E4, E5	Power	Negative (lowest) power supply
V+	8	A5	Power	Positive (highest) power supply
DNC	—	B1, B2, B3, B4, C1, C2, C4, D1, D2, D3, D4	—	Do not connect

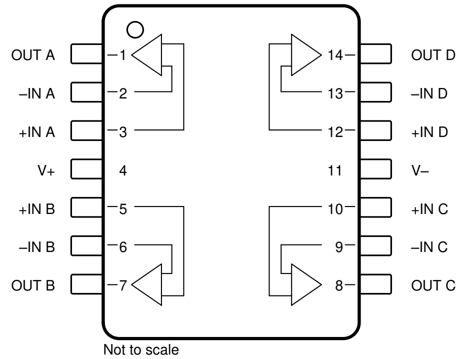


Figure 4-6. OPA4328 PW Package (Preview), 14-Pin TSSOP (Top View)

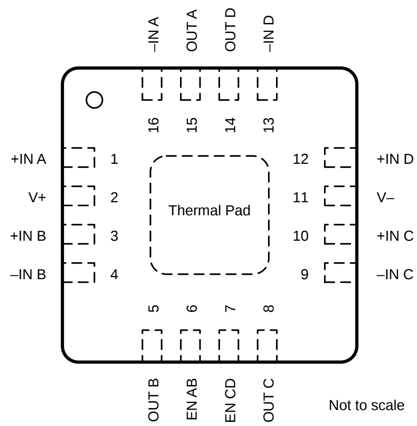


Figure 4-7. OPA4328 RUM Package (Preview), 16-Pin WQFN (Top View)

Table 4-1. Pin Functions: OPA4328

PIN			TYPE	DESCRIPTION
NAME	NO.			
	PW (TSSOP)	RUM (WQFN)		
EN AB	—	6	Input	Enable pin for A and B amplifiers. High = amplifiers A and B are enabled.
EN CD	—	7	Input	Enable pin for C and D amplifiers. High = amplifiers C and D are enabled.
–IN A	2	16	Input	Inverting input, channel A
+IN A	3	1	Input	Noninverting input, channel A
–IN B	6	4	Input	Inverting input, channel B
+IN B	5	3	Input	Noninverting input, channel B
–IN C	9	9	Input	Inverting input, channel C
+IN C	10	10	Input	Noninverting input, channel C
–IN D	13	13	Input	Inverting input, channel D
+IN D	12	12	Input	Noninverting input, channel D
OUT A	1	15	Output	Output, channel A
OUT B	7	5	Output	Output, channel B
OUT C	8	8	Output	Output, channel C
OUT D	14	14	Output	Output, channel D
Thermal Pad	—	Thermal Pad	Power	Connect thermal pad to V–
V–	11	11	Power	Negative (lowest) power supply
V+	4	2	Power	Positive (highest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	–0.3	6	V
	Input voltage, all pins	(V–) – 0.3	(V+) + 0.3	V
	Input current (INA+, INA–, INB+, INB–, INSA/B, OUTSA/B/1/2/3)	–10	10	mA
	Output short-circuit[2]	Continuous	Continuous	
T_A	Operating temperature	–55	150	°C
T_J	Junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single-supply	2.2		5.5	V
		Dual-supply	±1.1		±2.75	V
T_A	Specified temperature		–40		125	°C

5.4 Thermal Information - OPA328

THERMAL METRIC[1]		OPA328	UNIT
		DBV (SOT-23)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	163.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	97.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	40.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Thermal Information - OPA2328

THERMAL METRIC[1]		OPA2328	OPA2328	OPA2328	OPA2328	UNIT
		D (SOIC)	DGK (VSSOP)	DRG (WSON)	YBJ (DSBGA)	
		8 PINS	8 PINS	8 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	123.9	165	50.3	66.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.1	53	50.2	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.4	87	23.4	15.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	15.7	4.9	0.8	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	66.6	85	23.4	15.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	7.3	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.6 Electrical Characteristics

at T_A = 25°C, V_S = ±1.1 V to ±2.75 V (V_S = 2.2 V to 5.5 V), R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_{OUT} = V_S / 2, and min and max specification established from manufacturing final test (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	OPA2328D, DGK, and DRG		±3	±50	µV
		OPA328DBV		±3	±75	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C, OPA328DBV, OPA2328D, DGK		±0.15	±1	µV/°C
		T_A = –40°C to +125°C, OPA2328DRG		±0.15	±1.5	
PSRR	Power-supply rejection ratio	V_S = ±1.1 V to ±2.75 V		±1	±10	µV/V
		V_S = ±1.1 V to ±2.75 V, T_A = –40°C to +125°C		±15	±40	
	Channel separation (dual, quad)	f = dc		140		dB
		f = 100 kHz		75		
INPUT BIAS CURRENT						
I_B	Input bias current			±0.2	±1	pA
		T_A = 0°C to 85°C			10	
		T_A = –40°C to +125°C			100	
I_{OS}	Input offset current			±0.2	±1	pA
		T_A = 0°C to 85°C			10	
		T_A = –40°C to +125°C			100	
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		3		$µV_{PP}$
e_N	Input voltage noise density	f = 100 Hz		25		nV/√Hz
		f = 1 kHz		9.8		
		f = 10 kHz		6.1		
i_N	Input current noise	f = 10 kHz		0.125		pA/√Hz
INPUT VOLTAGE						
V_{CM}	Common-mode voltage		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	106	120		dB
		(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V, T_A = –40°C to +125°C	96	110		
INPUT CAPACITANCE						
Z_{ID}	Differential			1 || 4		TΩ || pF
Z_{ICM}	Common-mode			1 || 2		TΩ || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 100 mV < V_O < (V+) – 100 mV	108	132		dB
		(V–) + 100 mV < V_O < (V+) – 100 mV, T_A = –40°C to +125°C	96	130		
		(V–) + 200 mV < V_O < (V+) – 200 mV, R_L = 2 kΩ	106	123		
		(V–) + 200 mV < V_O < (V+) – 200 mV, R_L = 2 kΩ, T_A = –40°C to +125°C	90			
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	Gain = 100		40		MHz
SR	Slew rate	4-V step, gain = +1		30		V/µs
t_S	Settling time	To 0.1%, 1-V step, gain = +1		0.1		µs
		To 0.01%, 1-V step, gain = +1		0.18		
	Overload recovery time	V_{IN} × gain > V_S		0.5		µs
THD+N	Total harmonic distortion + noise	V_O = 1 V_{RMS}, gain = +1, f = 1 kHz		0.0001		%

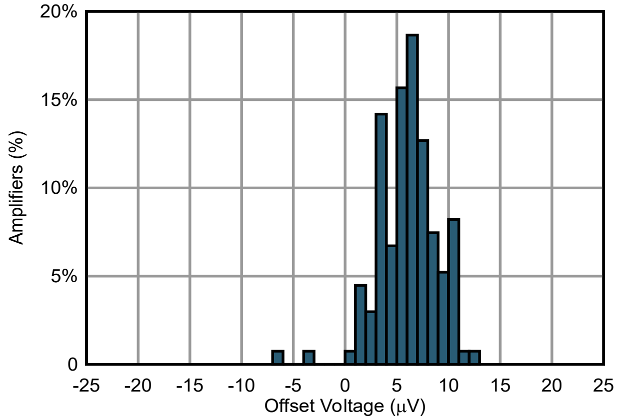
5.6 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±1.1 V to ±2.75 V (V_S = 2.2 V to 5.5 V), R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_{OUT} = V_S / 2, and min and max specification established from manufacturing final test (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing from both rails	V_S = 2.2 V				5	mV
	Voltage output swing from both rails	V_S = 2.2 V	R_L = 2 kΩ			15	mV
	Voltage output swing from both rails	V_S = 5.5 V	OPA328DBV, OPA2328D, DGK			5	mV
	Voltage output swing from both rails	V_S = 5.5 V	OPA2328DRG			10	mV
	Voltage output swing from both rails	V_S = 5.5 V	R_L = 2 kΩ, OPA328DBV, OPA2328D, DGK			15	mV
	Voltage output swing from both rails	V_S = 5.5 V	R_L = 2 kΩ, OPA2328DRG			20	mV
I_{SC}	Short-circuit current	Sinking, V_S = 5.5 V			–65		mA
I_{SC}	Short-circuit current	Sourcing, V_S = 5.5 V			55		mA
C_{LOAD}	Capacitive load drive	Gain = +1			28		pF
R_O	Open-loop output impedance	f = 10 kHz			55		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			3.8	4.5	mA
I_Q	Quiescent current per amplifier	I_O = 0 A, T_A = –40°C to +125°C				5.0	mA
SHUTDOWN (OPA328SDBV and OPA4328RUM)							
I_{QSD}	Quiescent current in shutdown	All amplifiers disabled			30	50	µA
Z_{OFF}	Output impedance in shutdown	All amplifiers disabled			100 || 16		GΩ || pF
V_{IH}	High-level input voltage	Amplifier enabled		(V+) – 0.5			V
V_{IL}	Low-level input voltage	Amplifier disabled				(V–) + 0.5	V
t_{ON}	Output enable time	G = 1, V_{OUT} = 0.9 × V_S/2, all amplifiers enabled			10		µs
t_{OFF}	Output disable time	G = 1, V_{OUT} = 0.1 × V_S/2, all amplifiers disabled			3		µs
	EN pin input leakage current	V_{IH} = V+			0.02		µA
	EN pin input leakage current	V_{IL} = V–			1		µA

5.7 Typical Characteristics

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_{OUT} = mid-supply, C_L = 20 pF, and R_L = 10 kΩ (unless otherwise noted)



V_S = 2.2 V

Figure 5-1. Offset Voltage Production Distribution

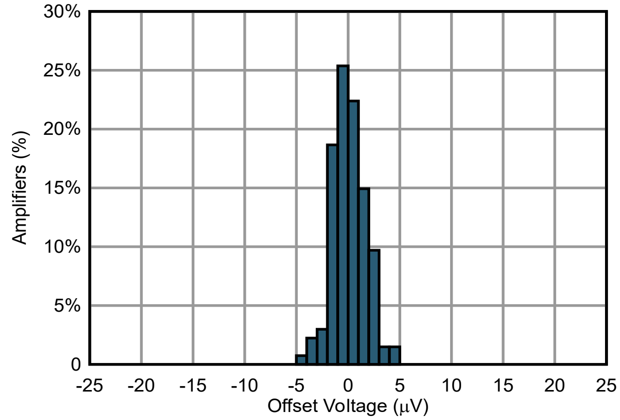
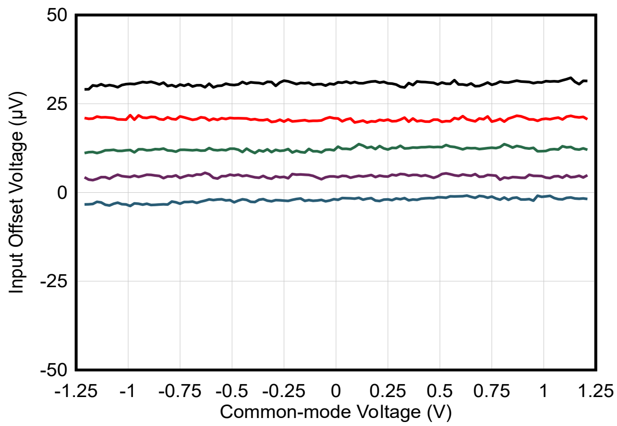


Figure 5-2. Offset Voltage Production Distribution



V_S = 2.2 V

Figure 5-3. Offset Voltage vs Common-Mode Voltage

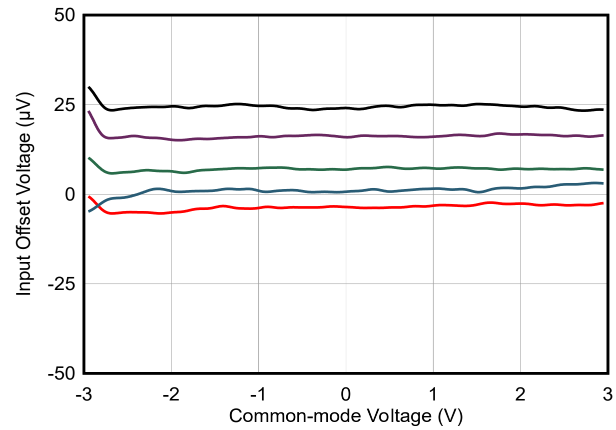


Figure 5-4. Offset Voltage vs Common-Mode Voltage

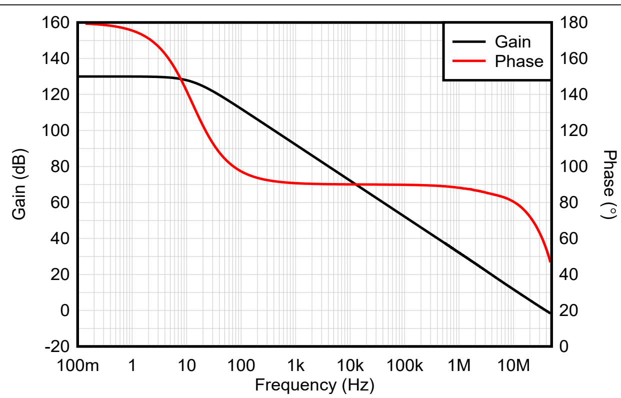


Figure 5-5. Open-Loop Gain and Phase vs Frequency

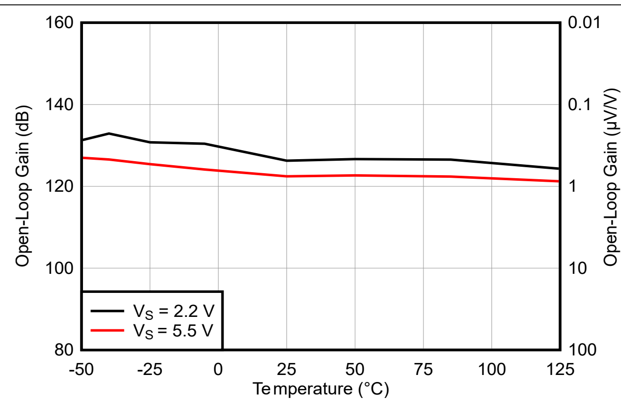


Figure 5-6. Open-Loop Gain vs Temperature

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_{OUT} = mid-supply, C_L = 20 pF, and R_L = 10 kΩ (unless otherwise noted)

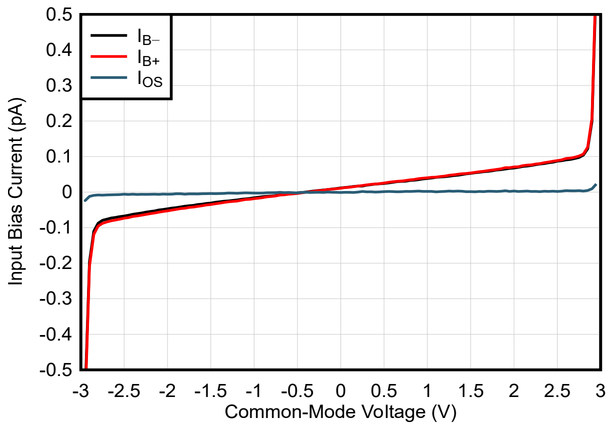


Figure 5-7. Input Bias Current vs Common-Mode Voltage

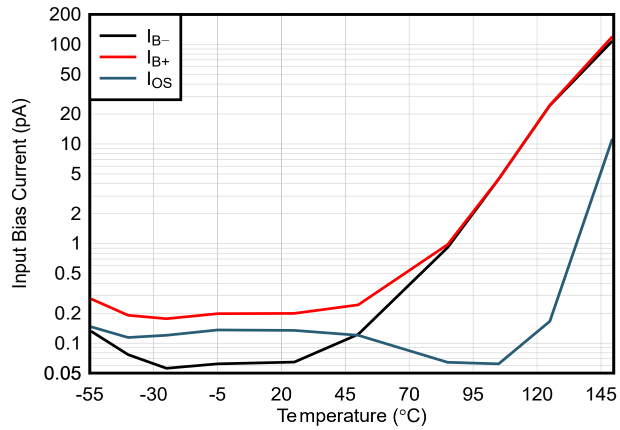


Figure 5-8. Input Bias Current vs Temperature

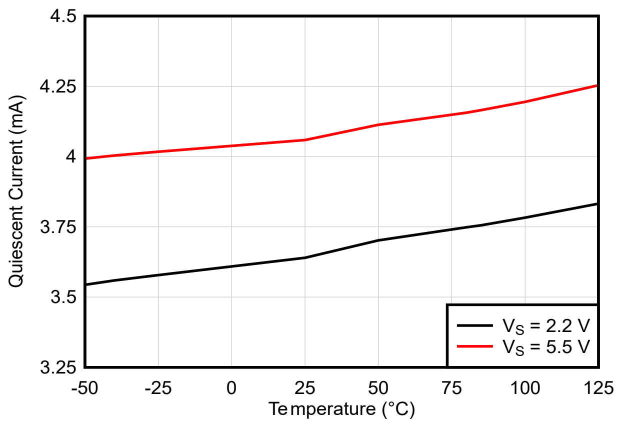


Figure 5-9. Quiescent Current vs Supply Voltage

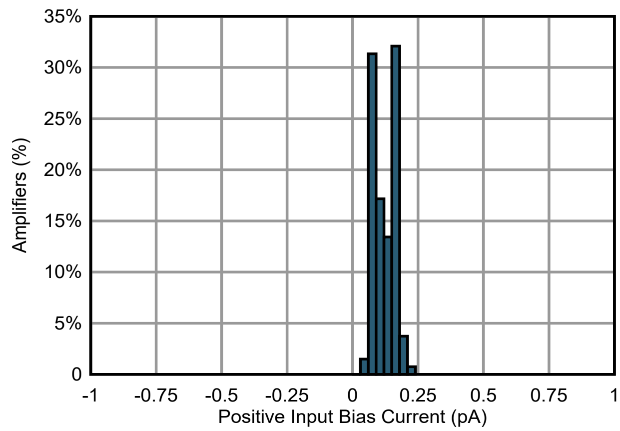


Figure 5-10. Positive Input Bias Current Distribution

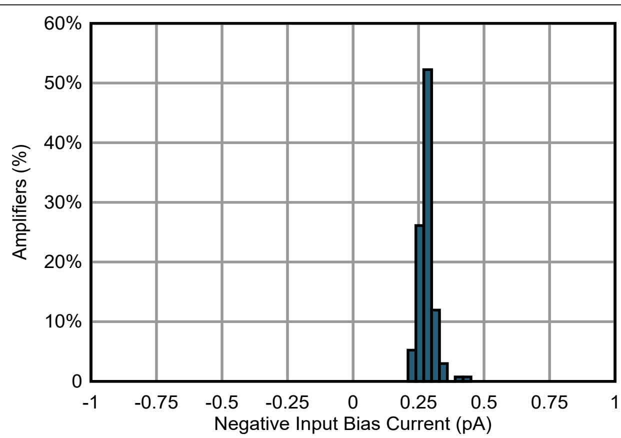


Figure 5-11. Negative Input Bias Current Distribution

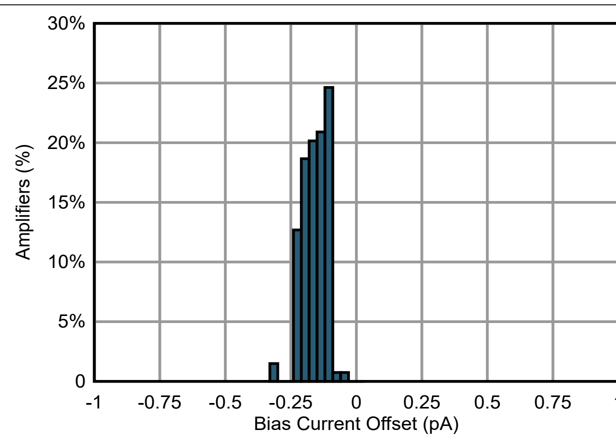


Figure 5-12. Input Bias Offset Current Distribution

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_{OUT} = mid-supply, C_L = 20 pF, and R_L = 10 kΩ (unless otherwise noted)

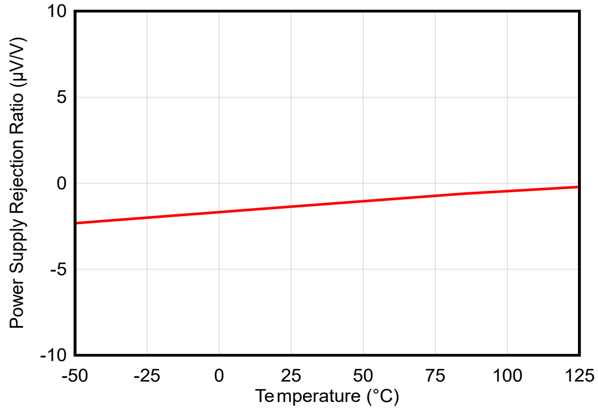


Figure 5-13. PSRR vs Temperature

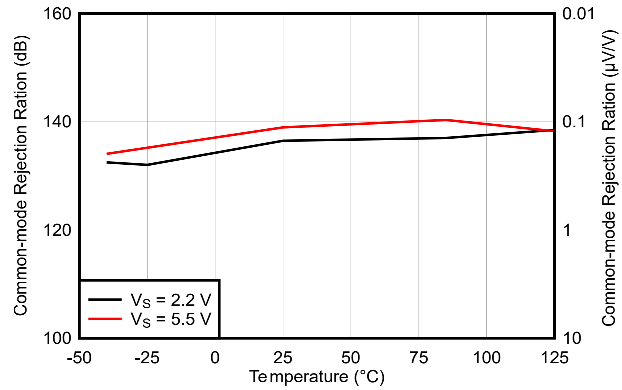


Figure 5-14. CMRR vs Temperature

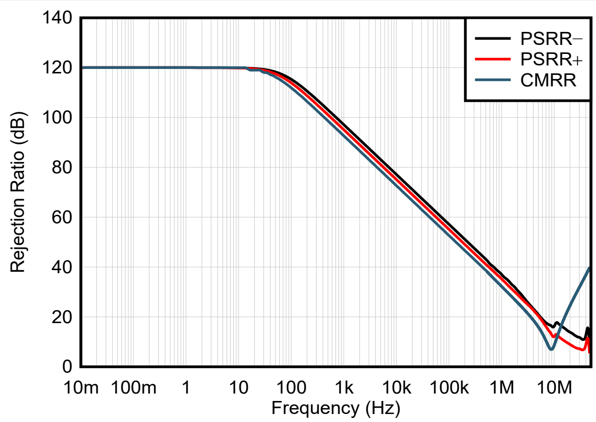


Figure 5-15. CMRR and PSRR vs Frequency

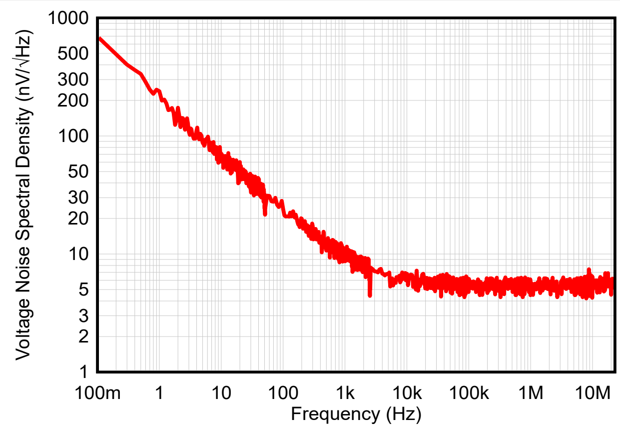


Figure 5-16. Input Voltage Noise Spectral Density vs Frequency

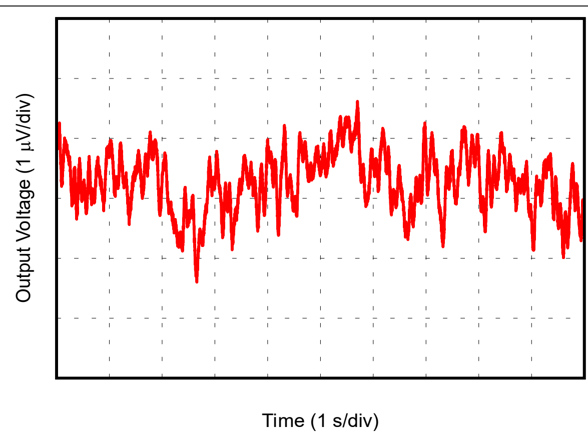


Figure 5-17. 0.1-Hz to 10-Hz Input Voltage Noise

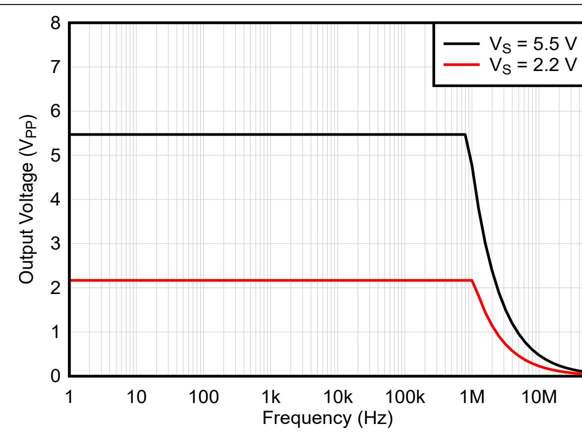
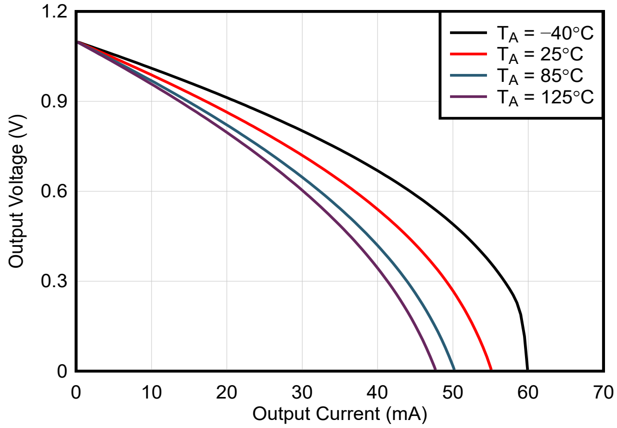


Figure 5-18. Maximum Output Voltage vs Frequency

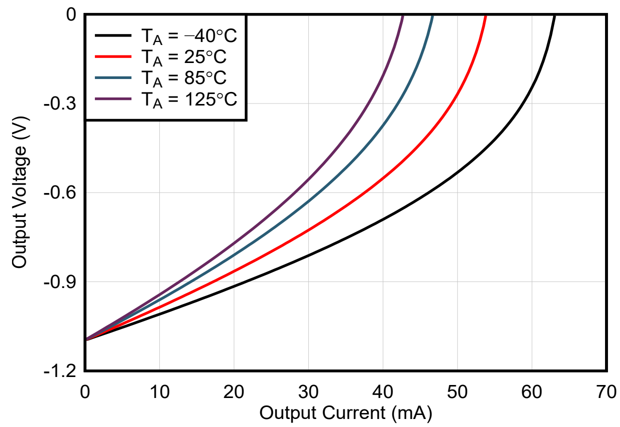
5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_{OUT} = mid-supply, C_L = 20 pF, and R_L = 10 kΩ (unless otherwise noted)



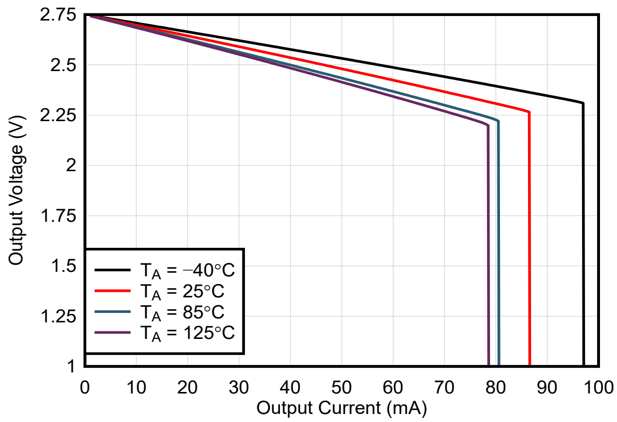
V_{V+} = 1.1 V, $V_{V–}$ = –1.1 V, current source load

Figure 5-19. Output Voltage Swing vs Output Current



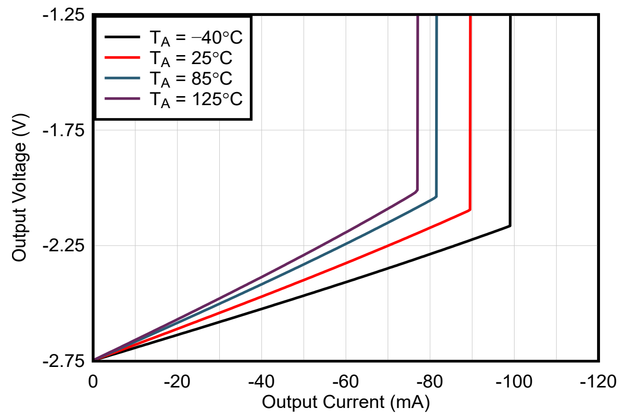
V_{V+} = 1.1 V, $V_{V–}$ = –1.1 V, current source load

Figure 5-20. Output Voltage Swing vs Output Current



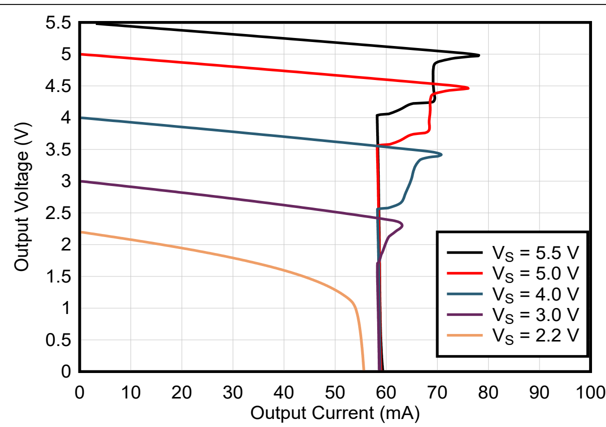
V_{V+} = 2.75 V, $V_{V–}$ = –2.75 V, current source load

Figure 5-21. Output Voltage Swing vs Output Current



V_{V+} = 2.75 V, $V_{V–}$ = –2.75 V, current source load

Figure 5-22. Output Voltage Swing vs Output Current



V_{V+} = 5.5 V, $V_{V–}$ = 0 V, voltage source load

Figure 5-23. Output Voltage Swing vs Output Current

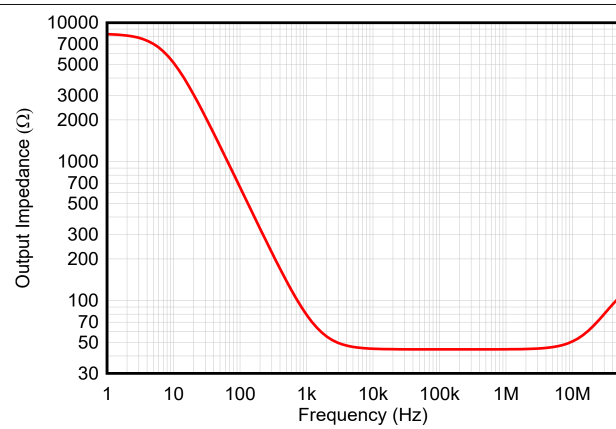


Figure 5-24. Open-Loop Output Impedance vs Frequency

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_{OUT} = mid-supply, C_L = 20 pF, and R_L = 10 kΩ (unless otherwise noted)

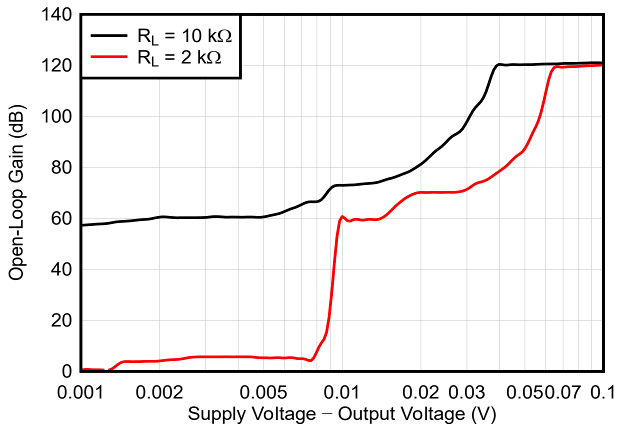
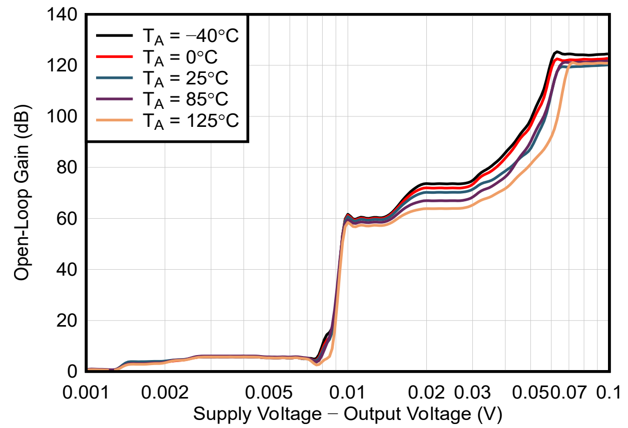
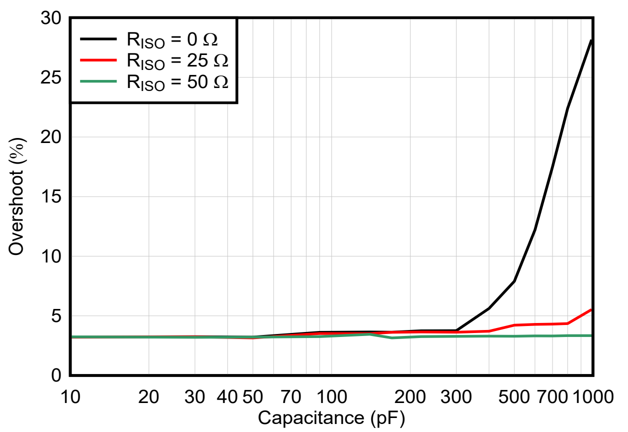


Figure 5-25. Open-Loop Gain vs Output to Supply Voltage Delta



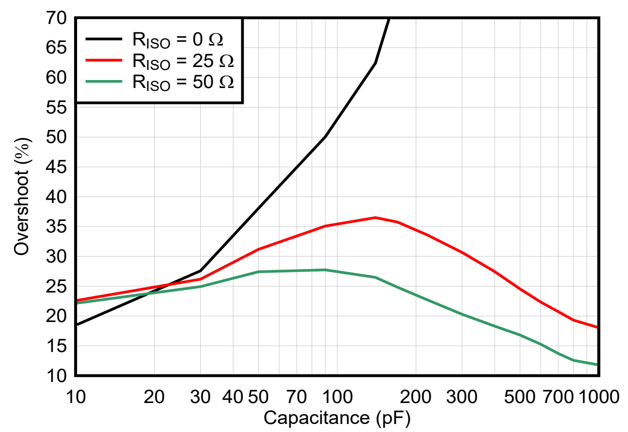
R_L = 2 kΩ

Figure 5-26. Open-Loop Gain vs Output to Supply Voltage Delta



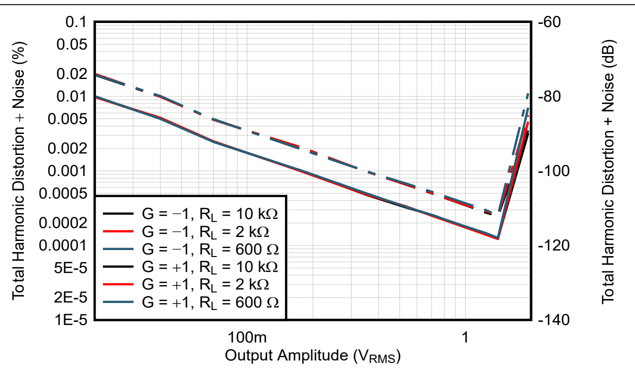
G = –1

Figure 5-27. Small-Signal Overshoot vs Load Capacitance



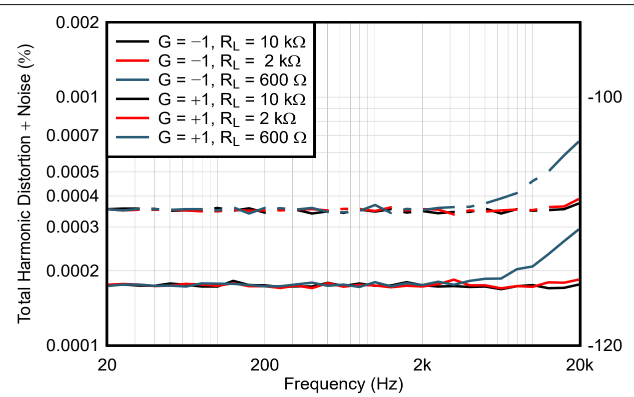
G = +1

Figure 5-28. Small-Signal Overshoot vs Load Capacitance



f = 1 kHz

Figure 5-29. THD+N vs Amplitude



V_{OUT} = 1 V_{RMS}

Figure 5-30. THD+N vs Frequency

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_{OUT} = mid-supply, C_L = 20 pF, and R_L = 10 kΩ (unless otherwise noted)

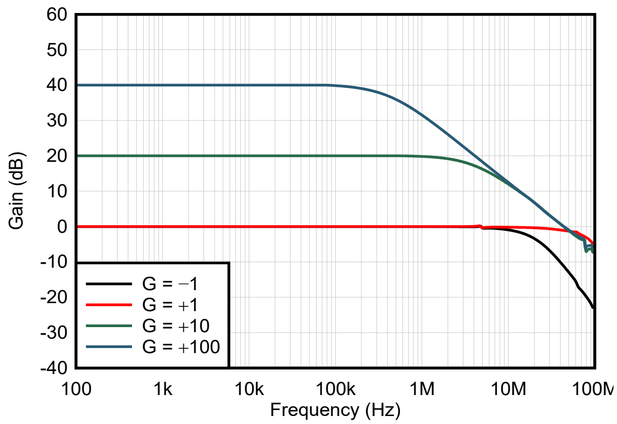


Figure 5-31. Closed-Loop Gain vs Frequency

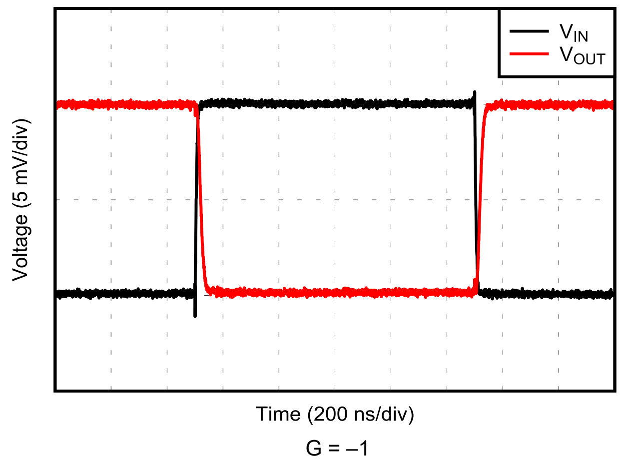


Figure 5-32. Small-Signal Step Response

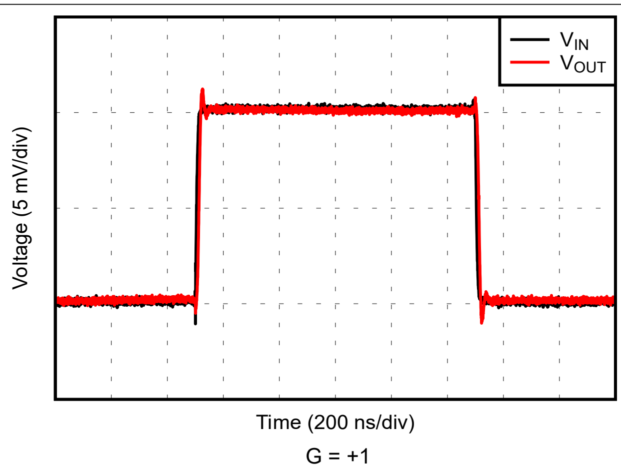


Figure 5-33. Small-Signal Step Response

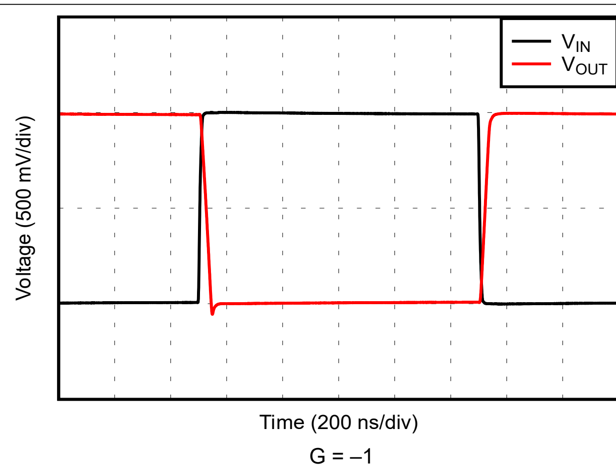


Figure 5-34. Large-Signal Step Response

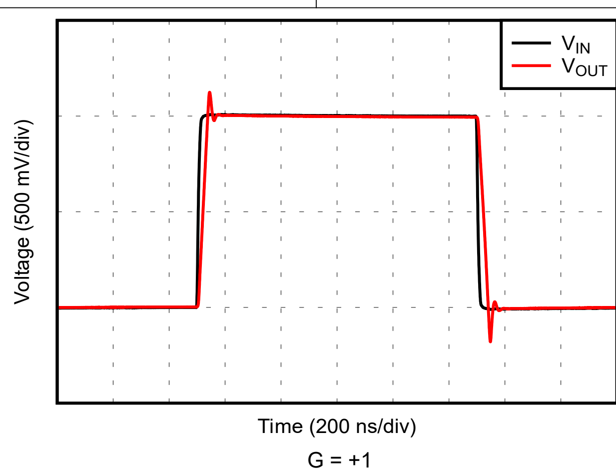


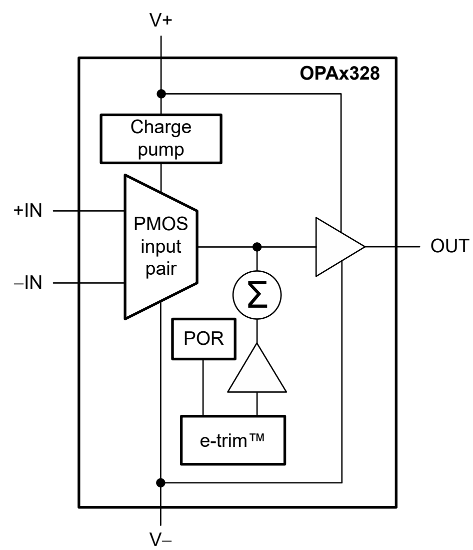
Figure 5-35. Large-Signal Step Response

6 Detailed Description

6.1 Overview

The OPAx328 family features high-speed, precision amplifiers that make this op amp family an excellent choice for driving high-resolution analog-to-digital converters (ADCs). Low output impedance with flat frequency characteristics and zero-crossover distortion circuitry enable high linearity over the full input common-mode range, achieving true rail-to-rail input from a 2.2-V to 5.5-V single supply.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Input and ESD Protection

The OPAx328 incorporate internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit input overdrive protection if the current is limited to 10 mA. Many input signals are inherently current-limited to less than 10 mA; therefore, a limiting resistor is not required. Figure 6-1 shows how a series input resistor (R_{IN}) can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input; therefore, keep this value to a minimum in noise-sensitive applications.

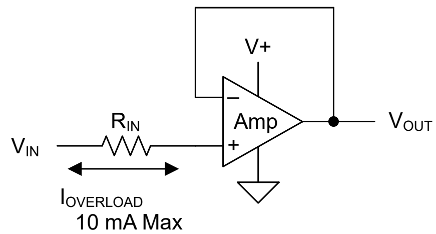


Figure 6-1. Input Current Protection

6.3.2 Rail-to-Rail Input

The OPAx328 feature true rail-to-rail input operation, with supply voltages as low as ±1.1 V (2.2 V). The design of the OPAx328 amplifiers includes an internal charge-pump that powers the amplifier input stage with an internal supply rail at approximately 1.6 V greater than the external supply (V_{S+}). This internal supply rail allows the single differential input pair to operate and remain very linear over a very-wide input common-mode range. A unique zero-crossover input topology eliminates the input offset transition region typical of many rail-to-rail, complementary-input-stage operational amplifiers. This topology allows the OPAx328 to provide excellent common-mode performance (CMRR > 120 dB, typical) over the entire common-mode input range, which extends 100 mV beyond both power-supply rails. When driving analog-to-digital converters (ADCs), the highly linear V_{CM} range of the OPAx328 provides maximum linearity and lowest distortion.

6.3.3 Phase Reversal

The OPAx328 op amps are designed to be immune to phase reversal when the input pins exceed the supply voltages, and thus provide further in-system stability and predictability. Figure 6-2 shows the input voltage exceeding the supply voltage without any phase reversal.

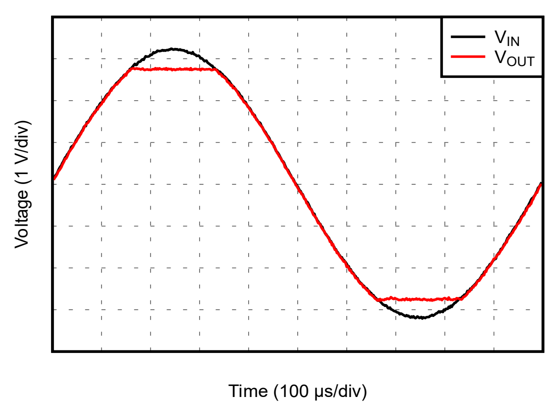


Figure 6-2. No Phase Reversal

6.4 Device Functional Modes

The OPAx328 operational amplifier is operational when power-supply voltages between 2.2 V to 5.5 V are applied. Devices with an *S* suffix have shutdown capability.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx328 offer outstanding dc and ac performance. These devices operate with up to a 5.5-V power supply, and offer an ultra-low input bias current and a 40-MHz bandwidth. These features make the OPAx328 family of robust operational amplifiers great for both communication and industrial applications.

7.1.1 Capacitive Load and Stability

The OPAx328 are designed for use in high-speed applications for transimpedance amplifiers (TIA) and ADC input-driving amplifiers. As with all op amps, there can be specific instances where the OPAx328 become unstable. The particular op-amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation. An op amp in the unity-gain (1-V/V) buffer configuration driving a capacitive load exhibits a greater tendency to become unstable compared to an amplifier operating at a higher noise gain (see Figure 5-28). The capacitive load, in conjunction with the op-amp output impedance, creates a pole within the loop gain that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPAx328 remain stable with a pure capacitive load up to 100 pF.

Figure 7-1 shows one technique to increase the capacitive load drive capability of an amplifier operating in a unity-gain configuration is to insert a small resistor (R_S), typically 10 Ω to 50 Ω, in series with the output. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads.

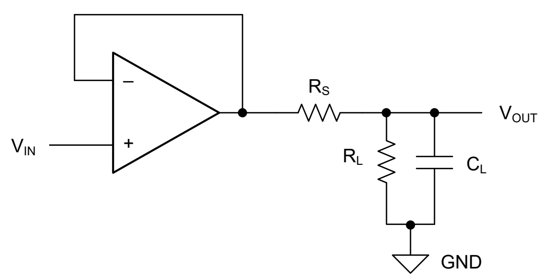


Figure 7-1. Improving Capacitive Load Drive

7.2 Typical Applications

7.2.1 Bidirectional Current-Sensing

This single-supply, low-side, bidirectional current-sensing design example detects load currents from –1 A to +1 A. The single-ended output spans from 110 mV to 3.19 V. This design uses the OPAx328 because of the low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other amplifier provides the reference voltage.

Figure 7-2 shows the schematic.

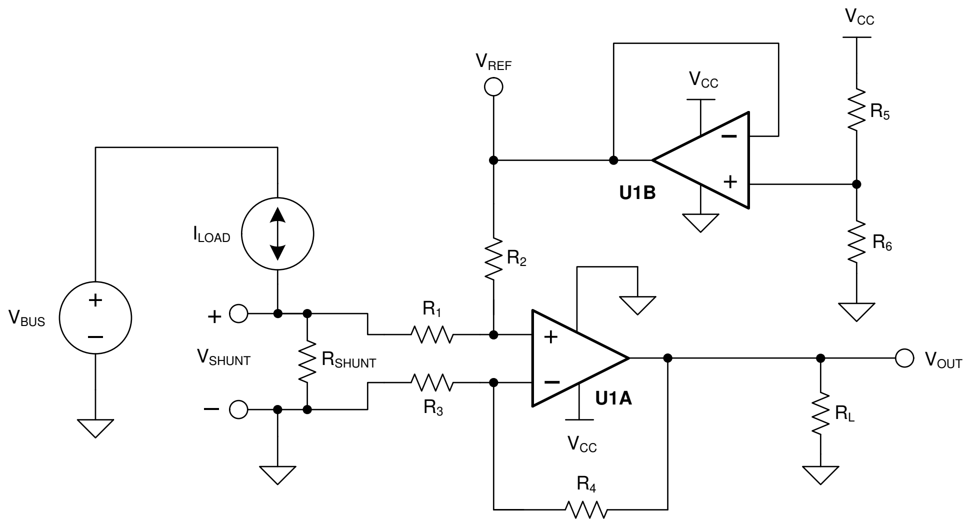


Figure 7-2. Bidirectional Current-Sensing Schematic

7.2.1.1 Design Requirements

This design example has the following requirements:

- Supply voltage: 3.3 V
- Input: –1 A to +1 A
- Output: 1.65 V ±1.54 V (110 mV to 3.19 V)

7.2.1.2 Detailed Design Procedure

The load current, I_{LOAD}, flows through the shunt resistor, R_{SHUNT}, to develop the shunt voltage, V_{SHUNT}. The shunt voltage is then amplified by the difference amplifier consisting of U1A and R_1 through R_4. The gain of the difference amplifier is set by the ratio of R_4 to R_3. To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF}, is supplied by buffering a resistor divider using U1B. The transfer function is given by Equation 1.

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff\_Amp} + V_{REF} \quad (1)$$

where

- $V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$
- $Gain_{Diff\_Amp} = \dfrac{R_4}{R_3}$
- $V_{REF} = V_{CC} \times \left(\dfrac{R_6}{R_5 + R_6} \right)$

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4 / R_3 matches R_2 / R_1. The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

The value of V_{SHUNT} is the ground potential for the system load because V_{SHUNT} is a low-side measurement. Therefore, a maximum value must be placed on V_{SHUNT}. In this design, the maximum value for V_{SHUNT} is set to 100 mV. Equation 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100 mV and maximum load current of 1 A.

$$R_{SHUNT(Max)} = \frac{V_{SHUNT(Max)}}{I_{LOAD(Max)}} = \frac{100\ \text{mV}}{1\ \text{A}} = 100\ \text{m}\Omega \quad (2)$$

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% is selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is –100 mV to +100 mV. This voltage is divided down by R_1 and R_2 before reaching the operational amplifier, U1A. Make sure that the voltage present at the noninverting node of U1A is within the common-mode range of the device. Therefore, use an operational amplifier, such as the OPAx328, that has a common-mode range that extends below the negative supply voltage. Finally, to minimize offset error, the OPAx328 have a typical offset voltage of merely ±3 µV (±25 µV maximum).

Given a symmetric load current of –1 A to +1 A, the voltage divider resistors (R_5 and R_6) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% is selected. To minimize power consumption, 10-kΩ resistors are used.

To set the gain of the difference amplifier, the common-mode range and output swing of the OPAx328 must be considered. Equation 3 and Equation 4 depict the typical common-mode range and maximum output swing, respectively, of the OPAx328 given a 3.3-V supply.

$$-100\ \text{mV} < V_{CM} < 3.4\ \text{V} \tag{3}$$

$$100\ \text{mV} < V_{OUT} < 3.2\ \text{V} \tag{4}$$

The gain of the difference amplifier can now be calculated as shown in Equation 5:

$$\text{Gain}_{\text{Diff\_Amp}} = \frac{V_{\text{OUT\_Max}} - V_{\text{OUT\_Min}}}{R_{\text{SHUNT}} \times (I_{\text{MAX}} - I_{\text{MIN}})} = \frac{3.2\ \text{V} - 100\ \text{mV}}{100\ \text{m}\Omega \times [1\ \text{A} - (-\ 1\text{A})]} = 15.5\ \frac{\text{V}}{\text{V}} \tag{5}$$

The resistor value selected for R_1 and R_3 is 1 kΩ. A value of 15.4 kΩ is selected for R_2 and R_4 because this number is the nearest standard value. Therefore, the calculated gain of the difference amplifier is 15.4 V/V.

The gain error of the circuit primarily depends on R_1 through R_4. As a result of this dependence, 0.1% resistors are selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

7.2.1.3 Application Curve

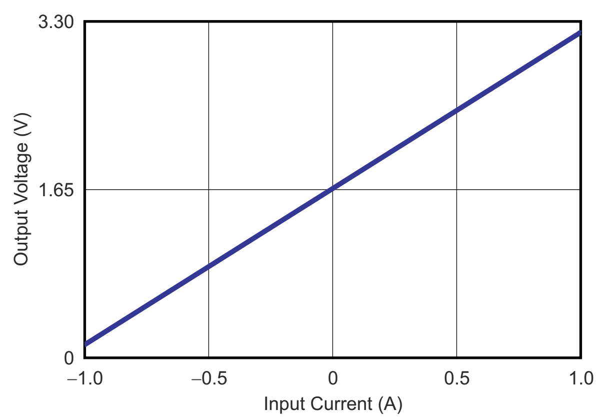


Figure 7-3. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs Input Current

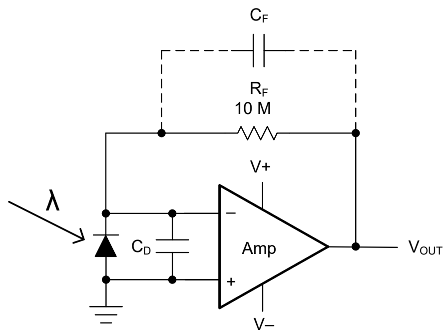
7.2.2 Transimpedance Amplifier

Wide gain bandwidth, low input bias current, low input voltage, and low current noise make the OPAx328 excellent wideband photodiode transimpedance amplifiers. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

Figure 7-4 shows that the key elements to a transimpedance design are the:

- Expected diode capacitance (C_D), including the parasitic input common-mode voltage and differential-mode input capacitance
- Desired transimpedance gain (R_F)
- Gain-bandwidth (GBW) = 40 MHz

With these three variables set, the feedback capacitor (C_F) value can be set to control the frequency response. C_F includes the stray capacitance of R_F, which is 0.2 pF for a typical surface-mount resistor.



NOTE: C_F is optional to prevent gain peaking, and includes the stray capacitance of R_F.

Figure 7-4. Dual-Supply Transimpedance Amplifier

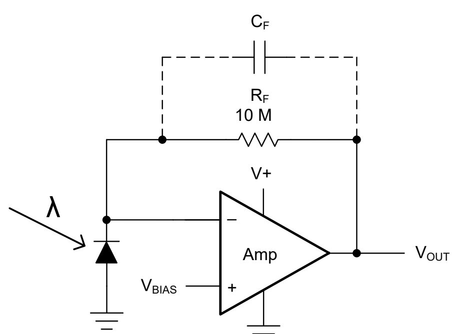
For an optimized frequency response, use Equation 6 to set the feedback pole:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBW}{4\pi R_F C_D}} \tag{6}$$

Equation 7 calculates the bandwidth:

$$f_{-3dB} = \sqrt{\frac{GBW}{2\pi R_F C_D}} \quad \text{(Hz)} \tag{7}$$

For single-supply applications, the +IN input can be biased with a positive dc voltage to allow the output to reach true zero when the photodiode is not exposed to any light, and respond without the added delay that results from coming out of the negative rail. Figure 7-5 shows this configuration. This bias voltage also appears across the photodiode, providing a reverse bias for faster operation.



NOTE: C_F is optional to prevent gain peaking, and includes the stray capacitance of R_F.

Figure 7-5. Single-Supply Transimpedance Amplifier

For more information, see the *Compensate Transimpedance Amplifiers Intuitively* application report.

7.3 Power Supply Recommendations

The OPAx328 are specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Section 5.7*.

CAUTION

Supply voltages greater than 6 V can permanently damage the device; see *Section 5.1*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Section 7.4*.

7.4 Layout

7.4.1 Layout Guidelines

The OPA328 is a wideband amplifier. To realize the full operational performance of this device, use good, high-frequency PCB layout practices. Connect the bypass capacitors between each supply pin and ground, as close to the device as possible. Design the bypass capacitor traces for minimum inductance.

7.4.2 Layout Example

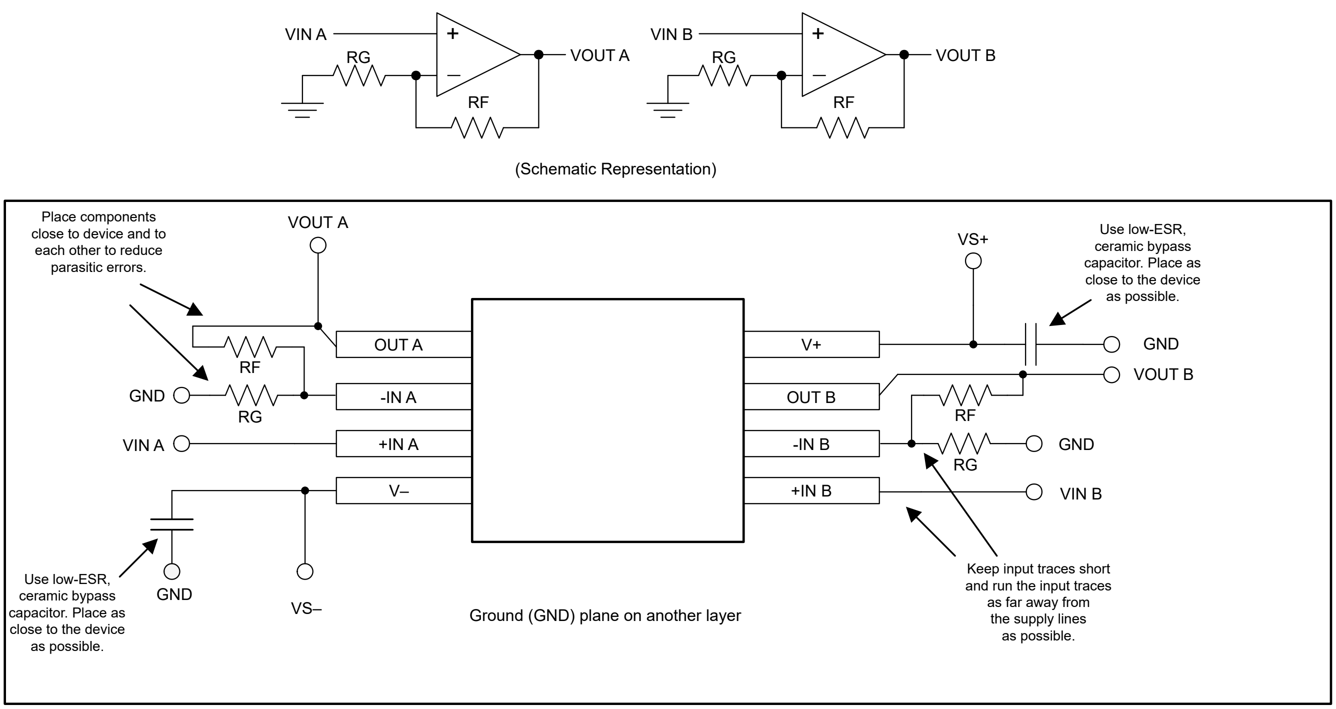


Figure 7-6. Operational Amplifier Board Layout for Noninverting Configuration

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

8.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design and simulation tools web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

8.1.1.3 DIP-Adapter-EVM

Speed up your op amp prototyping and testing with the DIP-Adapter-EVM, which provides a fast, easy and inexpensive way to interface with small, surface-mount devices. Connect any supported op amp using the included Samtec terminal strips or wire them directly to existing circuits. The DIP-Adapter-EVM kit supports the following industry-standard packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT-23-6, SOT-23-5 and SOT-23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6).

8.1.1.4 DIYAMP-EVM

The DIYAMP-EVM is a unique evaluation module (EVM) that provides real-world amplifier circuits, enabling the user to quickly evaluate design concepts and verify simulations. This EVM is available in three industry-standard packages (SC70, SOT23, and SOIC) and 12 popular amplifier configurations, including amplifiers, filters, stability compensation, and comparator configurations for both single and dual supplies.

8.1.1.5 Analog Filter Designer

Available as a web-based tool from the Design and simulation tool web page, the Analog Filter Designer allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

8.2 Documentation Support

8.2.1 Related Documentation

The following documents are recommended as a reference for this device, and available for download at www.ti.com:

- Texas Instruments, *Software Pacemaker Detection* design guide
- Texas Instruments, *TIDA-00378 Schematic and Block Diagram*
- Texas Instruments, *PM2.5/PM10 Particle Sensor Analog Front-End for Air Quality Monitoring Design* design guide
- Texas Instruments, *QFN/SON PCB Attachment* application note
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application note
- Texas Instruments, *Compensate Transimpedance Amplifiers Intuitively* application note
- Texas Instruments, *Noise Analysis of FET Transimpedance Amplifiers* application note
- Texas Instruments, *Noise Analysis for High-Speed Op Amps* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (December 2023) to Revision E (January 2025)	Page
• Added OPA2328 YBJ package to *Device Information*	1
• Added OPA2328 YBJ (WCSP, 24) pin configuration and pin functions table	3
• Added YBJ (DSBGA) package to *Thermal Information - OPA2328*	7

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2328DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2K6S
OPA2328DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2K6S
OPA2328DGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2K6S
OPA2328DGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2K6S
OPA2328DR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2328W
OPA2328DR.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2328W
OPA2328DRGR	Active	Production	SON (DRG) | 8	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2328W
OPA2328DRGR.A	Active	Production	SON (DRG) | 8	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2328W
OPA2328YBJR	Active	Production	DSBGA (YBJ) | 24	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	OPA2328
OPA2328YBJR.A	Active	Production	DSBGA (YBJ) | 24	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	OPA2328
OPA328DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OP328
OPA328DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OP328

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

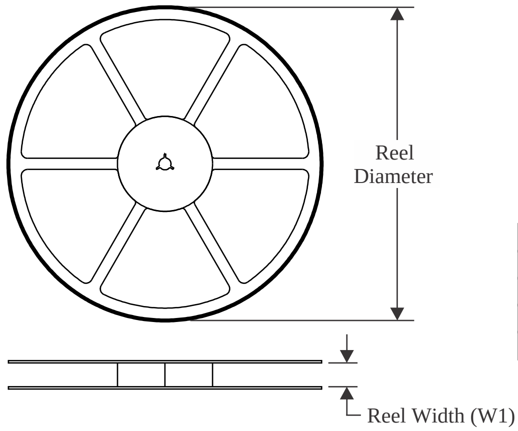
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

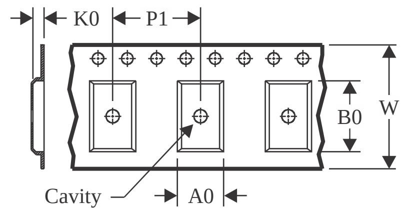
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

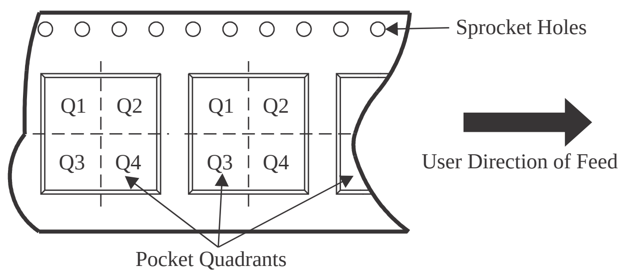


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

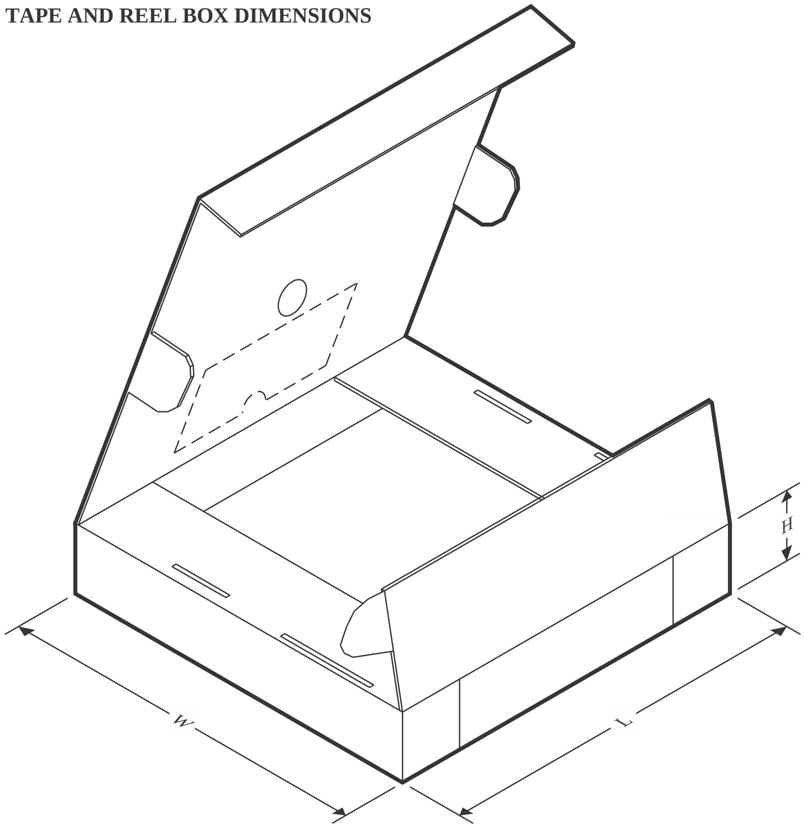
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

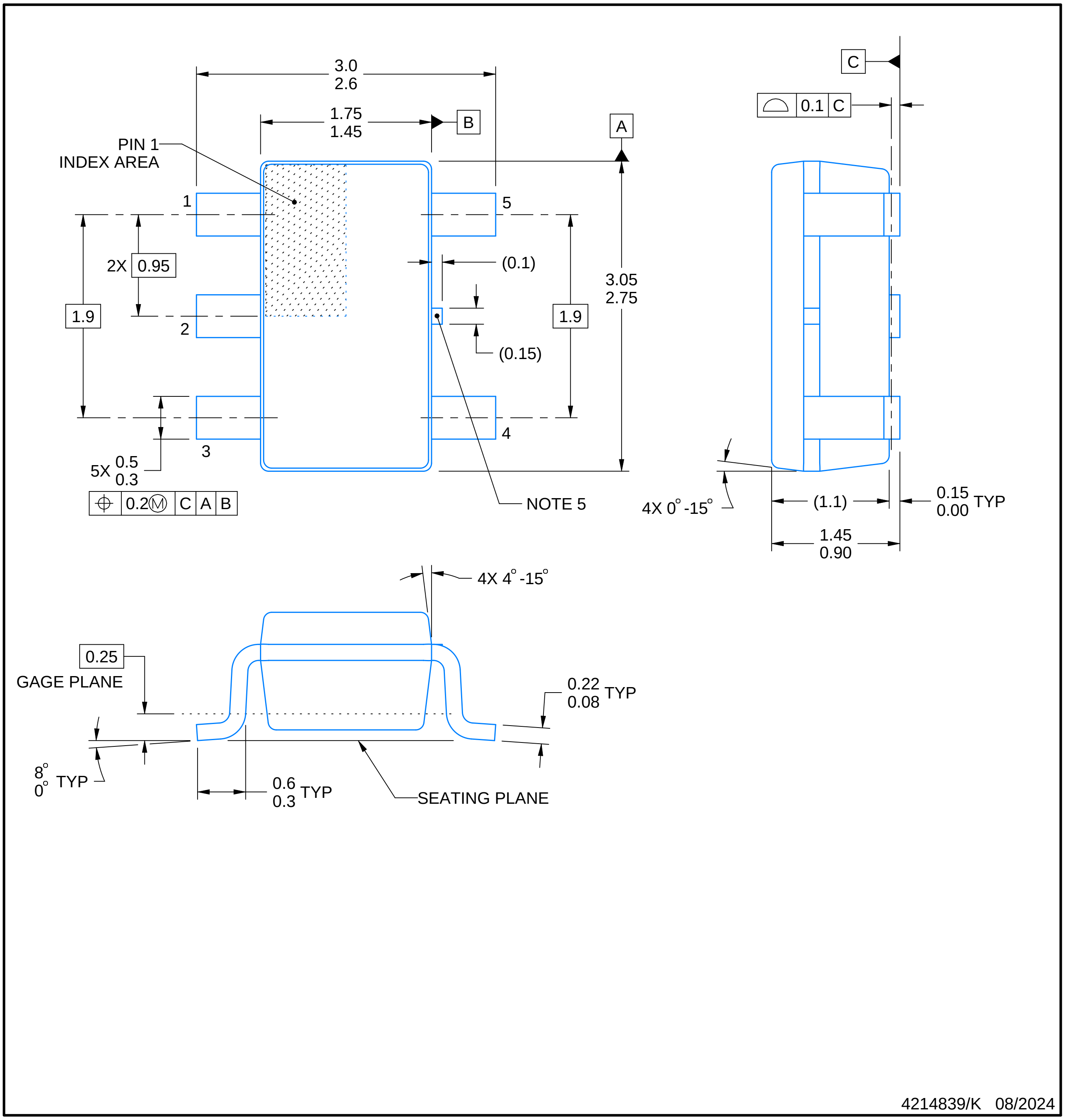
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2328DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2328DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2328DRGR	SON	DRG	8	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2328YBJR	DSBGA	YBJ	24	3000	180.0	8.4	2.24	2.24	0.45	4.0	8.0	Q1
OPA328DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



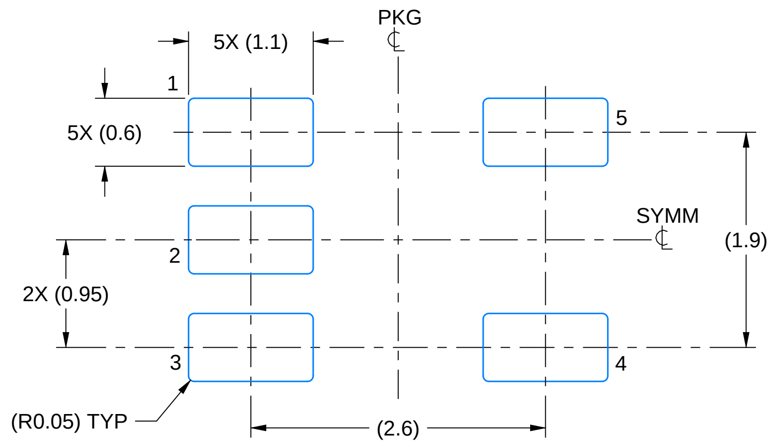
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2328DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2328DR	SOIC	D	8	3000	353.0	353.0	32.0
OPA2328DRGR	SON	DRG	8	5000	367.0	367.0	35.0
OPA2328YBJR	DSBGA	YBJ	24	3000	182.0	182.0	20.0
OPA328DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

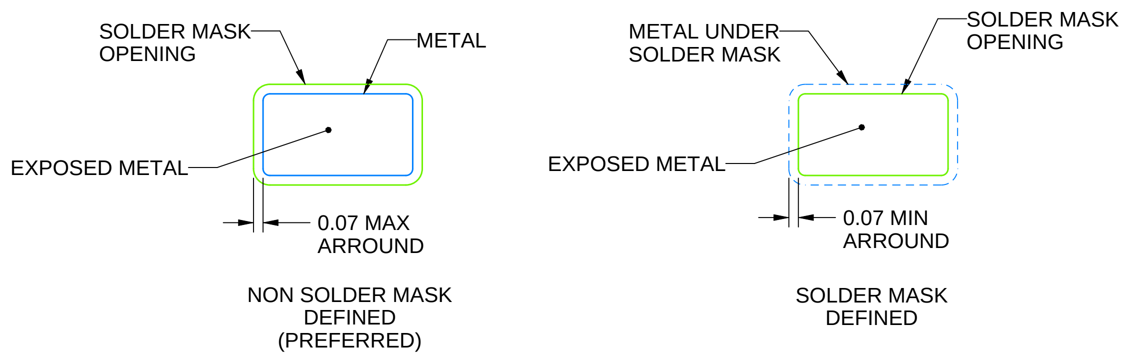


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

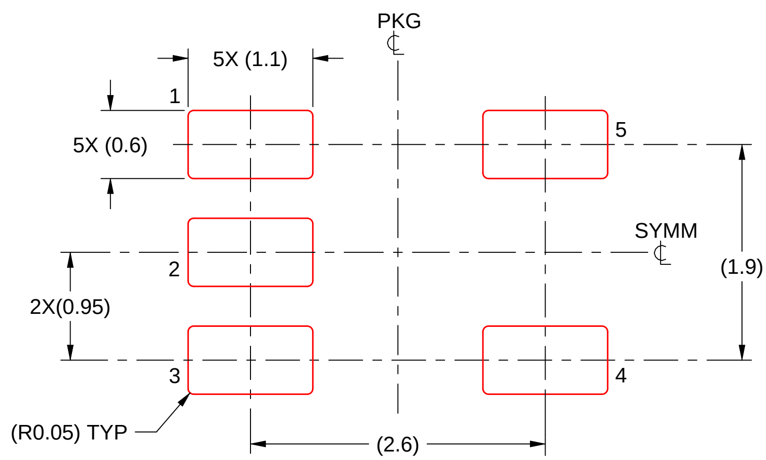


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

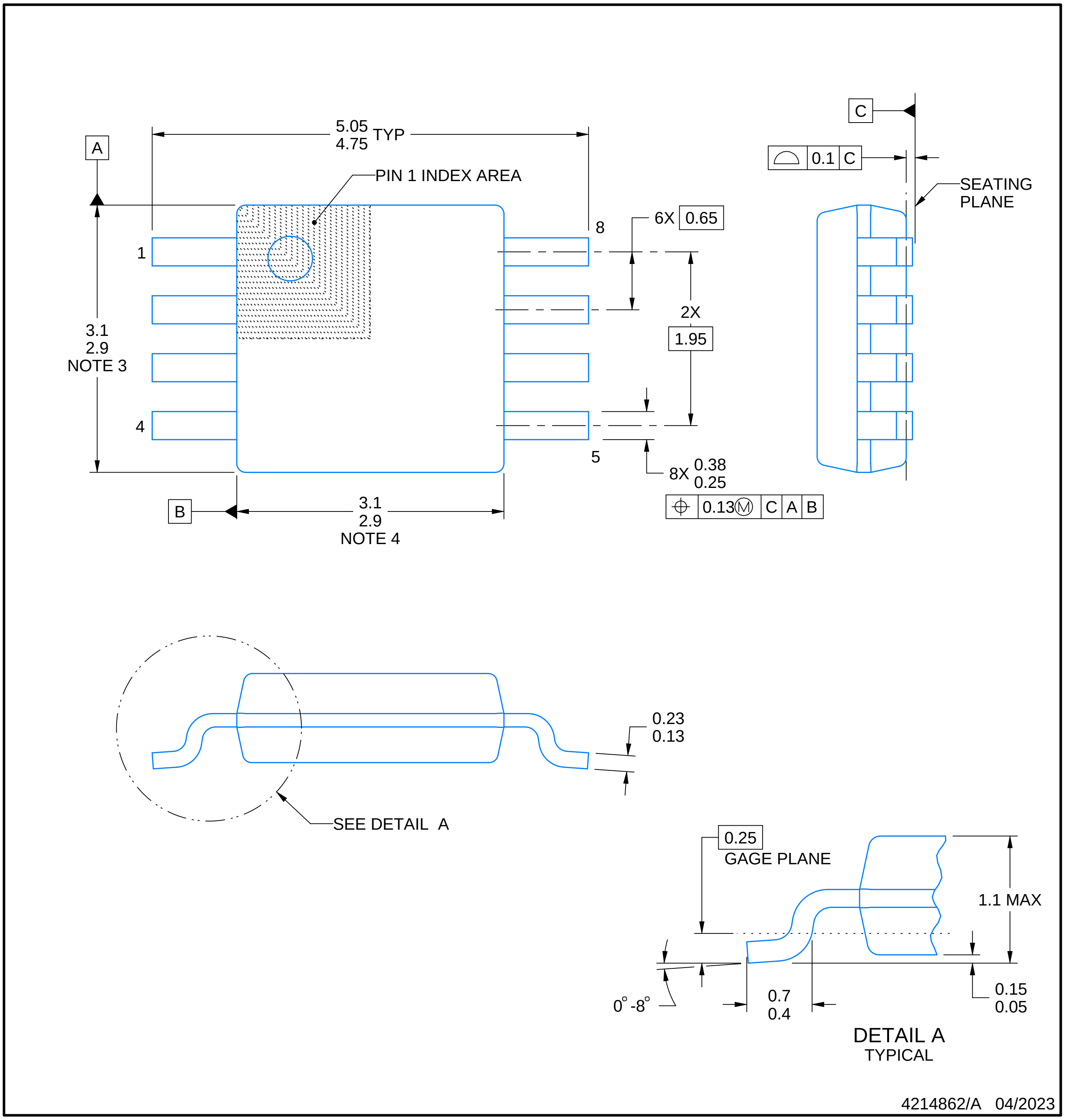


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

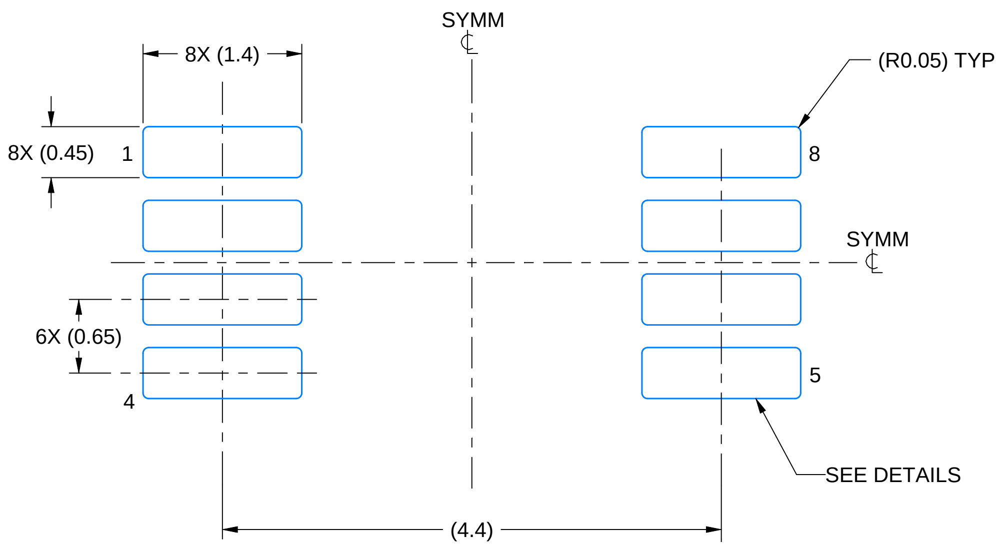
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



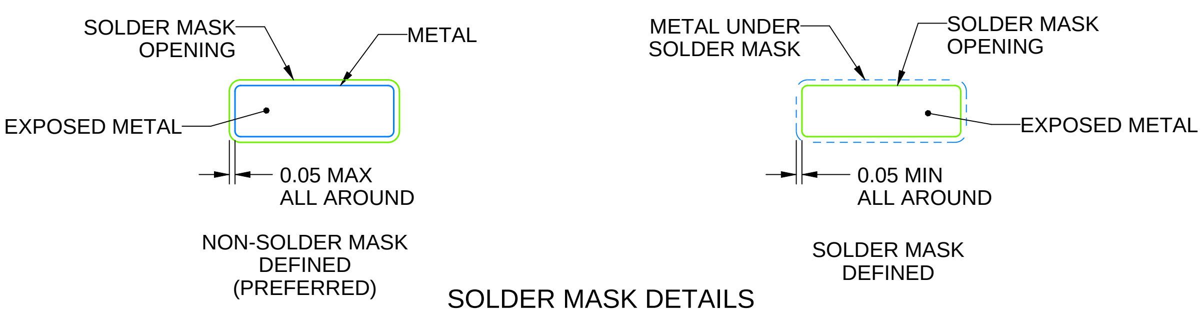
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

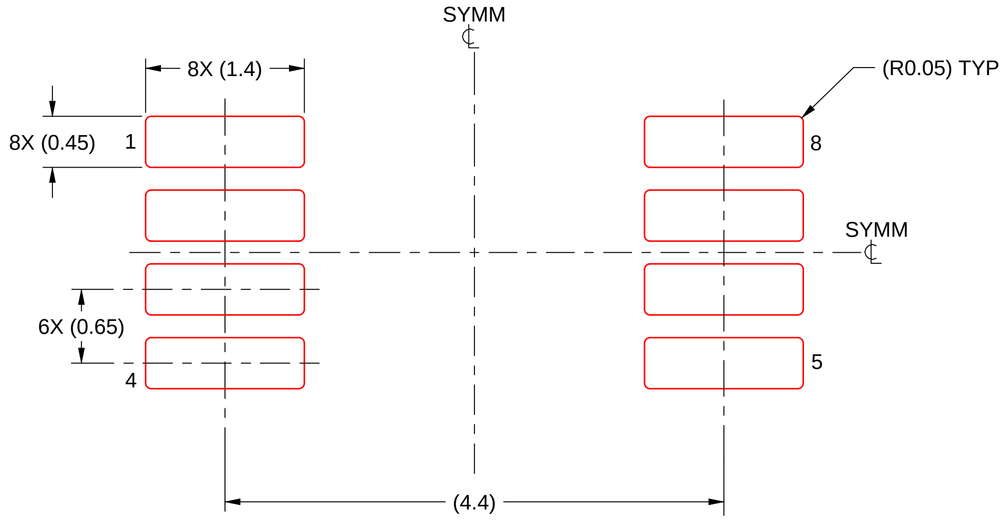


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

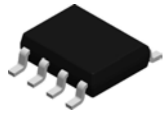


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

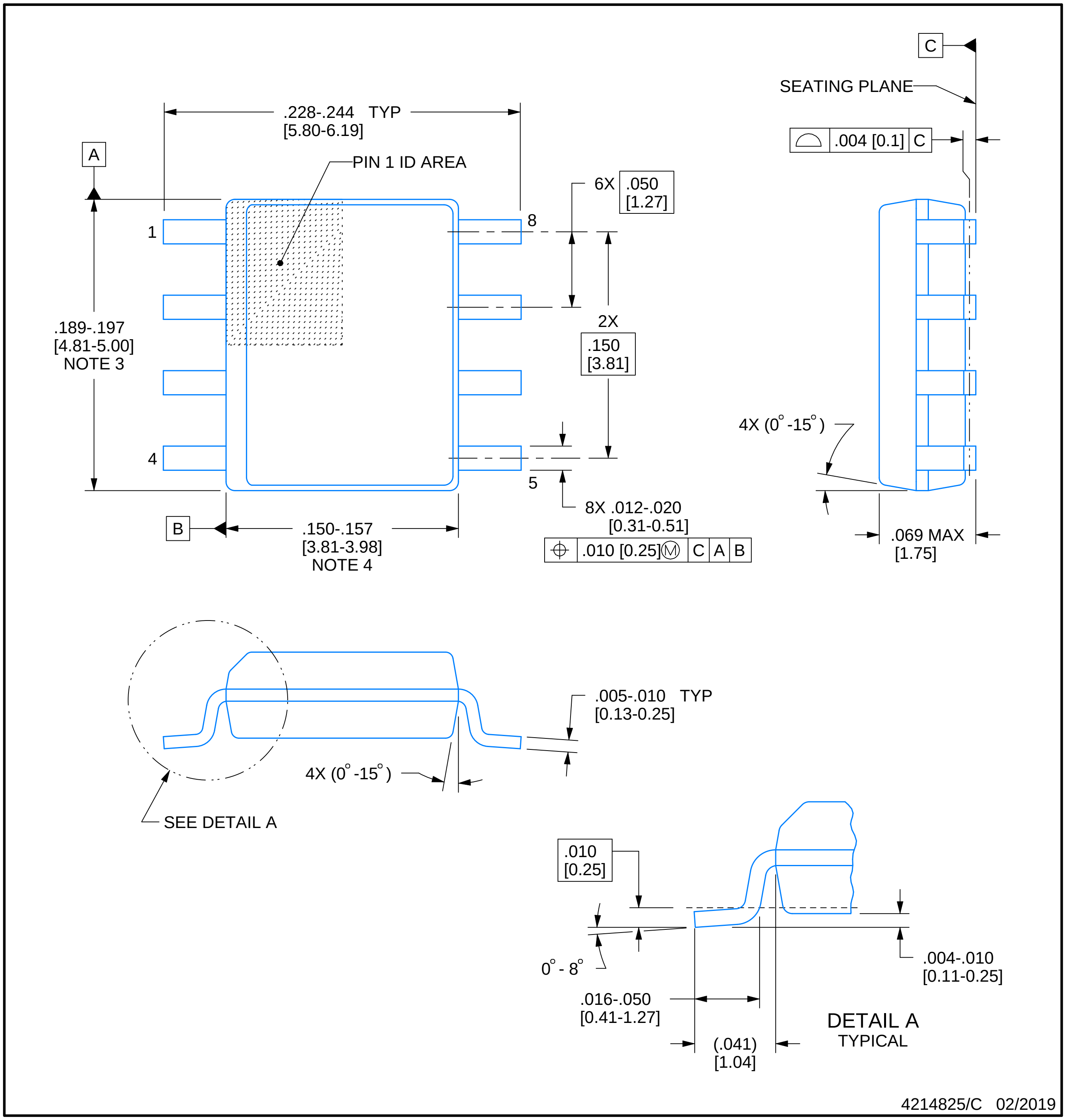
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

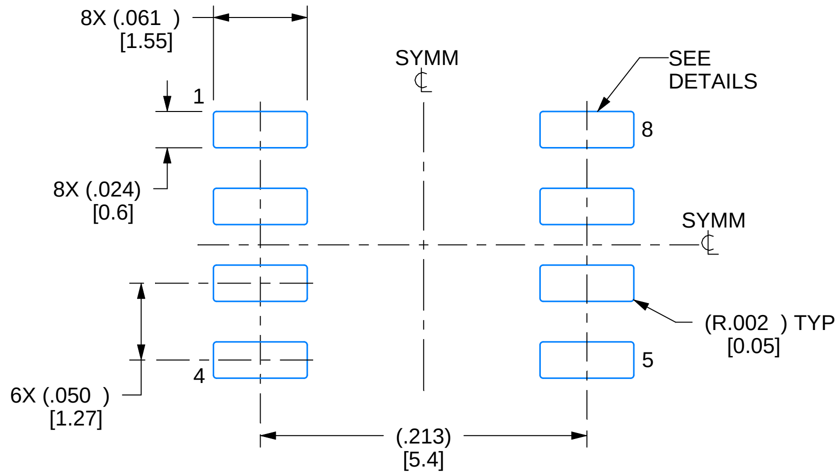
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

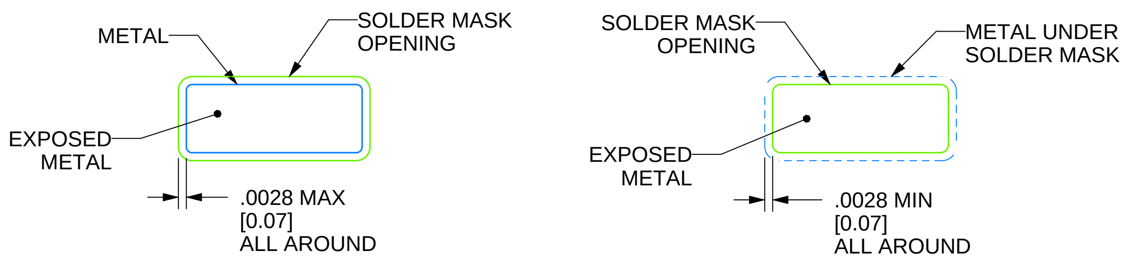


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

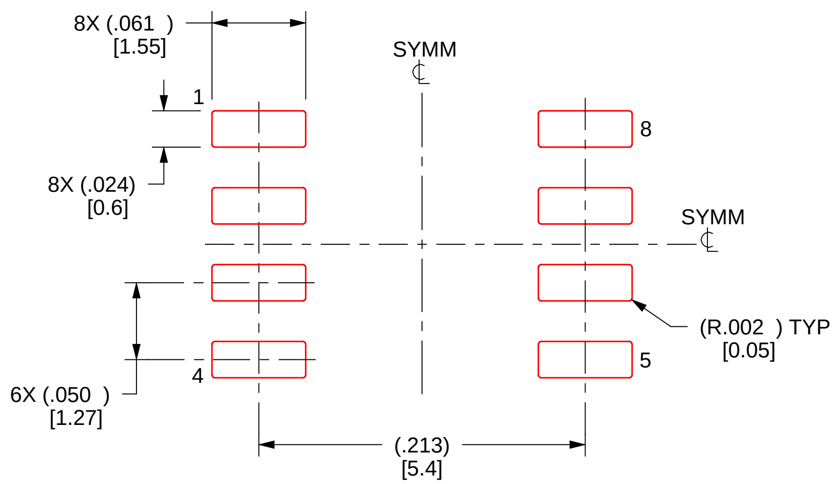
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

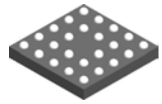


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

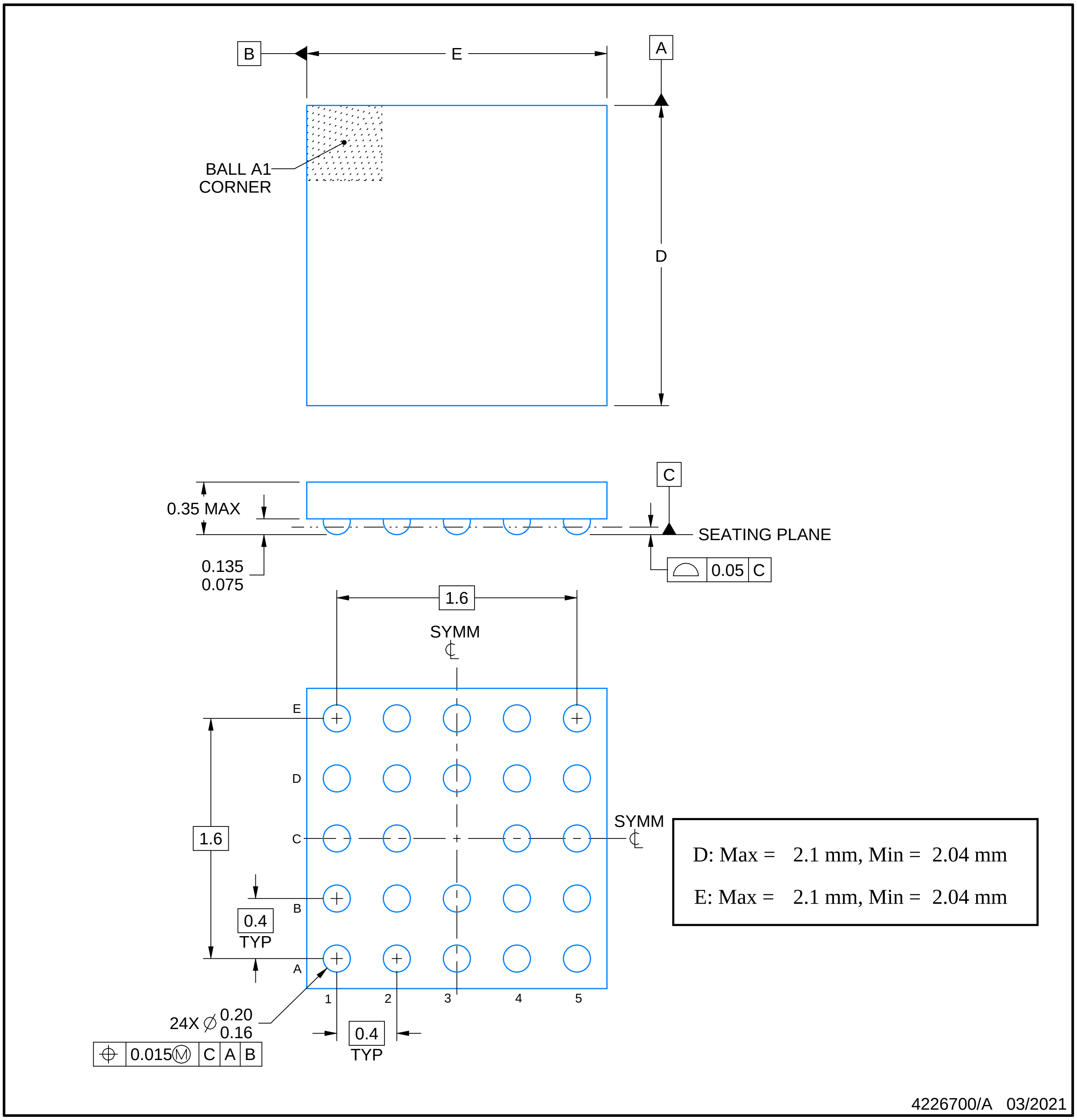


PACKAGE OUTLINE

YBJ0024

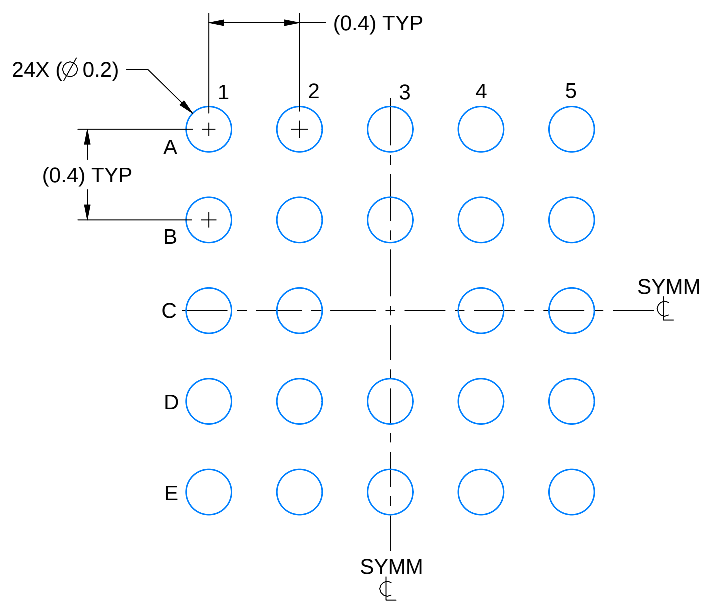
DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY

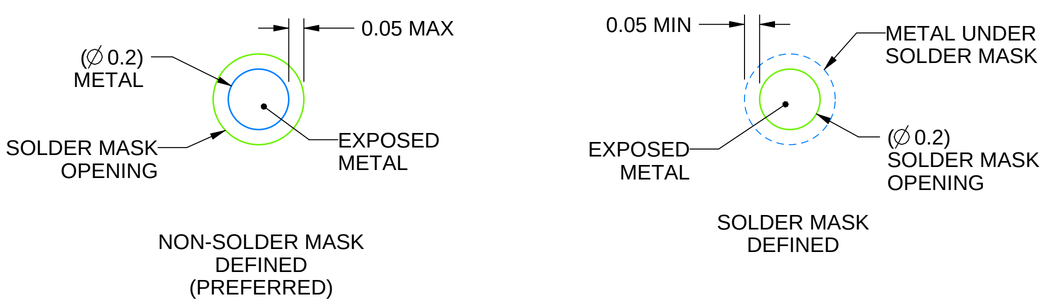


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

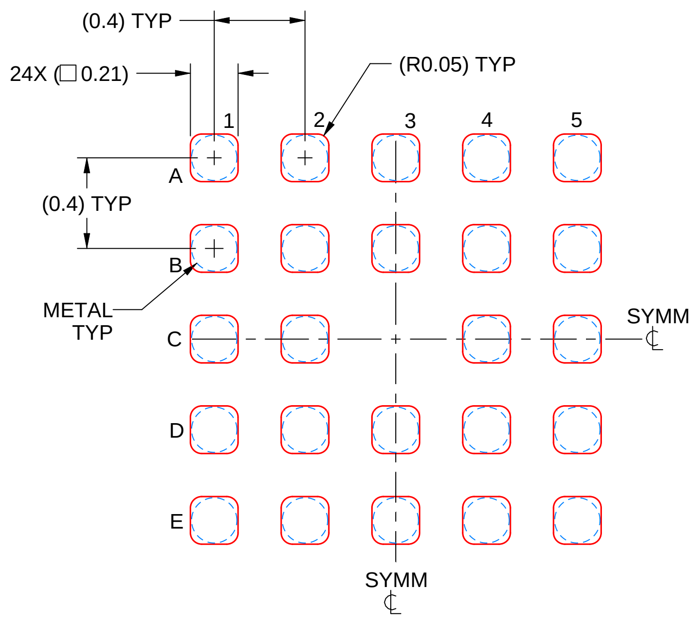


SOLDER MASK DETAILS
NOT TO SCALE

4226700/A 03/2021

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



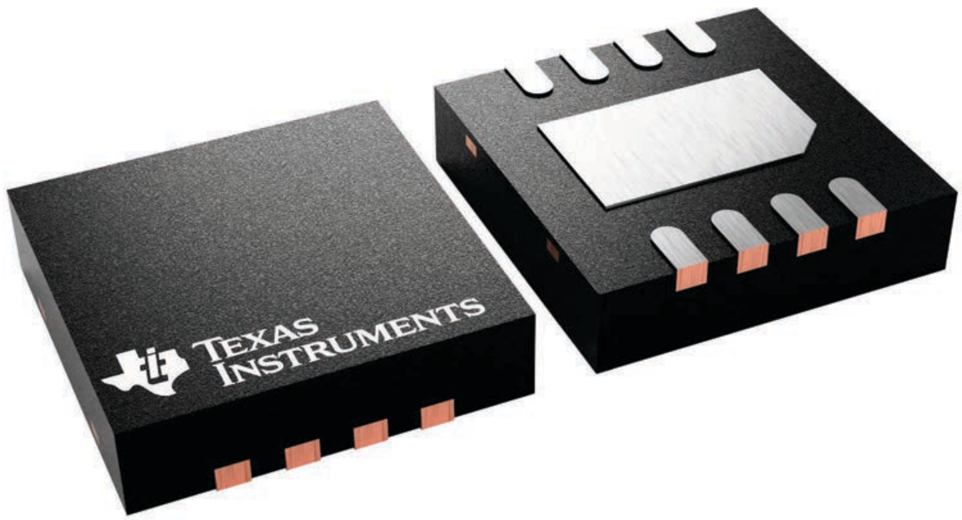
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

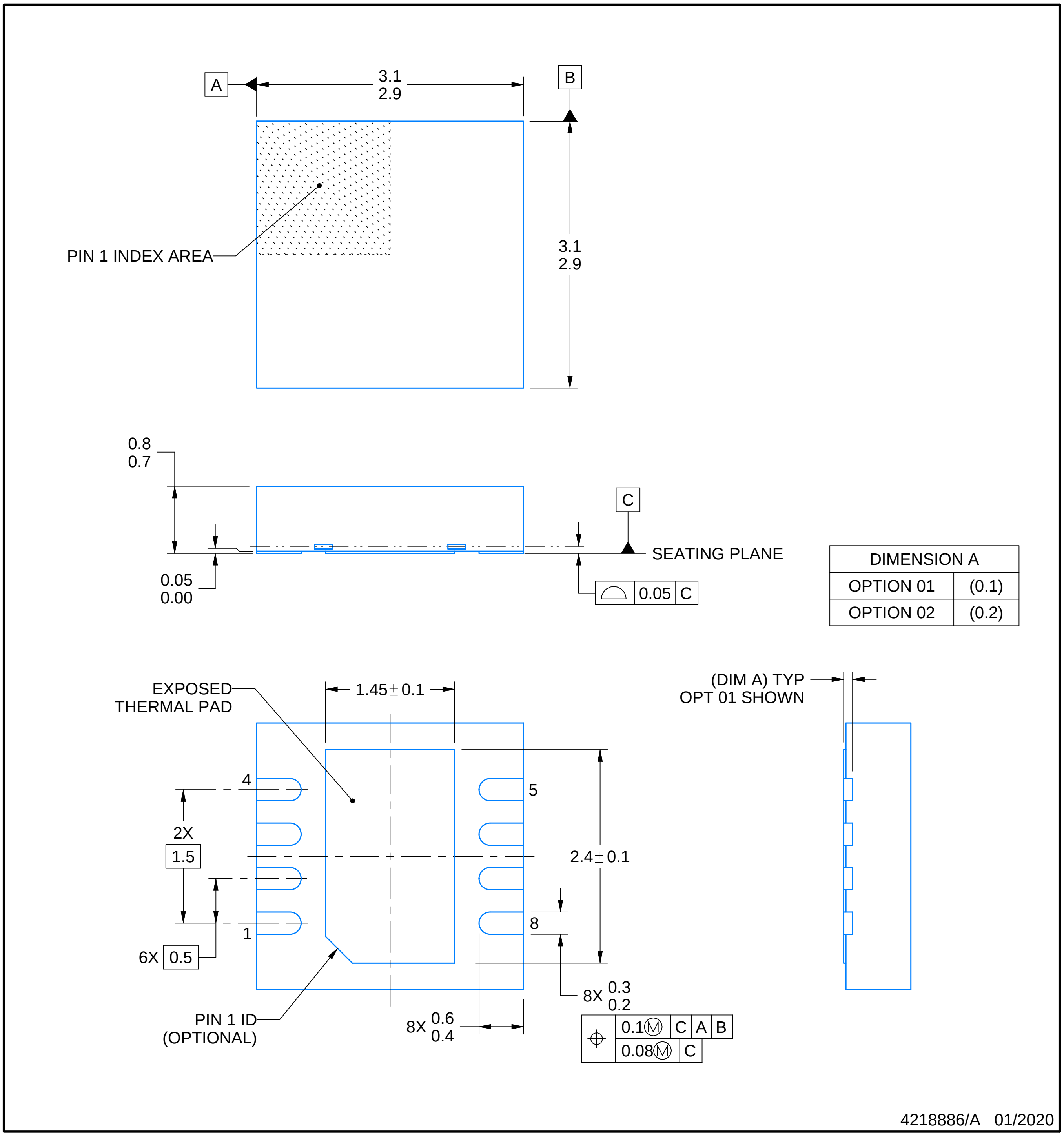
4226700/A 03/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

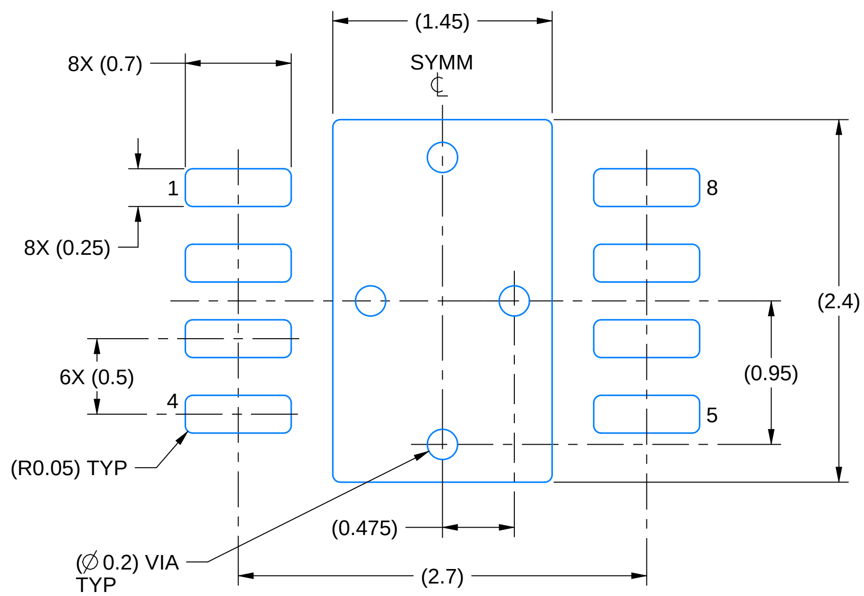




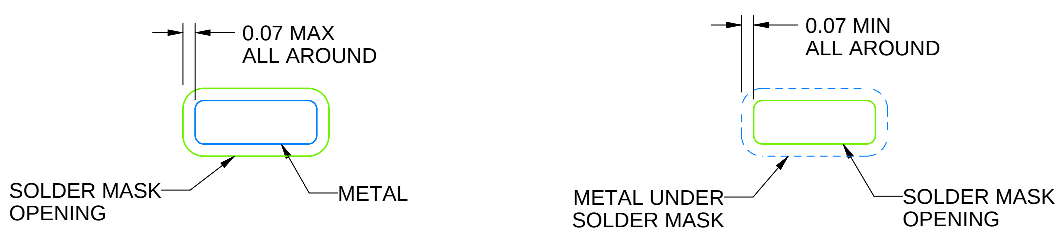
DIMENSION A	
OPTION 01	(0.1)
OPTION 02	(0.2)

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

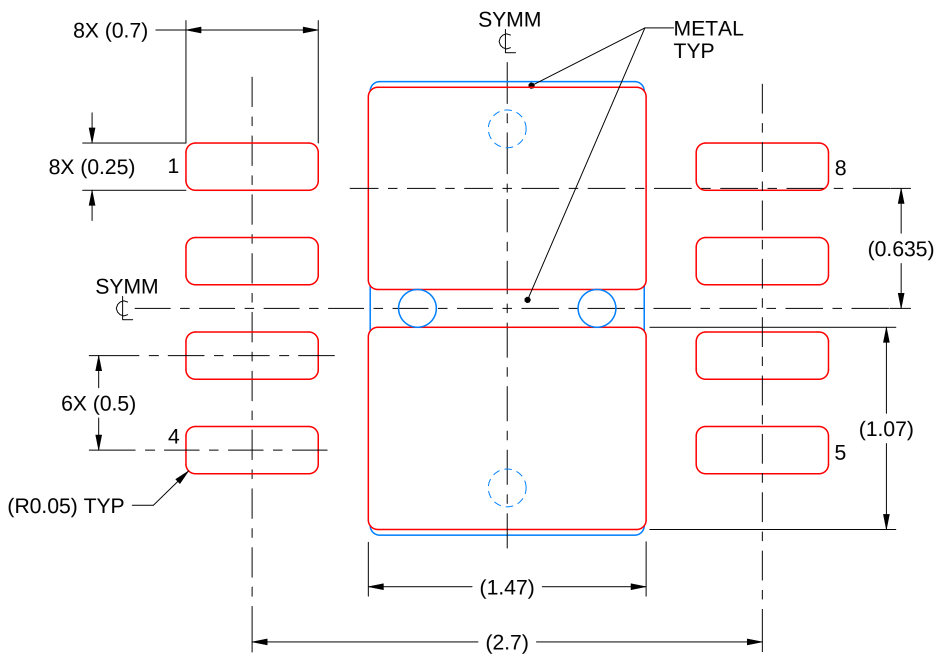
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218886/A 01/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218886/A 01/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER