











SBOS826D - DECEMBER 2017 - REVISED OCTOBER 2019

**OPA207** 

# OPA207 Low-Power, High-Precision, Low-Noise, Rail-to-Rail Output **Operational Amplifier**

## **Features**

Ultra-low offset voltage: 150 µV (maximum)

Ultra-low drift:  $\pm 1 \mu V/^{\circ}C$  (maximum) Gain bandwidth: 1 MHz (typical)

Slew rate: 3.6 V/μs (typical)

High open-loop gain: 130 dB (minimum)

High common-mode rejection: 115 dB (minimum)

High power-supply rejection: 5µV/V (maximum)

Low bias current: 2.8 nA (maximum)

Wide supply range: ±2.25 V to ±18 V

Low quiescent current: 375 μA (maximum)

Replaces OP-07, OP-77, and OP-177

# **Applications**

- Analog input module
- Battery test
- Data acquisition (DAQ)
- Pressure transmitter
- Temperature transmitter

# 3 Description

The OPA207 precision operational amplifier (op amp) replaces the industry standard OP-07, OP-77 and OP-177 amplifiers. The OPA207 offers improved noise, wider output voltage swing, and is twice as fast with half the quiescent current of the industry standard alternatives. Features include ultra-low input offset voltage and drift, low input bias current, high common-mode rejection ratio, and high power-supply rejection ratio.

The OPA207 op amp operates over a wide powersupply-voltage range, from ±2.25 V to ±18 V, with excellent performance. High performance maintained as the amplifiers swing to their specified limits.

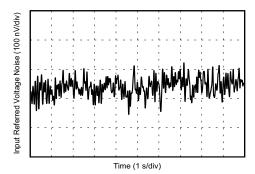
The OPA207 operational amplifier is easy to use and free from phase inversion and the overload problems found in some other operational amplifiers. The OPA207 is stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions.

# Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)		
	SOIC (8)	4.90 mm × 3.91 mm		
OPA207	VSSOP (8)	3.00 mm × 3.00 mm		
	SOT-23 (5)	2.90 mm × 1.60 mm		

(1) For all available packages, see the package option addendum at the end of the data sheet.

#### Ultra-Low 0.1-Hz to 10-Hz Noise





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# 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

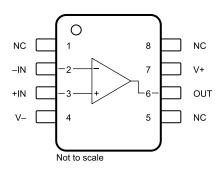
Changes from Revision C (March 2019) to Revision D	Page
Changed SOT-23 (DBV) package from preview to production data (active)	1
Added specifications for new DBV package	4
Changes from Revision B (March 2019) to Revision C	Page
Added input offset voltage specification for OPA207DGK	5
Added input offset voltage drift specification for OPA207DGK	5
Changes from Revision A (December 2018) to Revision B	Page
Added content for first release of production-data data sheet for VSSOP (DGK) package	1
Changes from Original (December 2017) to Revision A	Page
Added content re: 5-pin SOT-23 package for Advance Information	1

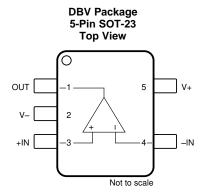
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# 5 Pin Configuration and Functions

D and DGK Packages 8-Pin SOIC and 8-Pin VSSOP **Top View** 





# **Pin Functions**

	PIN				
	N	0.	I/O	DESCRIPTION	
NAME	D (SOIC), DGK(VSSOP)	DBV (SOT-23)	20	DECORN HON	
-IN	2	4	1	Inverting input	
+IN	3	3	1	Non-inverting input	
NC	1, 5, 8	_		No internal connection (can be left floating or connected to ground)	
OUT	6	1	0	Output	
V-	4	2	_	Negative (lowest) power supply	
V+	7	5	_	Positive (highest) power supply	

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# 6 Specifications

#### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage, $Vs = (V+) - (V-)$		36	V
Input voltage - Common-mode (2)	(V-) -0.7	(V+) +0.7	V
Input voltage - Differential	-1	1	V
Output short-circuit <sup>(3)</sup>	Continuous		
Operating temperature	-55	125	°C
Junction temperature		150	°C
Storage temperature, T <sub>stg</sub>	-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# 6.2 ESD Ratings

			VALUE	UNIT
.,	Electrostatio discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	2000	
V <sub>(ESD)</sub> Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	1000	V	

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, $Vs = (V+) - (V-)$	Single Supply	4.5	30	36	V
Supply voltage, $VS = (V+) - (V-)$	Dual Supply	±2.25	±15	0 36 5 ±18	V
Specified temperature		-40		125	°C

#### 6.4 Thermal Information

			OPA207				
	THERMAL METRIC <sup>(1)</sup>	DGK (VSSOP)	D (SOIC)	DBV (SOT-23)	UNIT		
		8 PINS	8 PINS	8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	176.7	121.5	166.3	°C/W		
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.9	64.3	116.9	°C/W		
$R_{\theta JB}$	Junction-to-board thermal resistance	99.4	65.0	63.2	°C/W		
ΨЈТ	Junction-to-top characterization parameter	8.8	18.2	45	°C/W		
ΨЈВ	Junction-to-board characterization parameter	97.6	64.3	62.9	°C/W		

 For more information about traditional and new thermal metrics, see the Semiconductor and IC Package ThermalMetrics application report.

Product Folder Links: OPA207

<sup>(2)</sup> Input current must be limited to 10 mA.

<sup>(3)</sup> Short circuit to ground, one amplifier per package.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



### 6.5 Electrical Characteristics

at  $V_S = \pm 15 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ ,  $R_L = 2 \text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

	$\frac{15 \text{ V, T}_{A} = 25^{\circ}\text{C, R}_{L} = 2 \text{ F}}{\text{PARAMETER}}$		ONDITIONS	MIN	TYP	MAX	UNIT	
OFFSET V	OLTAGE							
					15	±100		
	Input offset voltage OPA207D	$T_A = -40$ °C to 85°C			±150			
		$T_A = -40^{\circ}\text{C} \text{ to } 125^{\circ}\text{C}$				±200		
	land offer to the se				15	±125		
V <sub>OS</sub>	Input offset voltage OPA207DGK	$T_A = 0$ °C to 85°C				±170	μV	
		$T_A = -40^{\circ}\text{C} \text{ to } 125^{\circ}\text{C}$				±225		
	Input offset voltage				15	±130		
	OPA207DBV	$T_A = 0$ °C to 85°C				±170		
		$T_A = -40$ °C to 125°C				±225		
	Input offset voltage drift	$T_A = -40$ °C to 85°C			±0.2	±.8		
dV <sub>OS</sub> /dT	OPA207D	T <sub>A</sub> = -40°C to 125°C			±0.2	±.8	μV/°C	
uvos/ui	Input offset voltage drift OPA207DGK	$T_A = 0$ °C to 85°C			±0.2	±1.1	μ., σ	
	and OPA207DBV	$T_A = -40$ °C to 125°C			±0.2	±1.1		
	lanut offeet veltere versus	$V_S = \pm 2.25 \text{ V to } \pm 18 \text{ V}$			±0.5	±3		
PSRR	Input offset voltage versus power supply	$V_S = \pm 2.25 \text{ V to } \pm 18 \text{ V}, T_A =$				±4.2	$\mu V/V$	
		$V_S = \pm 2.25 \text{ V to } \pm 18 \text{ V}, T_A =$	-40°C to 125°C			±5		
INPUT BIA	AS CURRENT							
					±0.2	±1.5		
I <sub>B</sub>	Input bias current	$T_A = -40$ °C to 85°C			±2	nA		
		$T_A = -40$ °C to 125°C				±7		
					±0.13	±1.5		
I <sub>OS</sub> Input offset current		$T_A = -40^{\circ}\text{C to } 85^{\circ}\text{C}$			±2	nA		
NOISE		$T_A = -40^{\circ}\text{C} \text{ to } 125^{\circ}\text{C}$				±7		
NOISE					0.16		\/	
	Input voltage noise	f = 0.1 Hz to 10 Hz			0.16		μV <sub>PP</sub>	
		f = 1 Hz			9.5		μV <sub>RMS</sub>	
		f = 10 Hz		7.5				
$e_N$	Input voltage noise density	f = 100 Hz		7.5		nV/√ <del>Hz</del>		
		f = 1 kHz		7.5				
i <sub>N</sub>	Input current noise	f = 1 kHz			0.18		pA/√ <del>Hz</del>	
	LTAGE RANGE							
V <sub>CM</sub>	Common-mode voltage range			(V-) + 1.25		(V+) - 1.25	V	
		(V-) + 1.25 V < V <sub>CM</sub> < (V+)	– 1.25 V	120	140			
CMRR	Common-mode rejection ratio	(V-) + 1.25 V < V <sub>CM</sub> < (V+) 125°C		115	140		dB	
INPUT CAI	PACITANCE	1						
Z <sub>ID</sub>	Differential				3    14		MΩ    pF	
Z <sub>ICM</sub>	Common-mode				1    1		GΩ    pF	
OPEN-LOC	OP GAIN							
		(V–) + 200 mV < V <sub>O</sub> <		130	140			
		$(V+) - 200 \text{ mV}, R_L = 10 \text{ k}\Omega$	$T_A = -40$ °C to 125°C	126				
		$(V-) + 200 \text{ mV} < V_O < (V+) - 200 \text{ mV}, R_L = 2 \text{ k}\Omega$	OPA207D, OPA207DGK	120	140			
A <sub>OL</sub>	Open-loop voltage gain	$(V-) + 300 \text{ mV} < V_O < (V+) - 300 \text{ mV}, R_L = 2 \text{ k}\Omega$	OPA207DBV	130	140		dB	
		(V–) + 200 mV < V <sub>O</sub> < (V+) – 200 mV, R <sub>L</sub> = 2 kΩ	$T_A = -40$ °C to 125°C, OPA207D, OPA207DGK	114				
		$(V-) + 300 \text{ mV} < V_O < T_A = -40^{\circ}\text{C to } 125^{\circ}\text{C},$ $(V+) - 300 \text{ mV}, R_L = 2 \text{ k}\Omega$ OPA207DBV		120				

Product Folder Links: OPA207



# **Electrical Characteristics (continued)**

at  $V_S = \pm 15$  V,  $T_A = 25$ °C,  $R_L = 2$  k $\Omega$  connected to  $V_S$  / 2,  $V_{CM} = V_S$  / 2, and  $V_{OUT} = V_S$ /2 (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUE	NCY RESPONSE					
GBW	Gain-bandwidth product			1.3		MHz
SR	Slew rate	10-V step, G = 1			V/μs	
		To 0.1%, 10-V step , G = 1		4.8		
$t_S$	Settling time	To 0.01%, 10-V step , G = 1		5.4		μS
		To 0.001%, 10-V step , G = 1		8.1		
	Overload recovery time	V <sub>IN</sub> × gain > V <sub>S</sub>		1.1		μS
	Total harmonic distortion + noise (THD+N)	$V_{O} = 3 V_{RMS}, G = 1, f = 1 \text{ kHz}, R_{L} = 10 \text{ k}\Omega$		-114		dB
OUTPUT	•					
		T <sub>A</sub> = 25°C, no load, OPA207DBV		15	40	
		$T_A = 25^{\circ}C, R_L = 10 \text{ k}\Omega, OPA207DBV$	40	60		
		$T_A = 25$ °C, $R_L = 2 \text{ k}\Omega$ , OPA207DBV		80	140	
	Voltage output swing from rail	T <sub>A</sub> = 25°C, no load, OPA207D, OPA207DGK		15	30	mV
	Tan	$T_A = 25$ °C, $R_L = 10 \text{ k}\Omega$ , OPA207D, OPA207DGK		40	50	
		$T_A = 25$ °C, $R_L = 2 \text{ k}\Omega$ , OPA207D, OPA207DGK		80	125	
		$T_A = -40$ °C to 125°C, $R_L = 10 \text{ k}\Omega$		75	200	
-	Short-circuit current	Sinking		-40		mA
I <sub>SC</sub>	Short-circuit current	Sourcing		40		mA
$C_{LOAD}$	Capacitive load drive			200		pf
R <sub>O</sub>	Open-loop output impedance	f = 1 MHz 45			Ω	
POWER	SUPPLY				<u>'</u>	
	Quiescent current per	I <sub>O</sub> = 0 A		350	375	^
IQ	amplifier	$I_{O} = 0 \text{ A}, T_{A} = -40^{\circ}\text{C to } 125^{\circ}\text{C}$			450	μΑ
	Turnon time	At $T_A = 25$ °C, $V_S = 36$ V, $V_S$ ramp rate > 0.3 V/ $\mu$ s		27		μS

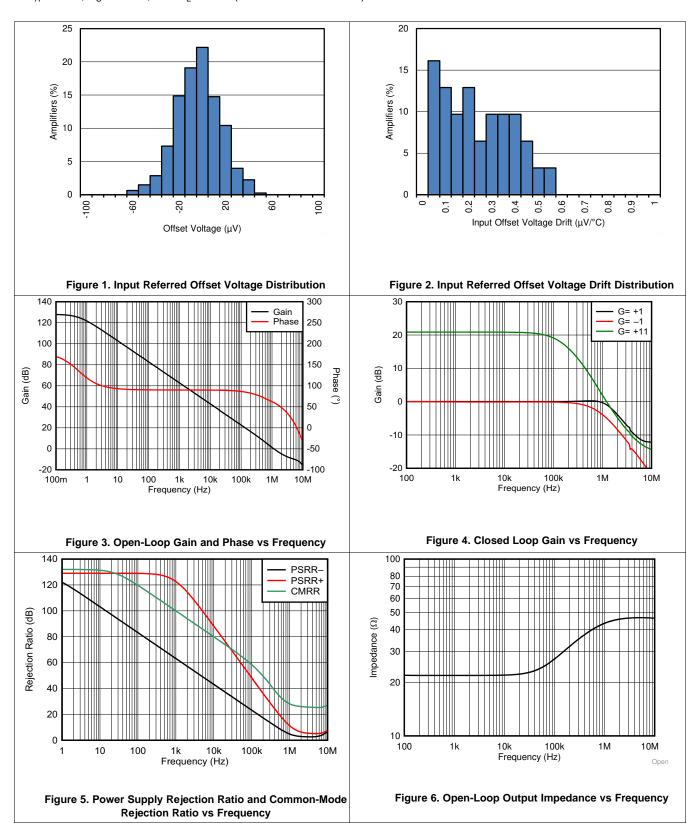
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# 6.6 Typical Characteristics

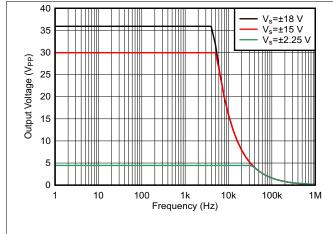
at  $T_A$  = 25°C,  $V_S$  = ±15 V, and  $R_L$  = 2 k $\Omega$  (unless otherwise noted)



# TEXAS INSTRUMENTS

# **Typical Characteristics (continued)**

at  $T_A$  = 25°C,  $V_S$  = ±15 V, and  $R_L$  = 2 k $\Omega$  (unless otherwise noted)



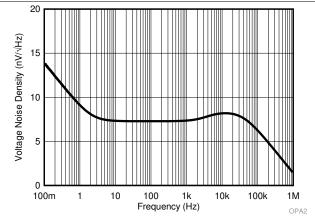
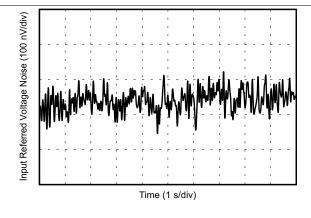


Figure 7. Full Power Bandwidth

Figure 8. Input Voltage Noise Spectral Density vs Frequency



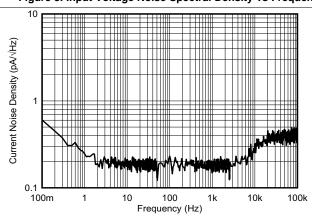
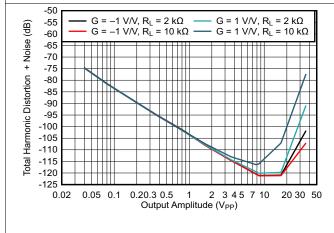


Figure 9. 0.1-Hz to 10-Hz Noise Voltage

Figure 10. Input Current Noise vs Frequency



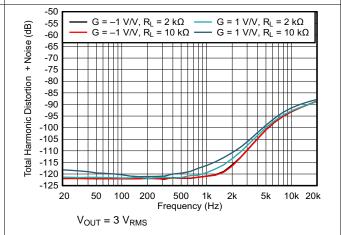


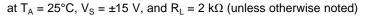
Figure 11. Total Harmonic Distortion + Noise vs Output Amplitude

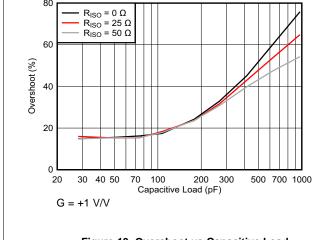
Figure 12. Total Harmonic Distortion + Noise vs Frequency

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# **Typical Characteristics (continued)**

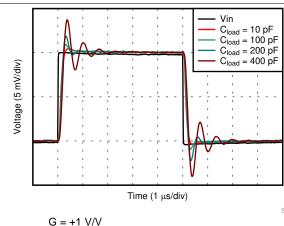




40  $\begin{aligned} R_{ISO} &= 0 \ \Omega \\ R_{ISO} &= 25 \ \Omega \\ R_{ISO} &= 50 \ \Omega \end{aligned}$ 35 30 Overshoot (%) 25 20 15 10 5 30 40 50 300 500 700 1000 20 100 Capacitive Load (pF) G = -1 V/V

Figure 13. Overshoot vs Capacitive Load

Figure 14. Overshoot vs Capacitive Load



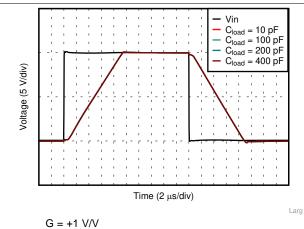


Figure 16. Large-Signal Step Response

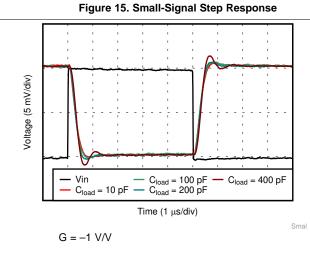


Figure 17. Small-Signal Step Response

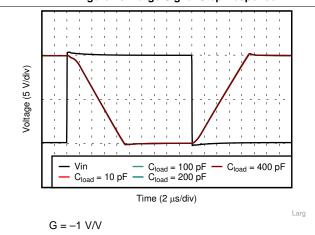
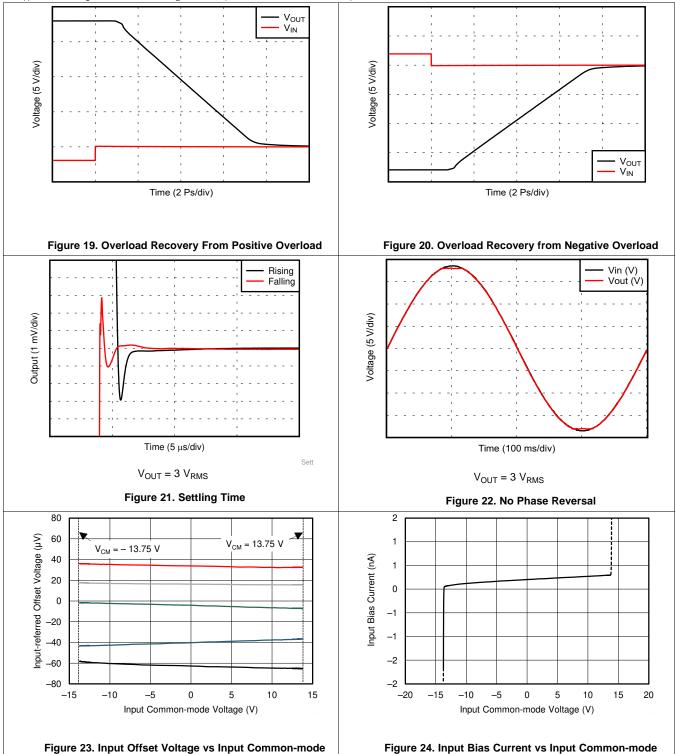


Figure 18. Large-Signal Step Response

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# **Typical Characteristics (continued)**

at  $T_A$  = 25°C,  $V_S$  = ±15 V, and  $R_L$  = 2 k $\Omega$  (unless otherwise noted)



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Voltage

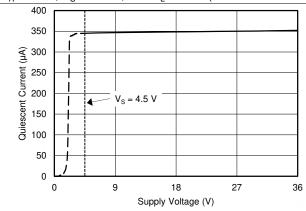
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Voltage



# **Typical Characteristics (continued)**

at  $T_A$  = 25°C,  $V_S$  = ±15 V, and  $R_L$  = 2 k $\Omega$  (unless otherwise noted)



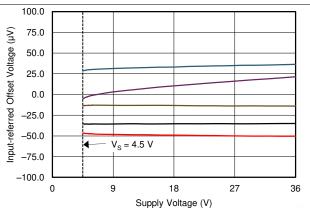
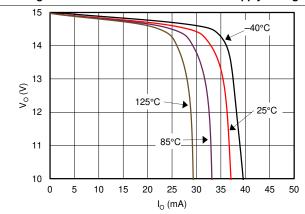


Figure 25. Quiescent Current vs Power Supply Voltage

Figure 26. Input Offset Voltage vs Power Supply Voltage



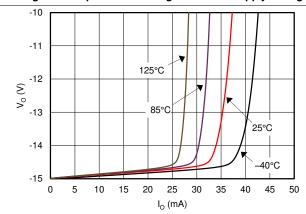
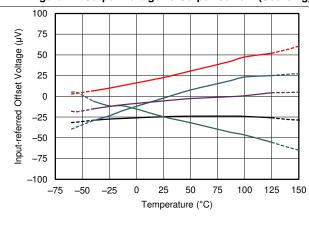


Figure 27. Output Voltage vs Output Current (Sourcing)

Figure 28. Output Voltage vs Output Current (Sinking)



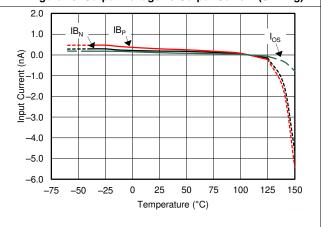


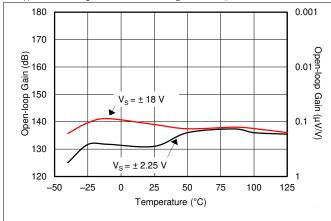
Figure 29. Input Offset Voltage vs Temperature

Figure 30. Input Bias Current vs Temperature

# **ISTRUMENTS**

# **Typical Characteristics (continued)**

at  $T_A$  = 25°C,  $V_S$  = ±15 V, and  $R_L$  = 2 k $\Omega$  (unless otherwise noted)



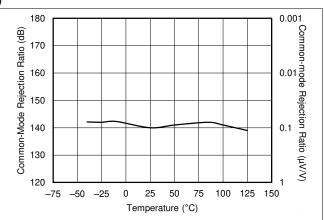
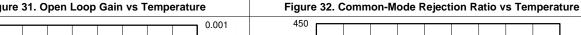
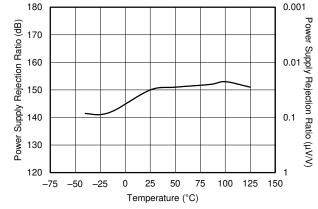


Figure 31. Open Loop Gain vs Temperature





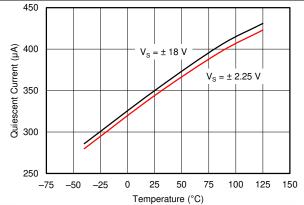


Figure 33. Power Supply Rejection Ratio vs Temperature

Figure 34. Quiescent Current vs Temperature

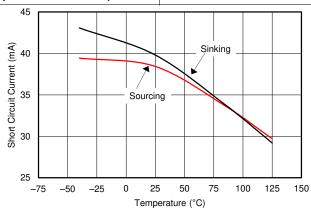


Figure 35. Output Short Circuit Current vs Temperature

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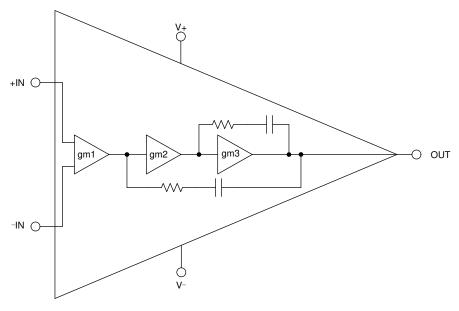


# **Detailed Description**

#### Overview

The OPA207 precision operational amplifier replaces the industry standard OP-177. The OPA207 offers improved noise, wider output voltage swing, has twice the bandwidth, ten times the slew rate and consumes only half the quiescent current as the OP-177. Additional features include ultralow offset voltage and drift, low bias current, high common-mode rejection, and high power supply rejection.

#### 7.2 Functional Block Diagram



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#### 7.3 Feature Description

The OPA207 is unity-gain stable and free from unexpected output phase reversal, making it easy to use in a wide range of applications. Applications with noisy or high-impedance power supplies may require decoupling capacitors close to the device pins. In most cases 0.1-μF capacitors are adequate.

#### 7.3.1 Operating Voltage

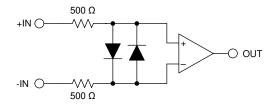
The OPA207 operates from ±2.25 V to ±18 V supplies with excellent performance. Key parameters are assured over the specified temperature range, -40°C to 125°C. Most behavior remains unchanged through the full operating voltage range (±2.25 V to ±18 V). Parameters which vary significantly with operating voltage or temperature are shown in *Typical Characteristics*.

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#### 7.3.2 Input Protection

The input stage of the OPA207 is internally protected with resistors in series with diode clamps as shown in Figure 36. The inputs can withstand ±10 V differential inputs without damage and the maximum input current should be limited to 10 mA or less.. The protection diodes conduct current when the inputs are over-driven such as when the opamp output is slewing. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the operational amplifier.

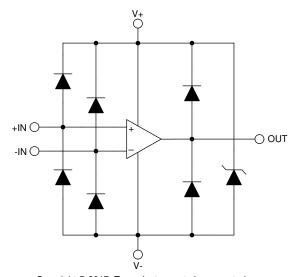


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Figure 36. Simplified OPA207 Input Protection Circuit

#### 7.3.3 ESD Protection

The OPA207 is internally protected against ESD events that can occur during manufacturing, handling, or printed-circuit-board assembly. The internal ESD protection diodes are not intended to protect the OPA207 during normal operation when the device is operating under power. In cases where the inputs or output can be driven above the positive power supply or below the negative power supply care must be taken to limit the current through the internal diodes to 10 mA or less. In harsh electrical environments external protection circuitry may be required and is dependant upon the application requirements and environmental conditions.



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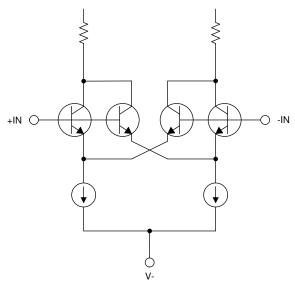
Figure 37. Simplified OPA207 ESD Protection Circuit

Product Folder Links: OPA207



# 7.3.4 Input Stage Linearization

The OPA207 uses linearization techniques to reduce the total harmonic distortion. Figure 38 illustrates the linearization concept, and Figure 38 illustrates the total harmonic distortion performance of the OPA207.



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Figure 38. Simplified Input Stage Linearization Circuit

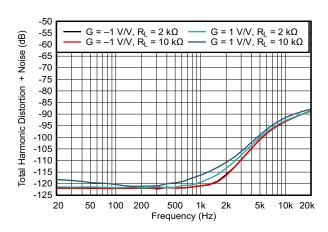


Figure 39. Total Harmonic Distortion

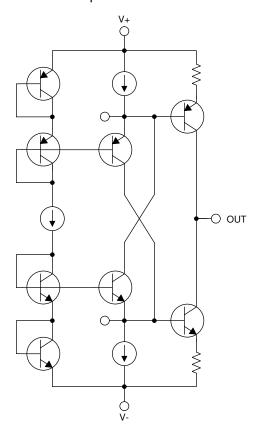
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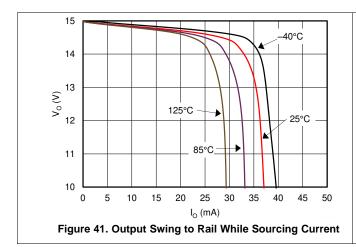
## 7.3.5 Rail-to-Rail Output

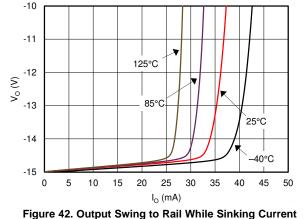
The OPA207 uses a rail-to-rail output stage capable of swinging within a few millivolts from either power supply rail while maintaining high open-loop gain. Figure 40 shows a simplified drawing of the output stage circuit. Resistors connected in series with each output transistor ensure a consistent output current limit. Limiting the output current in this way ensures reliable operation of the OPA207 under short circuited conditions and protects sensitive loads from being damaged by excessive current. Figure 41 and Figure 42 illustrate the maximum output current available from the OPA207 at various temperatures.



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Figure 40. Simplified Rail-to-Rail Output Stage Circuit





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#### 7.3.6 Low Input Bias Current

The OPA207 uses super-beta bipolar transistors and employs an input bias current cancellation technique. This combination results in very low input bias currents that remain low over the full specified temperature range from –40°C to + 125°C unlike CMOS or JFET amplifiers whose input bias currents typically double every 10°C and can be extremely high at 125°C. Figure 43 illustrates the comparison between the OPA207 and typical CMOS or JFET amplifiers.

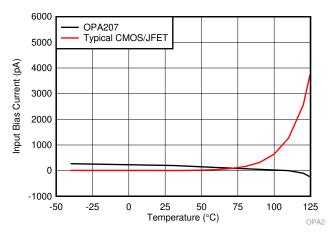
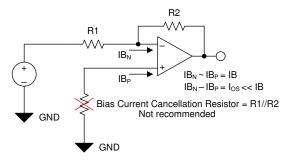


Figure 43. Input Bias Current vs Temperature

It is common practice to place a bias current cancellation resistor as illustrated in Figure 42. This approach works well with amplifiers that do not employ an internal input bias current cancellation technique. Because the OPA207 uses an internal bias current cancellation technique, TI does not recommend the bias cancellation resistor.



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Figure 44. Bias Current Cancellation Resistor — Not Recommended

Product Folder Links: OPA207



#### 7.3.7 Slew Boost

The OPA207 uses a novel internal slew-boost technique. This method allows the OPA207 to consume very low power yet still achieve a high slew rate of 3.6 V/µs. This makes the OPA207 ideal for applications that require low noise and high out voltage swings where the high slew rate is necessary to achieve fast settling times.

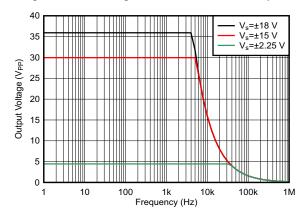


Figure 45. Full Power Bandwidth

### 7.3.8 EMI Rejection Ratio (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this report provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- 1. Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- 2. The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
- 3. EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a printed circuit board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

A more formal discussion of the EMIRR IN+ definition and test method is provided in TI Application Report *EMI Rejection Ratio of Operational Amplifiers*, available for download at www.ti.com. The EMIRR IN+ of the OPA207 is plotted versus frequency as shown in Figure 46.

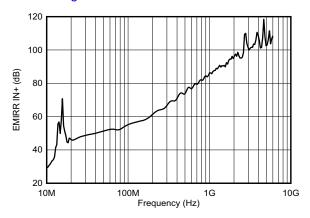


Figure 46. OPA207 EMIRR IN+ vs Frequency

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If available, any dual and quad operational amplifier device versions have nearly similar EMIRR IN+ performance. The OPA207 unity-gain bandwidth is 1 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.

Table 1 shows the EMIRR IN+ values for the OPA207 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 1 may be centered on or operated near the particular frequency shown. This information may be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

Table 1. OPA207 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION/ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite/space operation, weather, radar, UHF	72 dB
900 MHz	GSM, radio com/nav./GPS (to 1.6 GHz), ISM, aeronautical mobile, UHF	83 dB
1.8 GHz	GSM, mobile personal comm. broadband, satellite, L-band	95 dB
2.4 GHz	802.11b/g/n, Bluetooth <sup>®</sup> , mobile personal comm., ISM, amateur radio/satellite, S-band	94 dB
3.6 GHz	Radiolocation, aero comm./nav., satellite, mobile, S-band	103 dB
5 GHz	802.11a/n, aero comm./nav., mobile comm., space/satellite operation, C-band	102 dB

#### 7.4 Device Functional Modes

The OPA207 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V ( $\pm$  2.25 V). The maximum power supply voltage for the OPA207 is 36 V ( $\pm$ 18 V).

Product Folder Links: OPA207



# 8 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

# 8.1 Application Information

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA207 is designed to construct high-precision active filters. Figure 47 shows a second-order, low-pass filter commonly encountered in signal processing applications.

# 8.2 Typical Applications

#### 8.2.1 Typical OPA207 Application

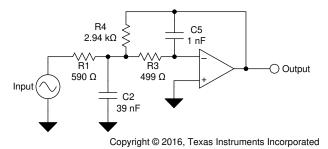


Figure 47. Typical OPA207 Application Schematic

#### 8.2.1.1 Design Requirements

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

#### 8.2.1.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 47. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1 R_3 C_2 C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3 R_4 C_2 C_5}$$
(1)

This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by Equation 2:

Gain = 
$$\frac{R_4}{R_1}$$
  
 $f_c = \frac{1}{2\pi} \sqrt{(1/R_3 R_4 C_2 C_5)}$  (2)

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets designers create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows to design, optimize, and simulate complete multi-stage active filter solutions within minutes.

Product Folder Links: OPA207



# **Typical Applications (continued)**

# 8.2.1.3 Application Curve

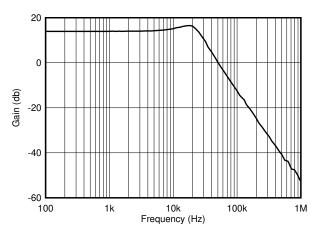
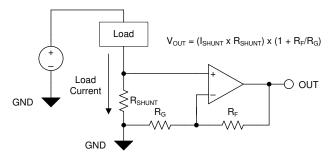


Figure 48. Low-Pass Filter Transfer Function

# 8.2.2 Precision Low-Side Current Sensing

With low offset voltage and low offset voltage drift over time and temperature the OPA207 works well for precision low-side current sensing applications as shown in Figure 49



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Figure 49. Precision Low-Side Current Sensing

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# **Typical Applications (continued)**

#### 8.2.3 Precision Buffer With Increased Output Current

The OPA207 can be configured as illustrated in Figure 50 to drive low impedance loads. In Figure 50, the OPA207 is configured in a gain of +10 V/V, and the output current is boosted by the NPN (2N2904) and PNP (2N2906) bipolar transistors. For low output voltages the OPA207 supplies the load current directly through the  $100-\Omega$  resistor. The bipolar transistors begin to supply current when the voltage drop across the  $100-\Omega$  resistor exceeds approximately 500 mV. Figure 50 illustrates the results for a  $50-\Omega$  load resistor driven with a 10-V step at the output. This results in a 200-mA current supplied by the circuit.

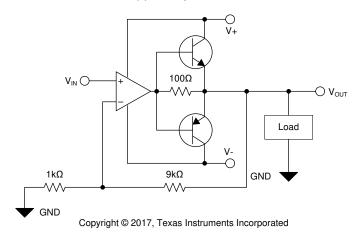


Figure 50. Precision Buffer (G = 10 V/V) With High Output Drive Capability

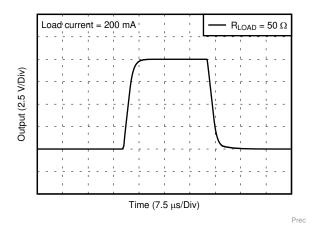


Figure 51. 50- $\Omega$  Load Driven With a 10-V Step

22 Submit D



# 9 Power Supply Recommendations

The OPA207 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

#### **CAUTION**

Supply voltages larger than 36 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines*.

# 10 Layout

## 10.1 Layout Guidelines

The OPA207 series has low offset voltage and drift. To achieve highest performance, optimize the circuit layout and mechanical conditions. Offset voltage and drift can be degraded by small thermoelectric potentials at the op amp inputs. Connections of dissimilar metals generate thermal potential, which can degrade the ultimate performance of the OPA207. These thermal potentials can be made to cancel by assuring that they are equal in both input terminals.

- Keep the thermal mass of the connections to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

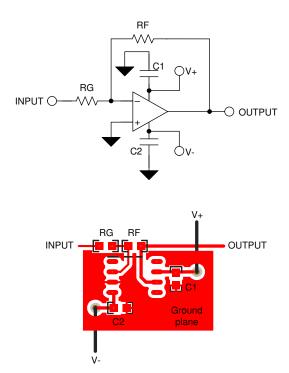
For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself.
   Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for singlesupply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective
  methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes.
  A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital
  and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as
  possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as
  opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As shown in Layout Example, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, TI recommends cleaning the PCB following board assembly.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, postcleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

Product Folder Links: OPA207



# 10.2 Layout Example



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Figure 52. OPA207 Layout Example for the Inverting Configuration

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# 11 Device and Documentation Support

# 11.1 Device Support

#### 11.1.1 Development Support

#### 11.1.1.1 Webench Filter Designer Tool

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

### 11.1.1.2 TINA-TI™ (Free Software Download)

TINA<sup>TM</sup> is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

#### NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

## 11.1.1.3 TI Precision Designs

The OPA207 is featured in several TI Precision Designs, available online at <a href="http://www.ti.com/ww/en/analog/precision-designs/">http://www.ti.com/ww/en/analog/precision-designs/</a>. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

#### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, EMI Rejection Ratio of Operational Amplifiers
- · Texas Instruments, Circuit Board Layout Techniques

# 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

Product Folder Links: OPA207



#### 11.5 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments. Bluetooth is a registered trademark of Bluetooth SIG, Inc.. TINA, DesignSoft are trademarks of DesignSoft, Inc. All other trademarks are the property of their respective owners.

## 11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *OPA207* 

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
OPA207ID	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA207
OPA207ID.B	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA207
OPA207IDBVR	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1NBW
OPA207IDBVR.B	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1NBW
OPA207IDBVT	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1NBW
OPA207IDBVT.B	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1NBW
OPA207IDGKR	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAUAG   SN	Level-2-260C-1 YEAR	-40 to 125	117Q
OPA207IDGKR.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	117Q
OPA207IDGKT	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAUAG   SN	Level-2-260C-1 YEAR	-40 to 125	117Q
OPA207IDGKT.B	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	117Q
OPA207IDR	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA207
OPA207IDR.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA207

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# **PACKAGE OPTION ADDENDUM**

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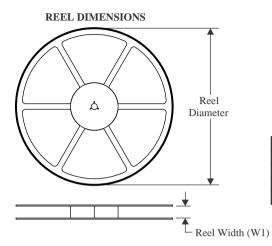
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# **PACKAGE MATERIALS INFORMATION**

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# TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA207IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA207IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA207IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA207IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA207IDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1



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#### \*All dimensions are nominal

7 III GIII I GII I GII GII GII GII GII G							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA207IDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA207IDBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA207IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA207IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA207IDR	SOIC	D	8	2500	353.0	353.0	32.0

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 23-May-2025

# **TUBE**



#### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA207ID	D	SOIC	8	75	507	8	3940	4.32
OPA207ID.B	D	SOIC	8	75	507	8	3940	4.32



SMALL OUTLINE INTEGRATED CIRCUIT



# NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE TRANSISTOR



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE PACKAGE



#### NOTES:

PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-187.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
- 9. Size of metal pad may vary due to creepage requirement.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.



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