www.ti.com

250-MHz, CMOS Transimpedance Amplifier (TIA) with Integrated Switch and Buffer

Check for Samples: OPA1S2384, OPA1S2385

FEATURES

Wide Bandwidth: 250 MHz
 High Slew Rate: 150 V/µs
 Rail-to-Rail Input/Output (I/O)

Fast Settling

Low Input Bias Current: 3 pA

High Input Impedance: 10¹³ Ω || 2 pF

SPST Switch:

Low On-Resistance: 4 Ω
Low Charge Injection: 1 pC
Low Leakage Current: 10 pA

Flexible Configuration:

- Transimpedance Gain

External Hold Capacitor

Post-Gain

• Single Supply: +2.7 V to +5.5 V

Quiescent Current: 9.2 mA

Small Package: 3-mm x 3-mm SON-10
 OPA1S2384: Internal Switch Active High
 OPA1S2385: Internal Switch Active Low

APPLICATIONS

Communications:

- Optical Networking: EPON, GPON

Signal Strength Monitors

Burst-Mode RSSI

Photodiode Monitoring

Fast Sample-and-Hold Circuits

Charge Amplifiers

High-Speed Integrators

DESCRIPTION

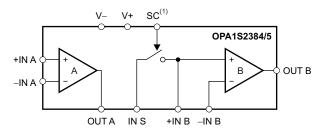
The OPA1S2384 and OPA1S2385 (OPA1S238x) combine high bandwidth, FET-input operational amplifiers with a fast SPST CMOS switch designed for applications that require the tracking and capturing of fast signals.

By providing a 250-MHz gain bandwidth product and rail-to-rail input/output swings in single-supply operation, the OPA1S238x is capable of wideband transimpedance gain and large output signal swing simultaneously. Low input bias current and voltage noise (6 nV/\delta Hz) make it possible to amplify extremely low-level input signals for maximum signal-to-noise ratio.

The characteristics of the OPA1S238x make this device ideally suited for use as a wideband photodiode amplifier.

In addition, the CMOS switch and subsequent buffer amplifier allow the OPA1S238x to be easily configured as a fast sample-and-hold circuit. The external hold capacitor and post-gain options make the OPA1S238x easily adaptable to a wide range of speed and accuracy requirements. Note that the OPA1S2384 closes the internal switch with a logic-high signal, and the OPA1S2385 closes the internal switch with a logic-low signal.

The OPA1S238x are optimized for low-voltage operation from as low as +2.7 V up to +5.5 V. These devices are specified for a temperature range of -40°C to +85°C.



 The OPA1S2384 internal switch is active high; the OPA1S2384 internal switch is active low.

M

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER
OPA1S2384	SON-10	DRC	-40°C to +85°C	OVAQ	OPA1S2384IDRCT
OFA132304	SON-10	DRC	-40 C to +65 C	OVAQ	OPA1S2384IDRCR
OPA1S2385	SON-10	DRC	-40°C to +85°C	OUZQ	OPA1S2385IDRCT
UPA152365	SON-10	DRC	-40°C 10 +65°C	002Q	OPA1S2385IDRCR

⁽¹⁾ For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		OPA1S238x	UNIT	
Supply voltage, V+ to V-		6	V V mA mA V mA °C	
Signal input terminals, op amp	Voltage ⁽²⁾	(V-) - 0.3 to (V+) + 0.3	V	
section	Current ⁽²⁾	±10	mA	
On-state switch current; V _{IN S} , V _{+IN B} = 0 to V+		±20	mA	
Output (OUT A, OUT B) short-cir	cuit current ⁽³⁾	Continuous		
Digital input voltage range (SC pi	in)	-0.3 to +6	V	
Digital input clamp current (SC pi	in)	-50	mA	
Operating temperature, T _A		-40 to +125	°C	
Storage temperature, T _{stg}		-65 to +150	°C	
Junction temperature, T _J		+150	°C	
Electrostatic discharge (ESD)	Human body model (HBM)	4000	V	
ratings	Charged-device model (CDM)	1000	V	

⁽¹⁾ Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(3) Short-circuit to ground, one amplifier per package.

⁽²⁾ Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.



ELECTRICAL CHARACTERISTICS: Amplifier Section, $V_{SS} = +2.7 \text{ V to } +5.5 \text{ V}^{(1)(2)}$

			OPA1S238x			
	PARAMETER	CONDITIONS	CONDITIONS MIN			
OFFSET \	/OLTAGE					
Vos	Input offset voltage			2	8	mV
$\Delta V_{OS}/\Delta T$	Input offset voltage vs temperature	$T_A = -40$ °C to +85°C		6		μV/°C
PSRR	Input offset voltage vs power supply	$V_{CM} = (V_S / 2) - 0.65 V$		0.2	0.8	mV/V
	Channel separation	f = 5 MHz		33		μV/V
INPUT VO	LTAGE RANGE					
V _{CM}	Common-mode voltage range	No phase reversal, rail-to-rail input	(V-) - 0.1	((V+) + 0.1	V
CMDD	Common mode valention votice	$V_S = 5.5 \text{ V}, (V-) - 0.1 \text{ V} < V_{CM} < (V+) - 2 \text{ V}$	66	80		dB
CMRR	Common-mode rejection ratio	$V_S = 3.3 \text{ V}, (V-) - 0.1 \text{ V} < V_{CM} < (V+) + 0.1 \text{ V}$	50	68		dB
INPUT BIA	AS CURRENT					
I _B	Input bias current			±3	±50	pA
Ios	Input offset current			±1	±50	pA
NOISE						
	Innut major valtage density	f = 1 MHz		6		nV/√ Hz
	Input noise voltage density	f = 10 MHz		26		nV/√ Hz
	Input current noise density	f = 1 MHz		50		fA/√ Hz
INPUT CA	PACITANCE					
	Differential			2		pF
	Common-mode			2		pF
OPEN-LO	OP GAIN					
		$V_S = 2.7 \text{ V}, 0.3 \text{ V} < V_O < (V+) - 0.3 \text{ V}, R_L = 1 \text{ k}\Omega$	88	100		dB
A _{OL}	Open-loop voltage gain	$V_S = 5.5 \text{ V}, 0.3 \text{ V} < V_O < (V+) - 0.3 \text{ V}, R_L = 1 \text{ k}\Omega$	90	110		dB
, OL	Open loop voltage gain	$T_A = -40$ °C to +85°C $V_S = 5.5$ V, 0.3 V < V_O < (V+) - 0.3 V, $R_L = 1$ k Ω	84			dB
FREQUEN	ICY RESPONSE					
	Online to an advaidable and advanta	$V_S = 3.3 \text{ V}, R_L = 1 \text{ k}\Omega, C_L = 10 \text{ pF}, G = 10$		90		MHz
	Gain bandwidth product	$V_S = 5.0 \text{ V}, R_L = 1 \text{ k}\Omega, C_L = 10 \text{ pF}, G = 10$		100		MHz
	One all aire all beauthoridab	$V_S = 5.0 \text{ V}, \text{ G} = 1, V_O = 0.1 \text{ V}_{PP}, R_F = 25 \Omega$		250		MHz
	Small-signal bandwidth	$V_S = 5.0 \text{ V}, \text{ G} = 2, V_O = 0.1 \text{ V}_{PP}, R_F = 25 \Omega$		90		MHz
		V _S = 3.3 V, G = 1, 2-V step		110		V/µs
SR	Slew rate	V _S = 5 V, G = 1, 2-V step		130		V/µs
		V _S = 5 V, G = 1, 4-V step	150			V/µs
t _r	Rise time	V _S = 5 V, G = 1, V _O = 2 V _{PP} , 10% to 90%		11		ns
t _f	Fall time	V _S = 5 V, G = 1, V _O = 2 V _{PP} , 90% to 10%		11		ns
	Cattling time	To 0.1%, V _S = 3.3 V, G = 1, 2-V step		30		ns
t _s	Settling time	To 0.01%, V _S = 3.3 V, G = 1, 2-V step		60		ns
	Overload recovery time	$V_S = 3.3 \text{ V}, V_{IN} \times \text{gain} = V_S$		5		ns
OUTPUT						
	Voltage output swing from supply rails	$V_{S} = 5.5 \text{ V}, R_{L} = 1 \text{ k}\Omega$		100		mV
	01	V _S = 5.0 V		100		mA
	Short-circuit current	V _S = 3.3 V		50		mA
	Closed-loop output impedance			0.05		Ω
	Open-loop output impedance			35		Ω

⁽¹⁾ Parameters with MIN and MAX specification limits are 100% production tested at +25°C, unless otherwise noted. Over temperature limits are based on characterization and statistical analysis.

⁽²⁾ Specified by design and/or characterization; not production tested.



ELECTRICAL CHARACTERISTICS: Amplifier Section, $V_{SS} = +2.7 \text{ V}$ to +5.5 $V^{(1)(2)}$ (continued)

At $T_A = +25$ °C, $R_L = 1$ k Ω connected to V_S / 2, and $V_O = V_{CM} = V_S$ / 2, unless otherwise noted.

			OPA1S238x		
	PARAMETER	CONDITIONS	MIN	TYP MAX	UNIT
POWE	R SUPPLY				
Vs	Operating supply range		2.7	5.5	V
IQ	Quiescent current (per amplifier)	V _S = 5.5 V, I _O = 0 mA		9.2 12	mA
TEMPE	RATURE				
	Specified range		-40	+85	°C
	Operating range		-40	+125	°C
	Storage range		-65	+150	°C

ELECTRICAL CHARACTERISTICS: Switch Section⁽¹⁾

At $T_A = +25$ °C and $V_S = 3.3$ V, unless otherwise noted.

			OF	OPA1S238x			
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	
DC					,		
	Analog voltage range	V _S = 2.7 V to 5.5 V	0		V+	V	
R _{on}	On-state resistance	$V_{IN} = V + / 2$, $I_{COM} = 10 \text{ mA}$		4	16	Ω	
I _{lkg}	Off-state leakage current	$V_{IN} = V + / 2$, $V_{+IN B} = 0 V$	-0.5	0.01	0.5	nA	
DYNAMI	C						
t _{ON}	Turn-on time	V_{IN} = V+ / 2, C_L = 35 pF, R_L = 300 Ω		20		ns	
t _{OFF}	Turn-off time	$V_{IN} = V + / 2$, $C_L = 35$ pF, $R_L = 300 \Omega$		15		ns	
Q_C	Charge injection	$C_L = 1 \text{ nF}, V_{BIAS} = 4 \text{ V}$		1		рС	
BW	Bandwidth	Signal = 0 dBm (0.632 mV _{PP} , 50 Ω)		450		MHz	
	Off isolation	$f = 1$ MHz, signal = 1 Vrms, 50 Ω		-82		dB	
	Off capacitance (IN_S)	Switch open, f = 1 MHz, V _{BIAS} = 0 V		6.5		pF	
	Off capacitance (+IN_B)	Switch open, f = 1 MHz, V _{BIAS} = 0 V		8.5		pF	
	On capacitance (IN_S)	Switch closed, f = 1 MHz, V _{BIAS} = 0 V		13		pF	
	On capacitance (+IN_B)	Switch closed, f = 1 MHz, V _{BIAS} = 0 V		15		pF	
DIGITAL	. CONTROL INPUT (SC pin)						
	High lavel in motor life an	$V_S = 5.5 \text{ V}, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	2.4		V _{S+}	V	
V_{IH}	High-level input voltage	$V_S = 3.3 \text{ V}, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	2.0		V _{S+}	V	
V _{IL}	Low-level input voltage		0		0.9	V	
	Innut looke as augrent	V _{IN S} = V+ or 0 V	-0.5	0.01	0.5	μΑ	
I _{lkg(SC)}	Input leakage current	$T_A = -40$ °C to +85°C	-5		5	μΑ	
	Input capacitance			3		pF	

⁽¹⁾ Parameters with MIN and MAX specification limits are 100% production tested at +25°C, unless otherwise noted. Over temperature limits are based on characterization and statistical analysis.

THERMAI INFORMATION

		OPA1S238x	
	THERMAL METRIC ⁽¹⁾	DRC (SON)	UNITS
		10 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	46.2	
θ_{JCtop}	Junction-to-case (top) thermal resistance	53.8	
θ_{JB}	Junction-to-board thermal resistance	21.7	00044
ΨЈΤ	Junction-to-top characterization parameter	1.1	°C/W
ΨЈВ	Junction-to-board characterization parameter	21.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	6.1	

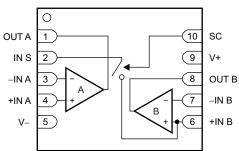
(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

Submit Documentation Feedback



PIN CONFIGURATION

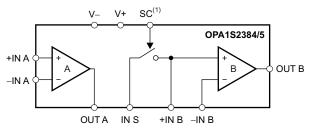
DRC PACKAGE DFN-10 (TOP VIEW)



PIN DESCRIPTIONS

PI	N	
NAME	NO.	DESCRIPTION
+IN A	4	Noninverting input of amplifier channel A
–IN A	3	Inverting input of amplifier channel A
+IN B	6	Noninverting input of amplifier channel B
–IN B	7	Inverting input of amplifier channel B
IN S	2	Switch input
OUT A	1	Voltage output of amplifier channel A
OUT B	8	Voltage output of amplifier channel B
SC	10	Switch control pin. This logic input pin controls the SPST switch operation. For the OPA1S2384, a logic-low signal opens the switch and a logic-high signal closes the switch. For the OPA1S2385, a logic-low signal closes the switch and a logic high signal opens the switch.
V+	9	Positive supply voltage pin. Connect this pin to a voltage +2.7V to +5.5V.
V-	5	Negative supply voltage pin. Connect this pin to the ground (0 V) rail of the single-supply system power supply.

FUNCTIONAL BLOCK DIAGRAM



(1) The OPA1S2384 internal switch is active high; the OPA1S2385 internal switch is active low.



TYPICAL CHARACTERISTICS

Table 1. Characteristic Performance Measurements

TITLE	FIGURE
Offset Voltage Production Distribution	Figure 1
Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency	Figure 2
Input Bias Current vs Temperature	Figure 3
Input Voltage and Current Noise Spectral Density vs Frequency	Figure 4
Open-Loop Gain and Phase	Figure 5
Noninverting Small-Signal Frequency Response	Figure 6
Inverting Small-Signal Frequency Response	Figure 7
Noninverting Small-Signal Step Response	Figure 8
Noninverting Large-Signal Step Response	Figure 9
Frequency Response for Various R _L	Figure 10
Frequency Response for Various C _L	Figure 11
Recommended R _S vs Capacitive Load	Figure 12
Output Voltage Swing vs Output Current	Figure 13
OPEN-Loop Gain vs Temperature	Figure 14
Closed-Loop Output Impedance vs Frequency	Figure 15
Maximum Output Voltage vs Frequency	Figure 16
Output Settling Time to 0.1%	Figure 17
Supply Current vs Temperature	Figure 18
R _{ON} vs Temperature	Figure 19
R _{ON} vs V _{COM}	Figure 20
Leakage Current vs Temperature	Figure 21
Charge-Injection (Q _C) vs V _{COM}	Figure 22
t _{ON} and t _{OFF} vs Supply Voltage	Figure 23
t _{ON} and t _{OFF} vs Temperature (V+ = 5 V)	Figure 24
Gain vs Frequency	Figure 25
Off Isolation vs Frequency	Figure 26



TYPICAL CHARACTERISTICS

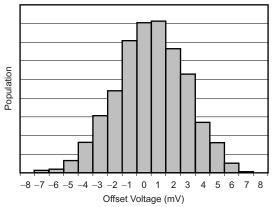


Figure 1. OFFSET VOLTAGE PRODUCTION DISTRIBUTION

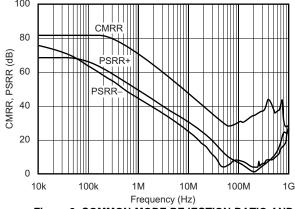


Figure 2. COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION RATIO vs FREQUENCY

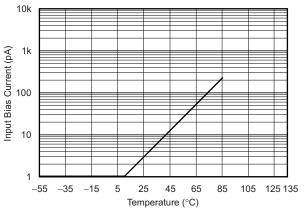


Figure 3. INPUT BIAS CURRENT vs TEMPERATURE

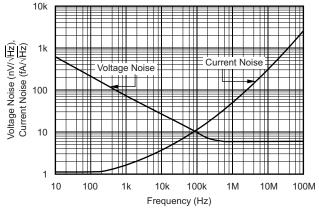


Figure 4. INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY

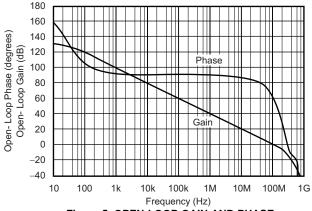


Figure 5. OPEN-LOOP GAIN AND PHASE

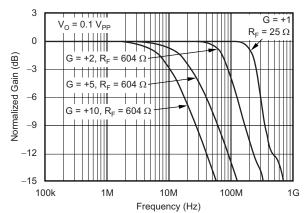


Figure 6. NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



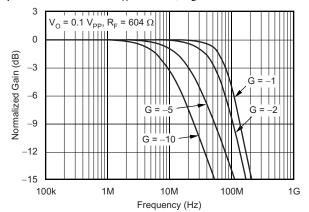


Figure 7. INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

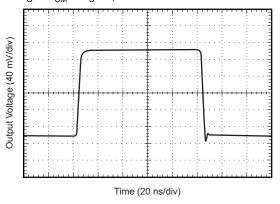


Figure 8. NONINVERTING SMALL-SIGNAL STEP RESPONSE

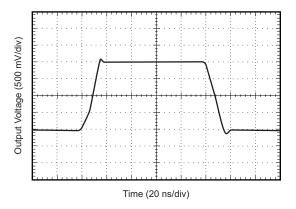


Figure 9. NONINVERTING LARGE-SIGNAL STEP RESPONSE

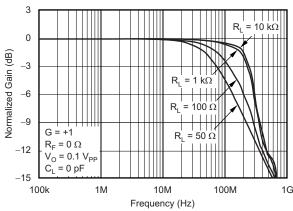


Figure 10. FREQUENCY RESPONSE FOR VARIOUS RL

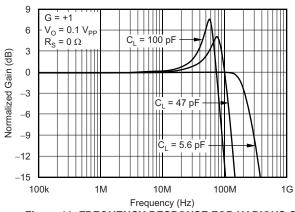


Figure 11. FREQUENCY RESPONSE FOR VARIOUS C_{L}

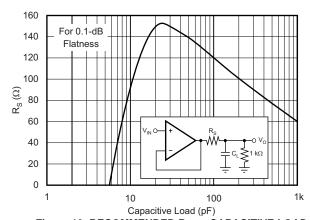


Figure 12. RECOMMENDED R_S vs CAPACITIVE LOAD



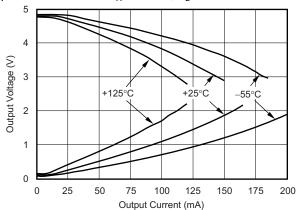


Figure 13. OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

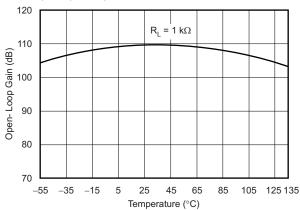


Figure 14. OPEN-LOOP GAIN vs TEMPERATURE

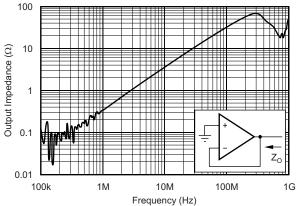


Figure 15. CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

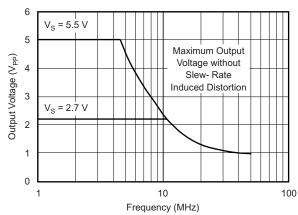


Figure 16. MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

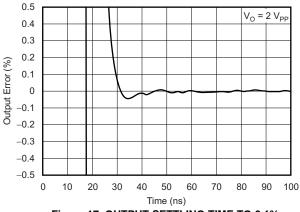


Figure 17. OUTPUT SETTLING TIME TO 0.1%

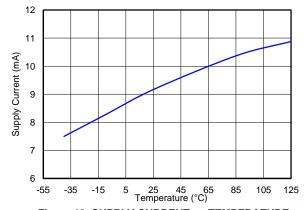


Figure 18. SUPPLY CURRENT vs TEMPERATURE (Vs = 5.5 V, I_O = 0 mA)



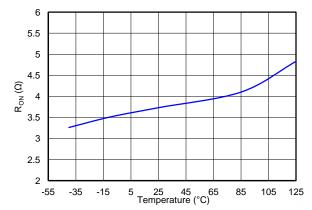


Figure 19. Ron vs TEMPERATURE

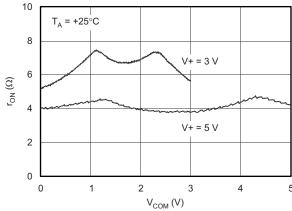


Figure 20. Ron vs V_{COM}

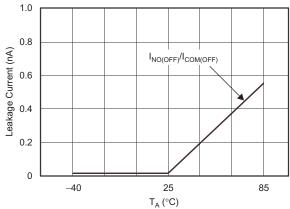


Figure 21. LEAKAGE CURRENT vs TEMPERATURE

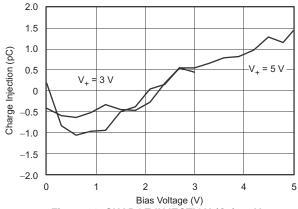


Figure 22. CHARGE-INJECTION (Q_C) vs V_{COM}

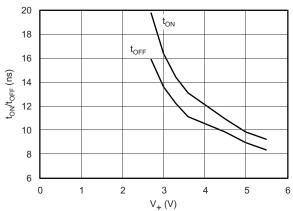


Figure 23. t_{ON} AND t_{OFF} vs SUPPLY VOLTAGE

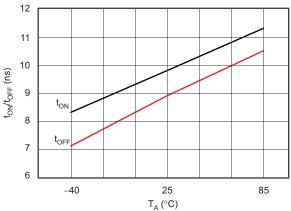


Figure 24. t_{ON} AND t_{OFF} vs TEMPERATURE (V+ = 5 V)



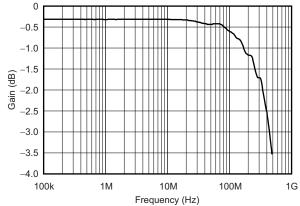


Figure 25. GAIN vs FREQUENCY

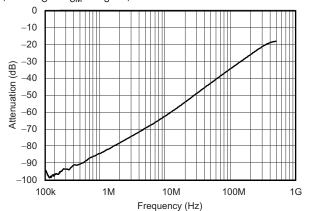


Figure 26. OFF ISOLATION vs FREQUENCY



APPLICATION INFORMATION

OPERATING VOLTAGE

The OPA1S238x operates over a power-supply range of +2.7 V to +5.5 V. Supply voltages higher than +6 V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or over temperature are shown in the *Typical Characteristics* section of this data sheet.

INPUT VOLTAGE

The OPA1S238x input common-mode voltage range extends 0.1 V beyond the supply rails. Under normal operating conditions, the input bias current is approximately 3 pA. Input voltages exceeding the supply voltage can cause excessive current to flow into or out of the input pins. If there is a possibility that this operating condition may occur, the inputs must be protected. Momentary voltages that exceed the supply voltage can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor between the signal and the input pin of the device.

OUTPUT VOLTAGE

Rail-to-rail output is achieved by using a class AB output stage with common-source transistors. For high-impedance loads (> 200Ω), the output voltage swing is typically 100 mV from the supply rails. With $10-\Omega$ loads, a useful output swing can be achieved while maintaining high open-loop gain; see Figure 13.

OUTPUT DRIVE

The OPA1S238x output stage can supply a continuous output current of ±100 mA and still provide approximately 2.7 V of output swing on a 5-V supply; see Figure 13.

The OPA1S238x provides peak currents of up to 200 mA, which corresponds to the typical short-circuit current. Therefore, an on-chip thermal shutdown circuit is provided to protect the OPA1S238x from dangerously-high junction temperatures. At +160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below +140°C.

CAPACITIVE LOAD AND STABILITY

The OPA1S238x can drive a wide range of capacitive loads. However, all op amps can become unstable under certain conditions. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability. An op amp in a unity-gain configuration is most susceptible to the effects of capacitive loading. The capacitive load reacts with the op amp output resistance, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin; see Figure 12 for details.

The OPA1S238x topology enhances its ability to drive capacitive loads. In unity gain, these op amps perform well with large capacitive loads. See Figure 10 and Figure 11 for details.

One method of improving capacitive load drive in the unity-gain configuration is to insert a $10-\Omega$ to $20-\Omega$ resistor in series with the output. This resistor significantly reduces ringing with large capacitive loads. For details about stability with certain output capacitors, see Figure 11. However, if there is a resistive load in parallel with the capacitive load, R_S creates a voltage divider. This voltage divider introduces a dc error at the output and slightly reduces output swing. This error may be insignificant. For instance, with $R_L = 10~k\Omega$ and $R_S = 20~\Omega$, there is only about a 0.2% error at the output.

WIDEBAND TRANSIMPEDANCE AMPLIFIER

Wide bandwidth, low input bias current and low current noise make the OPA1S238x an ideal wideband, photodiode, transimpedance amplifier for low-voltage, single-supply applications. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequencies.

POWER DISSIPATION

Power dissipation depends on power-supply voltage, signal, and load conditions. With dc signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor. Power dissipation can be minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

Submit Documentation Feedback

Copyright © 2012–2013, Texas Instruments Incorporated



For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power-supply voltage. Dissipation with ac signals is lower. Application bulletin AB-039 (SBOA022), *Power Amplifier Stress and Power Handling Limitations*, explains how to calculate or measure power dissipation with unusual signals and loads, and is available for download at www.ti.com.

Repeated activation of the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +150°C, maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered at +160°C. However, for reliable operation, design your system to operate at a maximum of 35°C below the thermal protection trigger temperature (that is, +125°C or less).

TYPICAL APPLICATIONS

The following sections show typical applications of the OPA1S238x and explain their basic functionality.

Signal Strength Detection

The OPA1S238x can be used to detect the signal strength of a fast changing optical signal. Figure 27 shows a simplified circuit for this application.

Optical sensors like photodiodes often generate a current that is proportional to the amount of light detected by these sensors. The current generated by this sensor is represented by the current source I_{IN} , as shown in Figure 27. One of the OPA1S238x op amps is configured in a transimpedance configuration. If it is assumed that this op amp behaves like an ideal op amp, then all the current generated by I_{IN} flows through R1 and generates a voltage drop of $I_{IN} \times R1$. The voltage at the output of this op amp can then be calculated by $V_{TIA} = V_{BIAS} + I_{IN} \times R1$. This calulation assumes ideal components.

In real-life applications, the current generated by I_{IN} can change very quickly. The current at a specific point in time can be measured by using the internal switch of the OPA1S238x. When the switch is closed, the C2 capacitor is charged to the output voltage level of the first amplifier (V_{TIA}). By opening the switch, the output is disconnected from C2, and the voltage at the noninverting terminal of the second op amp remains at the same voltage level as when the switch was opened. The second op amp is configured in a buffer configuration and prevents the C2 capacitor from being discharged by a load at the V_{OUT} terminal.

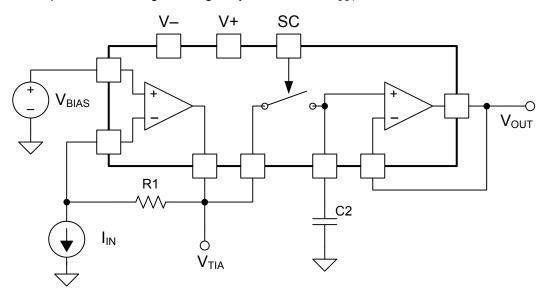


Figure 27. Signal Strength Detection



Sample and Hold

The OPA1S238x can be used in a basic sample-and-hold configuration. Figure 28 shows the simplified circuit for this application.

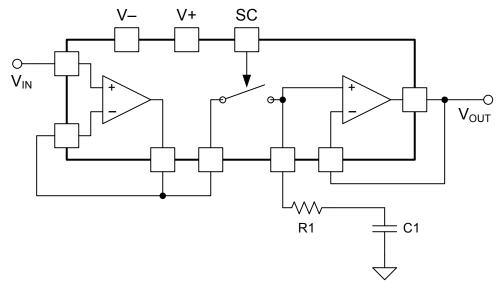


Figure 28. Sample-and-Hold Circuit

This sample-and-hold circuit can be used to sample the V_{IN} voltage at a specific point in time and hold it at V_{OUT} . This functionality is especially useful when fast-moving signals must be digitized.

When the switch connecting the two op amps is closed, the circuit operates in *track mode*. In track mode, if ideal components are assumed, the voltage at V_{OUT} follows the voltage at V_{IN} , only delayed by a filter consisting of R1 and C1.

As soon as the internal switch is opened, the output voltage no longer follows the input voltage. If ideal components are assumed again, the change in C1 remains constant and voltage at V_{OUT} reflects the voltage at V_{IN} at the moment that the switch was opened.

The values of R1 and C1 must be chosen depending on the bandwidth of the input signal, the sample time, and the hold time. Long hold times require larger capacitors in order to reduce the error from any leakage currents coming out of C1. Short sample times require smaller capacitors to allow for fast settling. It is important to choose the R1 value according to Figure 12 to prevent ringing or excessive damping, and to include the influence of switch on resistance in this selection.

There are several error sources that should be considered when designing a sample-and-hold circuit. The most important ones are:

- **Aperture Time** is the time required for a switch to open and remove the charging signal from the capacitor after the mode control signal has changed from sample to hold.
- **Effective Aperture Time** is the difference in propagation delay times of the analog signal and the mode control signal from their respective input pins to the switch.
- Charge Offset is the output voltage change that results from a charge transfer into the hold capacitor through stray capacitance when Hold mode is enabled.
- **Droop Rate** is the change in output voltage over time during Hold mode as a result of hold capacitor leakage, switch leakage, and bias current of the output amplifier.
- Drift Current is the net leakage current affecting the hold capacitor during Hold mode.
- **Hold Mode Feedthrough** is the fraction of the input signal that appears at the output while in Hold mode. It is primarily a function of switch capacitance, but may also be increased by poor layout practices.
- Hold Mode Settling Time is the time required for the sample-to-hold transient to settle within a specified error band.

Submit Documentation Feedback



REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

CI	hanges from Original (December 2012) to Revision A	Page
•	Changed document status from Product Mix to Production Data	1
•	Changed first sub-bullet of SPST Switch Features bullet	1
•	Changed Quiescent Current Features bullet	1
•	Added last two Features bullets	1
•	Changed front-page graphic footnote	1
•	Moved OPA1S2384 to Production Data	2
•	Deleted transport media column from Package Information table	2
•	Deleted second footnote from Package Information table	2
•	Changed title of Electrical Characteristics: Amplifier Section table	3
•	Changed Offset Voltage, Channel separation parameter	3
•	Changed Power Supply, I _Q parameter	4
•	Changed DC, Analog voltage range parameter maximum specification and Ron parameter typical specification	
•	Changed Dynamic, Q _C parameter test conditions	4
•	Changed block diagram footnote	
•	Added curve summary table	
•	Updated Figure 3	<mark>7</mark>
•	Updated Figure 18	9

www.ti.com

11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
OPA1S2384IDRCR	Active	Production	VSON (DRC) 10	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	OVAQ
OPA1S2384IDRCR.B	Active	Production	VSON (DRC) 10	3000 LARGE T&R	-	Call TI	Call TI	-40 to 85	
OPA1S2384IDRCT	Active	Production	VSON (DRC) 10	250 SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	OVAQ
OPA1S2384IDRCT.B	Active	Production	VSON (DRC) 10	250 SMALL T&R	-	Call TI	Call TI	-40 to 85	
OPA1S2385IDRCR	Active	Production	VSON (DRC) 10	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	OUZQ
OPA1S2385IDRCR.B	Active	Production	VSON (DRC) 10	3000 LARGE T&R	-	Call TI	Call TI	-40 to 85	
OPA1S2385IDRCT	Active	Production	VSON (DRC) 10	250 SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	OUZQ
OPA1S2385IDRCT.B	Active	Production	VSON (DRC) 10	250 SMALL T&R	=	Call TI	Call TI	-40 to 85	

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2025

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Jul-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1S2384IDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA1S2384IDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA1S2385IDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA1S2385IDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2



www.ti.com 24-Jul-2025



*All dimensions are nominal

	7 III GIII GII GII GII GII GII GII GII G								
	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
	OPA1S2384IDRCR	VSON	DRC	10	3000	353.0	353.0	32.0	
ı	OPA1S2384IDRCT	VSON	DRC	10	250	213.0	191.0	35.0	
	OPA1S2385IDRCR	VSON	DRC	10	3000	353.0	353.0	32.0	
	OPA1S2385IDRCT	VSON	DRC	10	250	213.0	191.0	35.0	

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com



PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025