

# OPA1632 High-Performance, Fully Differential Audio Operational Amplifier

## 1 Features

- Excellent sound quality
- Ultra low distortion: 0.000028%
- Low noise: 1.25 nV/ $\sqrt{\text{Hz}}$
- High speed:
  - Slew rate: 72 V/ $\mu\text{s}$
  - Gain bandwidth product: 180 MHz
- Fully differential architecture:
  - Balanced input and output converts single-ended input to balanced differential output
- Wide supply range:  $\pm 2.5 \text{ V}$  to  $\pm 15 \text{ V}$
- Shutdown current: 0.85 mA ( $V_S = \pm 5 \text{ V}$ )
- Temperature range:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$

## 2 Applications

- Professional audio mixer or control surface
- Professional microphones and wireless systems
- Professional speaker systems
- Professional audio amplifier
- Soundbar
- Turntable
- Professional video camera
- Guitar and other instrument amplifier
- Data acquisition (DAQ)

## 3 Description

The OPA1632 is a fully differential amplifier (FDA) designed to drive high-performance audio analog-to-digital converters (ADCs) or as a predriver for class-D amplifiers.

The OPA1632 delivers excellent audio quality, very low noise, large output voltage swing, and high current drive. The OPA1632 has an excellent gain bandwidth of 180 MHz, and a very fast slew rate of 72 V/ $\mu\text{s}$  that helps to produce exceptionally low distortion. A very low input voltage noise of 1.25 nV/ $\sqrt{\text{Hz}}$  further provides maximum signal-to-noise ratio and dynamic range.

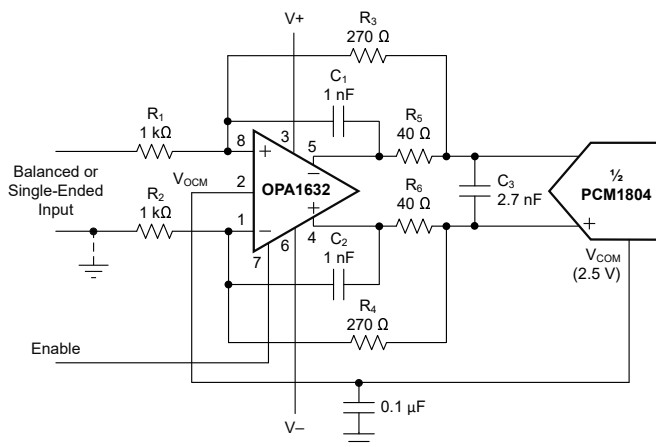
The flexibility of the fully differential architecture allows for easy implementation of a single-ended to fully differential output conversion. Differential output reduces even-order harmonics and minimizes common-mode noise interference. The OPA1632 provides excellent performance when used to drive high-performance audio ADCs such as the [PCM1804](#). A shutdown feature is included to save power when the device is not in use.

The OPA1632 is characterized to operate from  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  and is available in an SO-8 package and a thermally-enhanced HVSSOP-8 PowerPAD™ integrated circuit package.

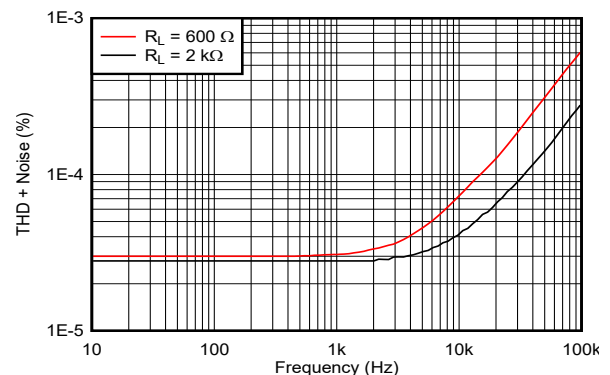
### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|-------------|------------------------|-----------------------------|
| OPA1632     | D (SOIC, 8)            | 4.9 mm × 6 mm               |
|             | DGN (HVSSOP, 8)        | 3 mm × 4.9 mm               |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Application Diagram



THD + Noise vs Frequency



## Table of Contents

|                                                |           |                                                                  |           |
|------------------------------------------------|-----------|------------------------------------------------------------------|-----------|
| <b>1 Features</b> .....                        | <b>1</b>  | 7.4 Device Functional Modes.....                                 | <b>13</b> |
| <b>2 Applications</b> .....                    | <b>1</b>  | <b>8 Application and Implementation</b> .....                    | <b>14</b> |
| <b>3 Description</b> .....                     | <b>1</b>  | 8.1 Application Information.....                                 | 14        |
| <b>4 Revision History</b> .....                | <b>2</b>  | 8.2 Typical Application.....                                     | 15        |
| <b>5 Pin Configuration and Functions</b> ..... | <b>5</b>  | 8.3 Power Supply Recommendations.....                            | 16        |
| <b>6 Specifications</b> .....                  | <b>6</b>  | 8.4 Layout.....                                                  | 16        |
| 6.1 Absolute Maximum Ratings.....              | 6         | <b>9 Device and Documentation Support</b> .....                  | <b>20</b> |
| 6.2 ESD Ratings.....                           | 6         | 9.1 Documentation Support.....                                   | 20        |
| 6.3 Recommended Operating Conditions.....      | 6         | 9.2 Receiving Notification of Documentation Updates.....         | 20        |
| 6.4 Thermal Information.....                   | 6         | 9.3 Support Resources.....                                       | 20        |
| 6.5 Electrical Characteristics.....            | 8         | 9.4 Trademarks.....                                              | 20        |
| 6.6 Typical Characteristics.....               | 10        | 9.5 Electrostatic Discharge Caution.....                         | 20        |
| <b>7 Detailed Description</b> .....            | <b>12</b> | 9.6 Glossary.....                                                | 20        |
| 7.1 Overview.....                              | 12        | <b>10 Mechanical, Packaging, and Orderable Information</b> ..... | <b>20</b> |
| 7.2 Functional Block Diagram.....              | 12        |                                                                  |           |
| 7.3 Feature Description.....                   | 13        |                                                                  |           |

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision D (March 2022) to Revision E (August 2023)</b>                                                                                                                                                | <b>Page</b> |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| • Changed all instances of MSOP package to VSSOP package and all instances of MSOP PowerPAD to HVSSOP.....                                                                                                             | 1           |
| • Changed ambient temperature in Recommended Operating Conditions to show only –40°C to +85°C.....                                                                                                                     | 6           |
| • Changed thermal specifications for DGN package in Thermal Information table.....                                                                                                                                     | 6           |
| • Changed Electrical Characteristics (EC) to combine both tables in to one table for both packages.....                                                                                                                | 8           |
| • Changed PSRR minimum limit of 316 $\mu\text{V/V}$ to maximum limit in EC table for DGN package.....                                                                                                                  | 8           |
| • Changed input offset drift, input voltage noise, small and large signal bandwidth, slew rate, rise and fall time, settling time, output voltage swing, and closed-loop output impedance to show improved values..... | 8           |
| • Changed typical and maximum input bias current from 2 $\mu\text{A}$ to 7.9 $\mu\text{A}$ and 6 $\mu\text{A}$ to 14 $\mu\text{A}$ , respectively for DGN package.....                                                 | 8           |
| • Changed input current noise from 0.4 $\text{pA}/\sqrt{\text{Hz}}$ to 1.7 $\text{pA}/\sqrt{\text{Hz}}$ in EC table for DGN package.....                                                                               | 8           |
| • Changed input impedance spec to show both common-mode and differential impedances in EC table for DGN package.....                                                                                                   | 8           |
| • Changed typical THD+N with differential input/output and $R_L = 2 \text{ k}\Omega$ from 0.000022% to 0.000028% in EC table for DGN package.....                                                                      | 8           |
| • Changed IMD of differential input/output and $R_L = 2 \text{ k}\Omega$ from 0.00005% to 0.000061% in EC table for DGN package.....                                                                                   | 8           |
| • Changed voltage output swing low and high to a typical only for a load of 2 $\text{k}\Omega$ in the EC table for DGN package.....                                                                                    | 8           |
| • Changed the enable and disable voltage threshold from $(V_-) + 2 \text{ V}$ and $(V_-) 0.8 \text{ V}$ to $(V_-) + 1.45 \text{ V}$ and $(V_-) 1.4 \text{ V}$ , respectively, for DGN package.....                     | 8           |
| • Changed one Turn-on delay specification to Turn-off delay in Electrical Characteristics table.....                                                                                                                   | 8           |
| • Deleted the DGN Typical Characteristics section and combined all plots into one section.....                                                                                                                         | 10          |
| <b>Changes from Revision C (September 2015) to Revision D (March 2022)</b>                                                                                                                                             | <b>Page</b> |
| • Updated the numbering format for tables, figures, and cross-references throughout the document.....                                                                                                                  | 1           |
| • Updated <i>Features</i> section.....                                                                                                                                                                                 | 1           |
| • Updated <i>Applications</i> section.....                                                                                                                                                                             | 1           |
| • Updated <i>Description</i> section.....                                                                                                                                                                              | 1           |
| • Changed nominal body size for both SOIC and MSOP-PowerPAD packages in <i>Description</i> section.....                                                                                                                | 1           |
| • Updated <i>Pin Configuration and Functions</i> section.....                                                                                                                                                          | 5           |

|                                                                                                                                                                            |   |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|
| • Added Supply turn-on/off dV/dT specification to Absolute Maximum Ratings table.....                                                                                      | 6 |
| • Added continuous input current specification to Absolute Maximum Ratings table.....                                                                                      | 6 |
| • Changed differential input voltage in Absolute Maximum Ratings table from $\pm 3V$ to $\pm 1.5V$ .....                                                                   | 6 |
| • Changed charged-device model (CDM) reference from JESD22-C101 to JS-002 in ESD Ratings table.....                                                                        | 6 |
| • Changed minimum temperature range from $0.4^{\circ}C$ to $-40^{\circ}C$ in Recommended Operating Conditions table.....                                                   | 6 |
| • Changed thermal specifications for D package in Thermal Information table.....                                                                                           | 6 |
| • Changed $R_{\theta JA}$ from $114.5^{\circ}C/W$ to $126.3^{\circ}C/W$ for D Package in Thermal Information table.....                                                    | 6 |
| • Changed $R_{\theta JC}(top)$ from $60.3^{\circ}C/W$ to $67.3^{\circ}C/W$ for D package in Thermal Information table.....                                                 | 6 |
| • Changed $R_{\theta JB}$ from $54.8^{\circ}C/W$ to $69.8^{\circ}C/W$ for D package in Thermal Information table.....                                                      | 6 |
| • Changed $\psi_{JT}$ from $14^{\circ}C/W$ to $19.5^{\circ}C/W$ for D package in Thermal Information table.....                                                            | 6 |
| • Changed $\psi_{JT}$ from $54.3^{\circ}C/W$ to $69.0^{\circ}C/W$ for D package in Thermal Information table.....                                                          | 6 |
| • Changed typical offset voltage vs temperature from $\pm 5 \mu V^{\circ}C$ to $\pm 2.5 \mu V^{\circ}C$ in <i>Electrical Characteristics: OPA1632D</i> table.....          | 8 |
| • Changed PSRR minimum limit of $316 \mu V/V$ to maximum limit in <i>Electrical Characteristics: OPA1632D</i> table .....                                                  | 8 |
| • Changed typical input bias current limit from $2 \mu A$ to $7.9 \mu A$ in <i>Electrical Characteristics: OPA1632D</i> table.....                                         | 8 |
| • Changed Max input bias current limit from $6 \mu A$ to $14 \mu A$ in <i>Electrical Characteristics: OPA1632D</i> table.....                                              | 8 |
| • Changed typical input voltage noise from $1.3 nV/\sqrt{Hz}$ to $1.25 nV/\sqrt{Hz}$ in <i>Electrical Characteristics: OPA1632D</i> table.....                             | 8 |
| • Changed typical input current noise from $0.4 pA/\sqrt{Hz}$ to $1.7 pA/\sqrt{Hz}$ in <i>Electrical Characteristics: OPA1632D</i> table.....                              | 8 |
| • Changed input impedance spec to show both common-mode and differential impedances in <i>Electrical Characteristics: OPA1632D</i> table.....                              | 8 |
| • Changed SSBW at $G = +2$ , $R_F = 602 \Omega$ from $90 MHz$ to $104 MHz$ in <i>Electrical Characteristics: OPA1632D</i> table.....                                       | 8 |
| • Changed SSBW at $G = +5$ , $R_F = 1.5 k\Omega$ from $36 MHz$ to $46 MHz$ in <i>Electrical Characteristics: OPA1632D</i> table.....                                       | 8 |
| • Changed SSBW at $G = +10$ , $R_F = 3.01 k\Omega$ from $18 MHz$ to $24 MHz$ in <i>Electrical Characteristics: OPA1632D</i> table.....                                     | 8 |
| • Changed typical Large-Signal Bandwidth from $800 kHz$ to $1.8 MHz$ in <i>Electrical Characteristics: OPA1632D</i> table.....                                             | 8 |
| • Changed typical slew rate from $50 V/\mu s$ to $72 V/\mu s$ in <i>Electrical Characteristics: OPA1632D</i> table .....                                                   | 8 |
| • Changed typical rise/fall time from $100 ns$ to $69 ns$ in <i>Electrical Characteristics: OPA1632D</i> table.....                                                        | 8 |
| • Changed typical settling time to $0.1\%$ from $75 ns$ to $36 ns$ in <i>Electrical Characteristics: OPA1632D</i> table.....                                               | 8 |
| • Changed typical settling time to $0.01\%$ from $200 ns$ to $49 ns$ in <i>Electrical Characteristics: OPA1632D</i> table .....                                            | 8 |
| • Changed typical THD+N with Differential Input/Output and $R_L = 600 \Omega$ from $0.0003\%$ to $0.00003\%$ in <i>Electrical Characteristics: OPA1632D</i> table.....     | 8 |
| • Changed typical THD+N with Differential Input/Output and $R_L = 2 k\Omega$ from $0.000022\%$ to $0.000028\%$ in <i>Electrical Characteristics: OPA1632D</i> table.....   | 8 |
| • Changed typical THD+N with single-ended Input/Output and $R_L = 600 \Omega$ from $0.000059\%$ to $0.000036\%$ in <i>Electrical Characteristics: OPA1632D</i> table ..... | 8 |
| • Changed typical THD+N with single-ended Input/Output and $R_L = 2 k\Omega$ from $0.000043\%$ to $0.000031\%$ in <i>Electrical Characteristics: OPA1632D</i> table.....   | 8 |
| • Changed IMD at differential input/output and $R_L = 600 \Omega$ from $0.00008\%$ to $0.000061\%$ in <i>Electrical Characteristics: OPA1632D</i> table.....               | 8 |
| • Changed IMD at differential input/output and $R_L = 2 k\Omega$ from $0.00005\%$ to $0.000061\%$ in <i>Electrical Characteristics: OPA1632D</i> table.....                | 8 |
| • Changed IMD at single-ended input/output and $R_L = 600 \Omega$ from $0.0001\%$ to $0.00007\%$ in <i>Electrical Characteristics: OPA1632D</i> table .....                | 8 |
| • Changed IMD at single-ended input/output and $R_L = 2 k\Omega$ from $0.0007\%$ to $0.000073\%$ in <i>Electrical Characteristics: OPA1632D</i> table.....                 | 8 |
| • Removed specified operating voltage specifications from <i>Electrical Characteristics: OPA1632D</i> table .....                                                          | 8 |

|                                                                                                     |    |
|-----------------------------------------------------------------------------------------------------|----|
| • Changed typical $I_Q$ from 14mA to 13mA in <i>Electrical Characteristics: OPA1632D</i> table..... | 8  |
| • Added new Typical Characteristics section for D package.....                                      | 10 |
| • Updated <i>Feature Description</i> section.....                                                   | 13 |
| • Updated <i>Output Common-Mode Voltage</i> section.....                                            | 14 |
| • Updated <i>Resistor Matching</i> section.....                                                     | 14 |
| • Updated <i>Application Curves</i> section.....                                                    | 16 |
| • Updated <i>Power Supply Recommendations</i> section.....                                          | 16 |
| • Updated the <i>Power Dissipation and Thermal Considerations</i> section.....                      | 18 |
| • Updated <i>Layout Example</i> section.....                                                        | 19 |
| • Changed list of documentation in <i>Related Documentation</i> section.....                        | 20 |

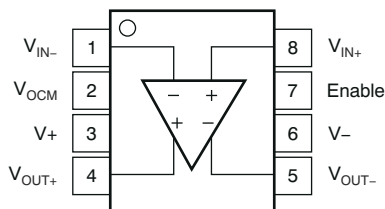
---

**Changes from Revision B (January 2010) to Revision C (September 2015)**
**Page**

|                                                                                                                                                                                                                                                                                                                                                     |   |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|
| • Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section..... | 1 |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|

---

## 5 Pin Configuration and Functions



**Figure 5-1. D Package, 8-Pin SOIC or DGN Package<sup>(1)</sup>, 8-Pin HVSSOP (Top View)**

**Table 5-1. Pin Functions**

| PIN               |     | TYPE <sup>(2)</sup> | DESCRIPTION                            |
|-------------------|-----|---------------------|----------------------------------------|
| NAME              | NO. |                     |                                        |
| Enable            | 7   | I                   | Active high enable pin                 |
| V+                | 3   | I/O                 | Positive supply voltage pin            |
| V–                | 6   | I/O                 | Negative supply voltage pin            |
| V <sub>IN+</sub>  | 8   | I                   | Positive input voltage pin             |
| V <sub>IN–</sub>  | 1   | I                   | Negative input voltage pin             |
| V <sub>OCM</sub>  | 2   | I                   | Output common-mode control voltage pin |
| V <sub>OUT+</sub> | 4   | O                   | Positive output voltage pin            |
| V <sub>OUT–</sub> | 5   | O                   | Negative output voltage pin            |

- (1) Solder the exposed DGN (HVSSOP) package thermal pad to a heat-spreading power or ground plane. This pad is electrically isolated from the die, but must be connected to a power or ground plane and not floated.
- (2) I = input, O = output.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

|                  |                                                  | MIN | MAX             | UNIT |
|------------------|--------------------------------------------------|-----|-----------------|------|
| V <sub>S</sub>   | Supply voltage                                   |     | ±16.5           | V    |
|                  | Supply turn on and turn off dV/dT <sup>(3)</sup> |     | 1.7             | V/μs |
| V <sub>I</sub>   | Input voltage                                    |     | ±V <sub>S</sub> | V    |
| I <sub>O</sub>   | Output current                                   |     | 150             | mA   |
| I <sub>IN</sub>  | Continuous input current                         |     | 10              | mA   |
| V <sub>ID</sub>  | Differential input voltage                       |     | ±1.5            | V    |
| T <sub>J</sub>   | Junction temperature                             |     | 150             | °C   |
| T <sub>A</sub>   | Ambient temperature                              | –40 | 85              | °C   |
| T <sub>stg</sub> | Storage temperature                              | –65 | 150             | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The OPA1632 HVSSOP PowerPAD integrated circuit package incorporates a thermal pad on the underside of the chip. This thermal pad acts as a heat sink and must be connected to a thermally-dissipative plane for proper power dissipation. Failure to do so can result in exceeding the maximum junction temperature, which can permanently damage the device. See TI technical brief [SLMA002](#) for more information about using the thermally-enhanced PowerPAD integrated circuit package.
- (3) Stay below this specification to make sure that the edge-triggered ESD absorption devices across the supply pins remain off.

### 6.2 ESD Ratings

|                    |                         |                                                                       | VALUE | UNIT |
|--------------------|-------------------------|-----------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>     | ±1000 | V    |
|                    |                         | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup> | ±500  |      |
|                    |                         | Machine model                                                         | ±200  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                |                     |        | MIN  | MAX | UNIT |
|----------------|---------------------|--------|------|-----|------|
| V <sub>S</sub> | Supply voltage      | Dual   | ±2.5 | ±15 | V    |
|                |                     | Single | 5    | 30  |      |
| T <sub>A</sub> | Ambient temperature |        | –40  | 85  | °C   |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | OPA1632  |              | UNIT |
|-------------------------------|----------------------------------------------|----------|--------------|------|
|                               |                                              | D (SOIC) | DGN (HVSSOP) |      |
|                               |                                              | 8 PINS   | 8 PINS       |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 126.3    | 57.6         | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 67.3     | 76.3         | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 69.8     | 30.0         | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 19.5     | 4.0          | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 69.0     | 29.9         | °C/W |

| THERMAL METRIC <sup>(1)</sup> |                                              | OPA1632  |              | UNIT |
|-------------------------------|----------------------------------------------|----------|--------------|------|
|                               |                                              | D (SOIC) | DGN (HVSSOP) |      |
|                               |                                              | 8 PINS   | 8 PINS       |      |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A      | 14.3         | °C/W |

(1) For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

at  $V_S = \pm 15\text{ V}$ ,  $R_F = 390\ \Omega$ ,  $R_L = 800\ \Omega$ , and  $G = +1$  (unless otherwise noted)

| PARAMETER                             |                     |                                  | TEST CONDITIONS                                          |                                   | MIN                     | TYP | MAX                   | UNIT     |
|---------------------------------------|---------------------|----------------------------------|----------------------------------------------------------|-----------------------------------|-------------------------|-----|-----------------------|----------|
| OFFSET VOLTAGE                        |                     |                                  |                                                          |                                   |                         |     |                       |          |
| Input offset voltage                  |                     |                                  |                                                          |                                   | ±0.5                    |     | ±3                    | mV       |
|                                       | vs temperature, dc  | dV <sub>OS</sub> /dT             |                                                          |                                   | ±2.5                    |     |                       | µV/°C    |
|                                       | vs power supply, dc | PSRR                             |                                                          |                                   | 13                      |     | 316                   | µV/V     |
| INPUT BIAS CURRENT                    |                     |                                  |                                                          |                                   |                         |     |                       |          |
| Input bias current, I <sub>B</sub>    |                     |                                  |                                                          |                                   | 7.9                     |     | 14                    | µA       |
| Input offset current, I <sub>OS</sub> |                     |                                  |                                                          |                                   | ±100                    |     | ±500                  | nA       |
| NOISE                                 |                     |                                  |                                                          |                                   |                         |     |                       |          |
| Input voltage noise                   |                     |                                  | f = 10 kHz                                               |                                   | 1.25                    |     |                       | nV/√Hz   |
| Input current noise                   |                     |                                  | f = 10 kHz                                               |                                   | 1.7                     |     |                       | pA/√Hz   |
| INPUT VOLTAGE                         |                     |                                  |                                                          |                                   |                         |     |                       |          |
| Common-mode input voltage             |                     |                                  |                                                          |                                   | (V <sup>-</sup> ) + 1.5 |     | (V <sup>+</sup> ) - 1 | V        |
| Common-mode rejection ratio, dc       |                     |                                  |                                                          |                                   | 74                      |     | 90                    | dB       |
| INPUT IMPEDANCE                       |                     |                                  |                                                          |                                   |                         |     |                       |          |
| Input impedance                       |                     |                                  | Measured into each input pin, common-mode                |                                   | 215    1.4              |     |                       | MΩ    pF |
|                                       |                     |                                  | Measured into each input pin, differential               |                                   | 10    3.1               |     |                       | kΩ    pF |
| OPEN-LOOP GAIN                        |                     |                                  |                                                          |                                   |                         |     |                       |          |
| Open-loop gain, dc                    |                     |                                  |                                                          |                                   | 66                      |     | 78                    | dB       |
| FREQUENCY RESPONSE                    |                     |                                  |                                                          |                                   |                         |     |                       |          |
| Small-signal bandwidth                |                     |                                  | G = +1, R <sub>F</sub> = 348 Ω                           |                                   | 180                     |     | MHz                   |          |
|                                       |                     |                                  | V <sub>O</sub> = 100 mV <sub>PP</sub> , peaking < 0.5 dB | G = +2, R <sub>F</sub> = 602 Ω    | 104                     |     |                       |          |
|                                       |                     |                                  |                                                          | G = +5, R <sub>F</sub> = 1.5 kΩ   | 46                      |     |                       |          |
|                                       |                     |                                  |                                                          | G = +10, R <sub>F</sub> = 3.01 kΩ | 24                      |     |                       |          |
| Bandwidth for 0.1-dB flatness         |                     |                                  | G = +1, V <sub>O</sub> = 100 mV <sub>PP</sub>            |                                   | 40                      |     | MHz                   |          |
| Peaking at a gain of 1                |                     |                                  | V <sub>O</sub> = 100 mV <sub>PP</sub>                    |                                   | 0.5                     |     | dB                    |          |
| Large-signal bandwidth                |                     |                                  | G = +2, V <sub>O</sub> = 20 V <sub>PP</sub>              |                                   | 1.8                     |     | MHz                   |          |
| Slew rate (25% to 75%)                |                     |                                  | G = +1                                                   |                                   | 72                      |     | V/µs                  |          |
| Rise and fall time                    |                     |                                  | G = +1, V <sub>O</sub> = 5-V step                        |                                   | 69                      |     | ns                    |          |
| Settling time                         | To 0.1%             |                                  | G = +1, V <sub>O</sub> = 2-V step                        |                                   | 36                      |     | ns                    |          |
|                                       | To 0.01%            |                                  | G = +1, V <sub>O</sub> = 2-V step                        |                                   | 49                      |     |                       |          |
| Total harmonic distortion + noise     |                     | Differential input/output        | G = +1, f = 1 kHz, V <sub>O</sub> = 3 V <sub>RMS</sub>   | R <sub>L</sub> = 600 Ω            | 0.00003%                |     |                       |          |
|                                       |                     |                                  |                                                          | R <sub>L</sub> = 2 kΩ             | 0.000028%               |     |                       |          |
|                                       |                     | Single-ended in/differential out | G = +1, f = 1 kHz, V <sub>O</sub> = 3 V <sub>RMS</sub>   | R <sub>L</sub> = 600 Ω            | 0.000036%               |     |                       |          |
|                                       |                     |                                  |                                                          | R <sub>L</sub> = 2 kΩ             | 0.000031%               |     |                       |          |
| Intermodulation distortion            |                     | Differential input/output        | G = +1, SMPTE/DIN, V <sub>O</sub> = 2 V <sub>PP</sub>    | R <sub>L</sub> = 600 Ω            | 0.000061%               |     |                       |          |
|                                       |                     |                                  |                                                          | R <sub>L</sub> = 2 kΩ             | 0.000061%               |     |                       |          |
|                                       |                     | Single-ended in/differential out | G = +1, SMPTE/DIN, V <sub>O</sub> = 2 V <sub>PP</sub>    | R <sub>L</sub> = 600 Ω            | 0.000073%               |     |                       |          |
|                                       |                     |                                  |                                                          | R <sub>L</sub> = 2 kΩ             | 0.00007%                |     |                       |          |
| Headroom                              |                     |                                  | THD < 0.01%, R <sub>L</sub> = 2 kΩ                       |                                   | 20                      |     | V <sub>PP</sub>       |          |



## 6.5 Electrical Characteristics (continued)

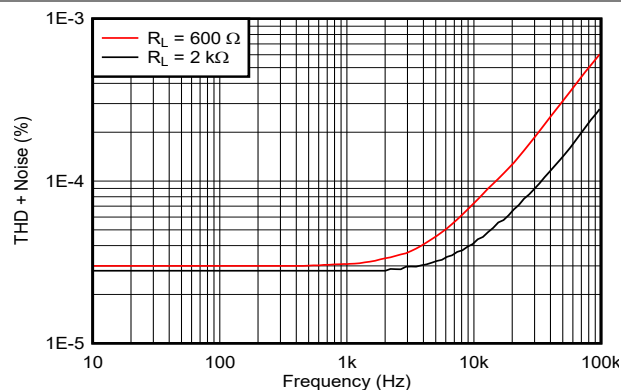
at  $V_S = \pm 15\text{ V}$ ,  $R_F = 390\ \Omega$ ,  $R_L = 800\ \Omega$ , and  $G = +1$  (unless otherwise noted)

| PARAMETER                              | TEST CONDITIONS                                   | MIN         | TYP  | MAX  | UNIT |
|----------------------------------------|---------------------------------------------------|-------------|------|------|------|
| OUTPUT                                 |                                                   |             |      |      |      |
| Voltage output swing low               | R <sub>L</sub> = 2 kΩ                             | (V−) + 1.6  |      |      | V    |
|                                        | R <sub>L</sub> = 1 kΩ                             | (V−) + 3.5  |      |      |      |
| Voltage output swing high              | R <sub>L</sub> = 2 kΩ                             | (V+) − 1.6  |      |      | V    |
|                                        | R <sub>L</sub> = 1 kΩ                             | (V+) − 3.5  |      |      |      |
| Short-circuit current, I <sub>SC</sub> | Sourcing                                          | 50          | 85   |      | mA   |
|                                        | Sinking                                           | −60         | −85  |      |      |
| Closed-loop output impedance           | G = +1, f = 100 kHz                               |             | 0.22 |      | Ω    |
| POWER DOWN                             |                                                   |             |      |      |      |
| Enable voltage threshold               |                                                   | (V−) + 1.45 |      |      | V    |
| Disable voltage threshold              |                                                   | (V−) + 1.4  |      |      | V    |
| Shutdown current <sup>(1)</sup>        | V <sub>S</sub> = ±5 V, V <sub>ENABLE</sub> = −5 V | 0.85        |      |      | mA   |
|                                        | V <sub>ENABLE</sub> = −15 V                       | 1.7         |      |      |      |
| Turn-on delay                          | Time for I <sub>Q</sub> to reach 50%              |             | 2    |      | μs   |
| Turn-off delay                         | Time for I <sub>Q</sub> to reach 50%              |             | 2    |      | μs   |
| POWER SUPPLY                           |                                                   |             |      |      |      |
| Quiescent current, I <sub>Q</sub>      |                                                   |             | 13   | 17.1 | mA   |

(1) Amplifier has internal 250-k $\Omega$  pullup resistor to  $V_+$  pin. This pullup resistor enables the amplifier with no connection to shutdown pin.

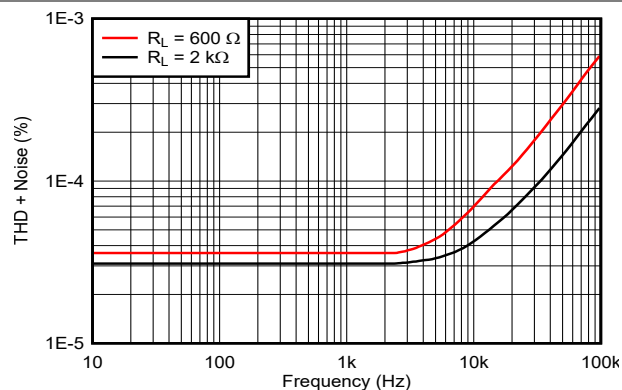
## 6.6 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_F = 348\ \Omega$ ,  $G = +1$  and  $R_L = 2\text{ k}\Omega$  (unless otherwise noted)



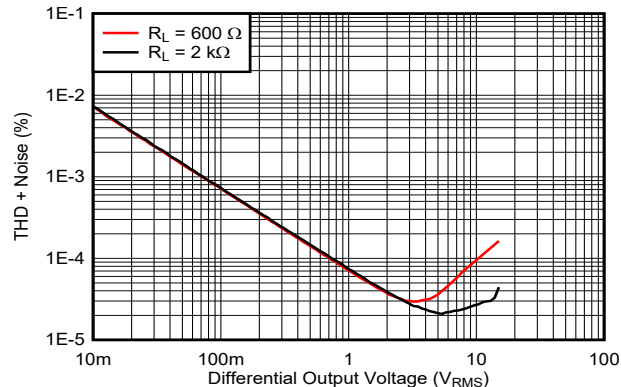
$V_O = 3\text{ V}_{\text{RMS}}$ , differential input and output

**Figure 6-1. THD + Noise vs Frequency**



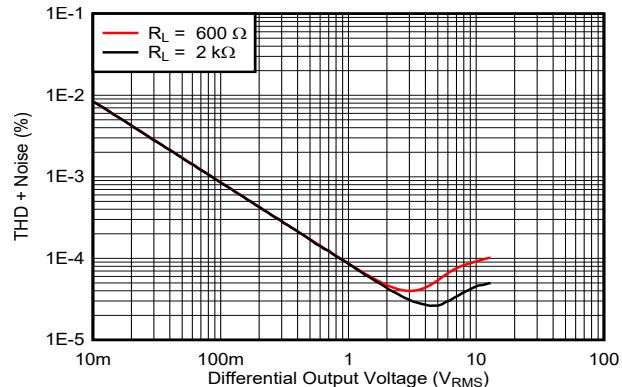
$V_O = 3\text{ V}_{\text{RMS}}$ , single-ended input to differential output

**Figure 6-2. THD + Noise vs Frequency**



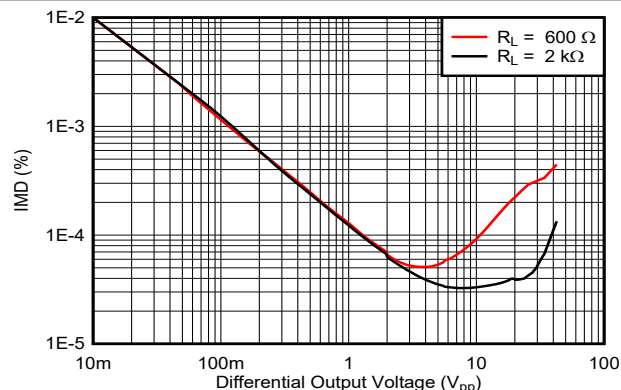
$f = 1\text{ kHz}$ , differential input and output

**Figure 6-3. THD + Noise vs Output Voltage**



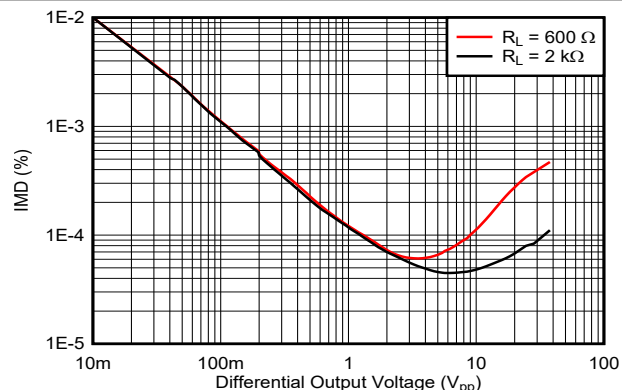
$f = 1\text{ kHz}$ ; single-ended input to differential output

**Figure 6-4. THD + Noise vs Output Voltage**



SMPTE 4:1: 60 Hz, 7 kHz; DIN 4:1: 250 Hz, 8 kHz, differential input and output

**Figure 6-5. Intermodulation Distortion vs Output Voltage**



SMPTE 4:1: 60 Hz, 7 kHz; DIN 4:1: 250 Hz, 8 kHz, differential input and output

**Figure 6-6. Intermodulation Distortion vs Output Voltage**

## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_F = 348\ \Omega$ ,  $G = +1$  and  $R_L = 2\text{ k}\Omega$  (unless otherwise noted)

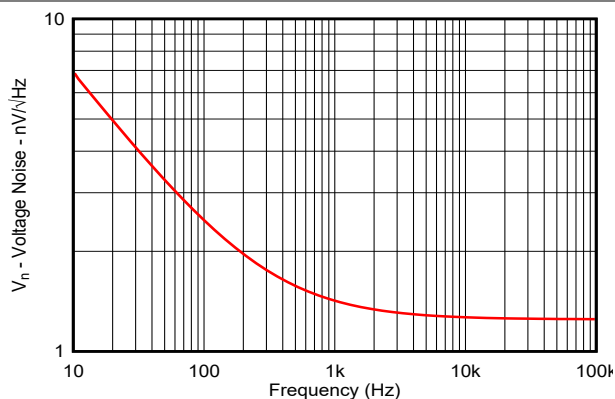


Figure 6-7. Voltage Noise vs Frequency

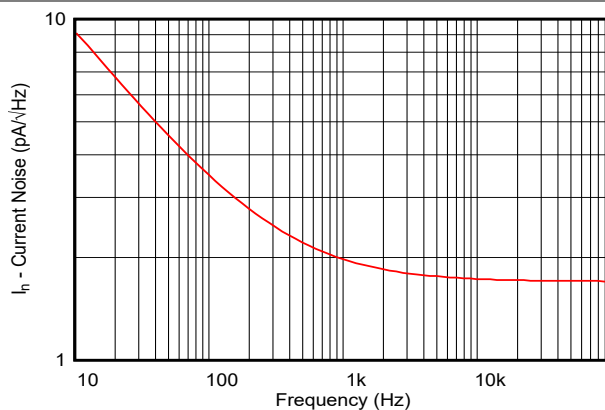


Figure 6-8. Current Noise vs Frequency

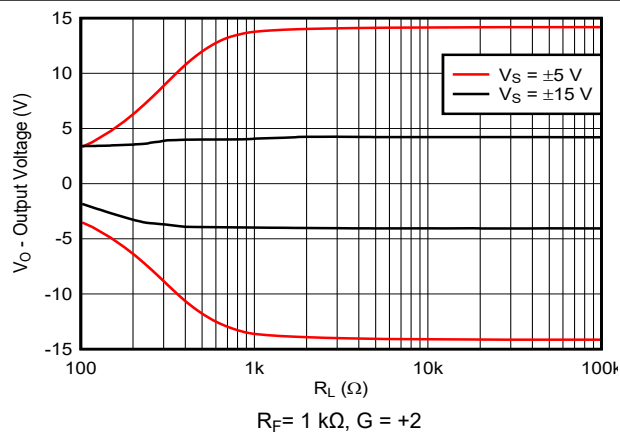


Figure 6-9. Output Voltage vs Differential Load Resistance

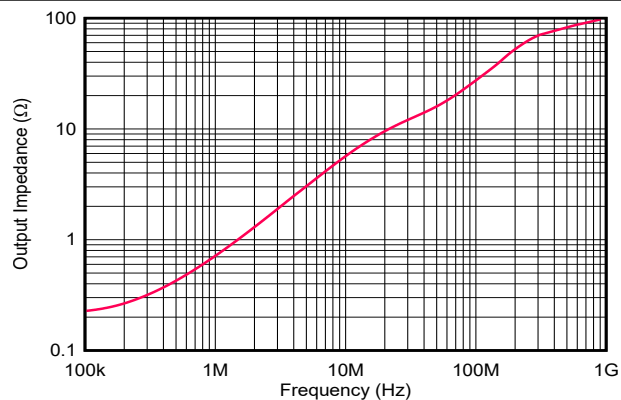


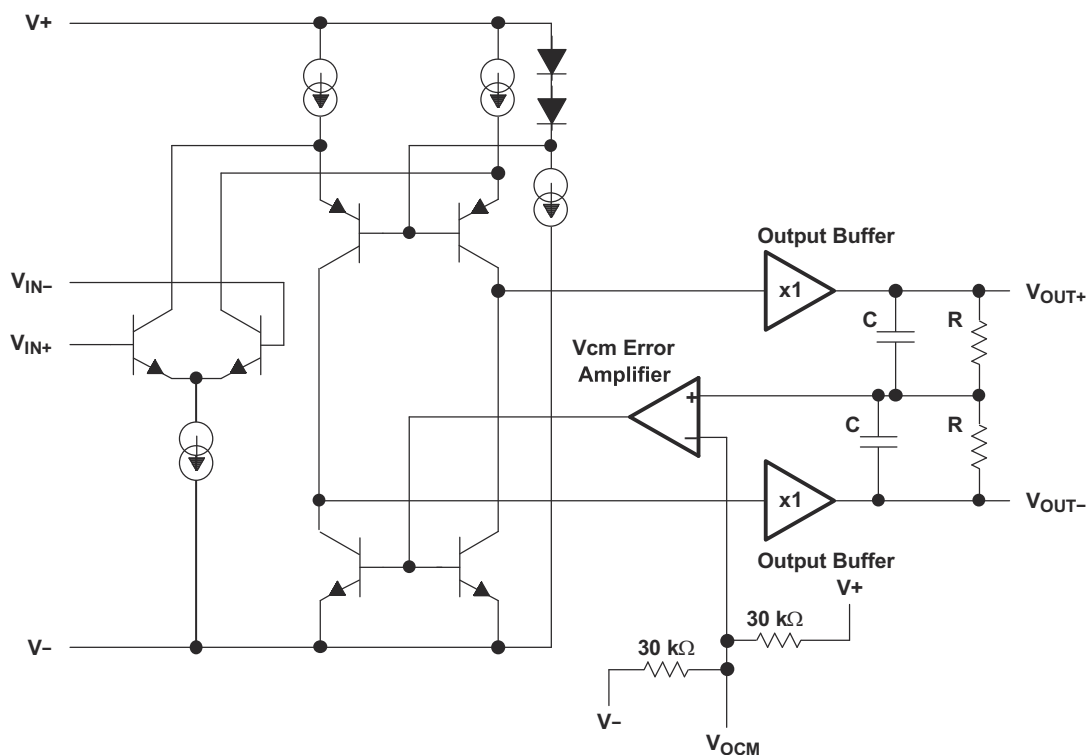
Figure 6-10. Output Impedance vs Frequency

## 7 Detailed Description

### 7.1 Overview

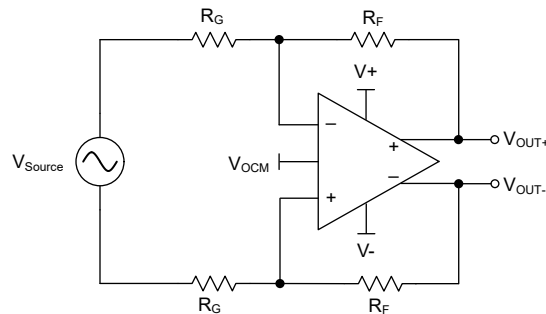
The OPA1632 is a fully differential amplifier (FDA). Differential signal processing offers a number of performance advantages in high-speed analog signal processing systems, including immunity to external common-mode noise, suppression of even-order nonlinearities, and increased dynamic range. FDAs not only serve as the primary means of providing gain to a differential signal chain, but also provide a monolithic solution for converting single-ended signals into differential signals allowing for easy, high-performance processing. For more information on the basic theory of operation for FDAs, refer to the [Fully Differential Amplifiers application note](#)

### 7.2 Functional Block Diagram

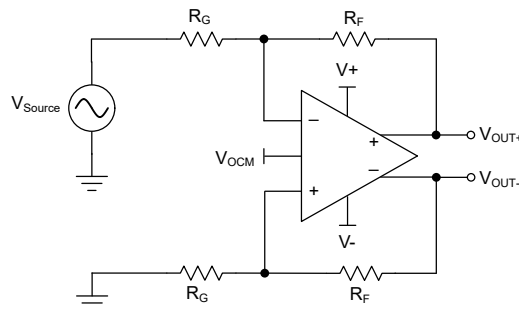


## 7.3 Feature Description

Figure 7-1 and Figure 7-2 depict the differences between the operation of the OPA1632 in two different modes. FDAs can work with differential inputs or can be implemented as single input and differential output.



**Figure 7-1. Amplifying Differential Input Signals**



**Figure 7-2. Amplifying Single-Ended Input Signals**

## 7.4 Device Functional Modes

### 7.4.1 Shutdown Function

The shutdown (enable) function of the OPA1632 is referenced to the negative supply of the operational amplifier. A valid logic low (< 0.8 V above negative supply) applied to the enable pin (pin 7) disables the amplifier output. Voltages applied to pin 7 that are greater than 2 V above the negative supply place the amplifier output in an active state, and the device is enabled. If pin 7 is left disconnected, an internal pull-up resistor enables the device. Turn-on and turn-off times are approximately 2  $\mu$ s each.

Quiescent current is reduced to approximately 0.85 mA when the amplifier is disabled. When disabled, the output stage is *not* in a high-impedance state. Thus, the shutdown function cannot be used to create a multiplexed switching function in series with multiple amplifiers.

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Output Common-Mode Voltage

The output common-mode voltage pin sets the dc output voltage of the OPA1632. A voltage applied to the  $V_{OCM}$  pin from a low-impedance source can be used to directly set the output common-mode voltage. If left floating, the  $V_{OCM}$  pin defaults to the mid-rail voltage, defined as:

$$\frac{(V_+) + (V_-)}{2} \quad (1)$$

To minimize common-mode noise, connect a 0.1-uF bypass capacitor to the  $V_{OCM}$  pin. Output common-mode voltage causes additional current to flow in the feedback resistor network. This current is supplied by the output stage of the amplifier; therefore, additional power dissipation is created. For commonly-used feedback resistance values, this current is easily supplied by the amplifier. The additional internal power dissipation created by this current can be significant in some applications and can dictate use of the HVSSOP PowerPAD™ integrated circuit package to effectively control self-heating.

##### 8.1.1.1 Resistor Matching

Resistor matching is important in FDAs to maintain good output balance. An ideal differential output signal implies the two outputs of the FDA should be exactly equal in amplitude and shifted 180° in phase. Any imbalance in amplitude or phase between the two output signals results in an undesirable common-mode signal at the output. The output balance error is a measure of how well the outputs are balanced and is defined as the ratio of the output common-mode voltage to the output differential signal.

$$\text{Output Balance Error} = \frac{\left( \frac{V_{OUT+} - V_{OUT-}}{2} \right)}{V_{OUT+} - V_{OUT-}} \quad (2)$$

At low frequencies, resistor mismatch is the primary contributor to output balance errors. Additionally CMRR, PSRR, and HD2 performance diminish if resistor mismatch occurs. Therefore, use 1% tolerance resistors or better to optimize performance. See [Table 8-1](#) for recommended resistor values to use for a particular gain.

**Table 8-1. Recommended Resistor Values**

| GAIN (V/V) | $R_G$ (Ω) | $R_F$ (Ω) |
|------------|-----------|-----------|
| 1          | 390       | 390       |
| 2          | 374       | 750       |
| 5          | 402       | 2010      |
| 10         | 402       | 4020      |

### Figure 8-1. ADC Driver for Professional Audio

### 8.2.1 Design Requirements

Table 8-2 shows example design parameters and values for the typical application design example in Figure 7-1.

### Table 8-2. Design Parameters

| DESIGN PARAMETERS  | VALUE                                                 |
|--------------------|-------------------------------------------------------|
| Supply voltage     | $\pm 2.5\text{ V}$ to $\pm 15\text{ V}$               |
| Amplifier topology | Voltage feedback                                      |
| Output control     | DC-coupled with output common-mode control capability |
| Filter requirement | 500-kHz, multiple-feedback low-pass filter            |

### 8.2.2 Detailed Design Procedure

Supply voltages of  $\pm 15$  V are commonly used for the OPA1632. The relatively low input voltage swing required by the ADC allows use of lower power-supply voltage, if desired. Power supplies as low as  $\pm 8$  V can be used in this application with excellent performance. Lower-voltage operation reduces power dissipation and heat rise. Bypass power supplies with 10- $\mu$ F tantalum capacitors in parallel with 0.1- $\mu$ F ceramic capacitors to avoid possible oscillations and instability.

The  $V_{COM}$  reference voltage output on the PCM1804 ADC provides the proper input common-mode reference voltage (2.5 V). This  $V_{COM}$  voltage is buffered with op amp  $A_2$  and drives the output common-mode voltage pin of the OPA1632. This biases the average output voltage of the OPA1632 to 2.5 V.

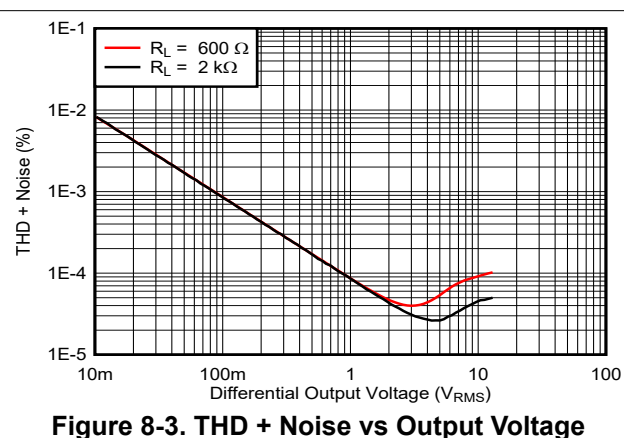
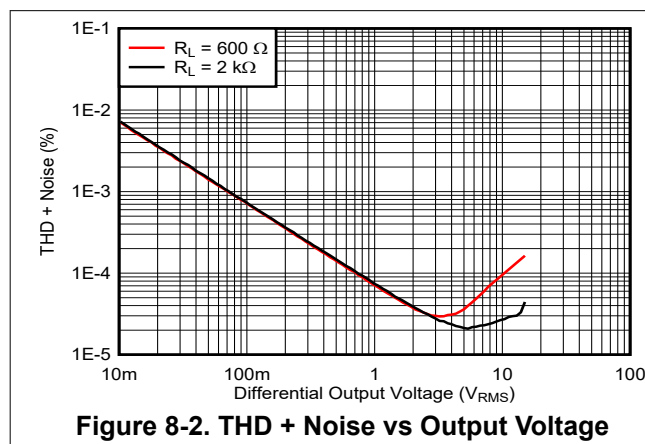
The signal gain of the circuit is generally set to approximately 0.25 to be compatible with commonly-used audio line levels. Gain can be adjusted, if necessary, by changing the values of  $R_1$  and  $R_2$ . Keep the feedback resistor values ( $R_3$  and  $R_4$ ) relatively low, as indicated, for best noise performance.

Resistors  $R_5$  and  $R_6$  and capacitor  $C_3$  provide an input filter and charge glitch reservoir for the ADC. The values shown are generally satisfactory. Some adjustment of the values can help optimize performance with different ADCs.

Make sure to maintain accurate resistor matching on  $R_1/R_2$  and  $R_3/R_4$  to achieve good differential signal balance. Use 1% resistors for highest performance. When connected for single-ended inputs (inverting input grounded, as shown in [Figure 8-1](#)), the source impedance must be low. Differential input sources must have well-balanced or low source impedance.

Choose capacitors  $C_1$ ,  $C_2$ , and  $C_3$  carefully for good distortion performance. Polystyrene, polypropylene, NPO ceramic, and mica types are generally excellent. Polyester and high-K ceramic types such as Z5U can create distortion.

### 8.2.3 Application Curves



## 8.3 Power Supply Recommendations

The OPA1632 device is designed to operate on power supplies ranging from  $\pm 2.5$  V to  $\pm 15$  V. Single power supplies ranging from 5 V to 30 V can also be used. Use a power-supply accuracy of 5%, or better. When operated on a board with high-speed digital signals, make sure to provide isolation between digital signal noise and the analog input pins. The OPA1632 is connected to power supplies through pin 3 ( $V_+$ ) and pin 6 ( $V_-$ ). Decouple each supply pin to GND as close to the device as possible with a low-inductance, surface-mount ceramic capacitor of approximately 10 nF. When vias are used to connect the bypass capacitors to a ground plane configure the vias for minimal parasitic inductance. One method of reducing via inductance is to use multiple vias. For broadband systems, two capacitors per supply pin are advised.

To avoid undesirable signal transients, do not power on the OPA1632 device with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs when an ADC is used in the application.

## 8.4 Layout

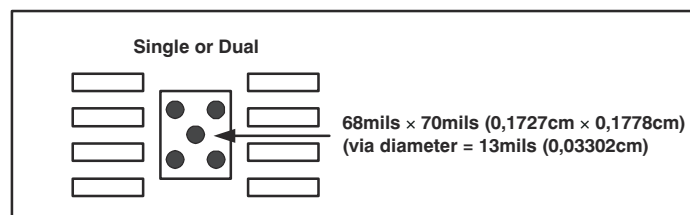
### 8.4.1 Layout Guidelines

1. The thermal pad is electrically isolated from the silicon and all leads. Connecting the thermal pad to any potential voltage between the power-supply voltages is acceptable, but best practice is to tie to ground because ground is generally the largest conductive plane.
2. Prepare the PCB with a top-side etch pattern as shown in [Figure 8-4](#). Use etch for the leads as well as etch for the thermal pad.



3. Place five holes in the area of the thermal pad that are 13 mils (0,03302 cm) in diameter. Keep these holes small so that solder wicking through the holes is not a problem during reflow.
4. Additional vias can be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the OPA1632 device, and can be larger than the 13-mil diameter vias directly under the thermal pad. These vias can be larger because the vias are not in the thermal pad area to be soldered so that wicking is not a problem.
5. Connect all holes to the internal ground plane.
6. When connecting these holes to the plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This slow heat transfer makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, make sure the holes under the OPA1632 PowerPAD™ integrated circuit package connect to the internal plane with a complete connection around the entire circumference of the plated through-hole.
7. The top-side solder mask must leave the package pins and the thermal pad area with the five holes exposed. The bottom-side solder mask must cover the five holes of the thermal pad area. This configuration prevents solder from being pulled away from the thermal pad area during the reflow process.
8. Apply solder paste to the exposed thermal pad area and all of the device pins.

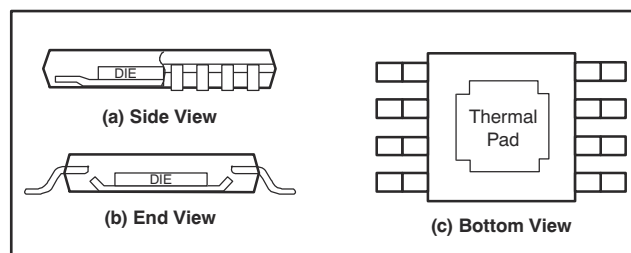
With these preparatory steps in place, the device is simply placed in position and runs through the solder reflow operation as any standard surface-mount component. This process results in a part that is properly installed.



**Figure 8-4. Thermal Pad PCB Etch and Via Pattern**

#### **8.4.1.1 PowerPAD™ Integrated Circuit Package Design Considerations**

The OPA1632 is available in a thermally-enhanced PowerPAD™ integrated circuit package. This package is constructed using a downset leadframe upon which the die is mounted (see [Figure 8-5\(a\)](#) and [Figure 8-5\(b\)](#)). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package (see [Figure 8-5\(c\)](#)). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.



**Figure 8-5. Views of the Thermally-Enhanced Package**

The PowerPAD integrated circuit package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the thermal pad to the printed circuit board (PCB) is always required, even with

applications that have low power dissipation. The thermal pad provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

#### 8.4.1.2 Power Dissipation and Thermal Considerations

The OPA1632 does not have thermal shutdown protection. Make sure that the maximum junction temperature is not exceeded. Excessive junction temperature can degrade performance or cause permanent damage. For best performance and reliability, make sure that the junction temperature does not exceed the absolute maximum ratings for the junction temperature.

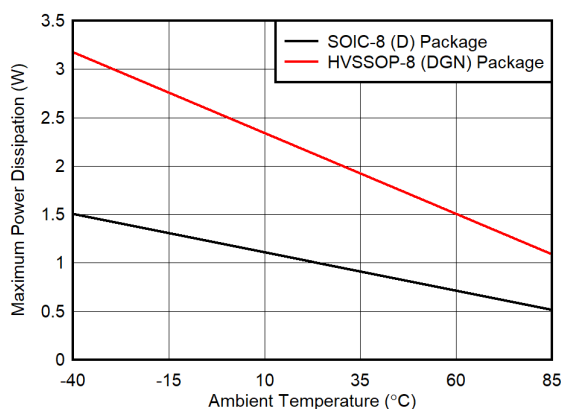
The thermal characteristics of the device are dictated by the package and the circuit board. Maximum power dissipation for a given package can be calculated using the following formula:

$$P_{DMax} = \frac{T_{Max} - T_A}{\theta_{JA}}$$

where:

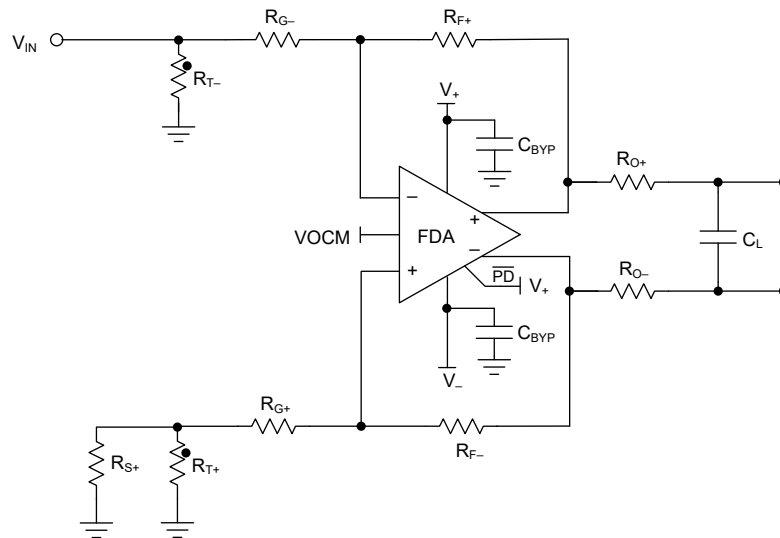
- $P_{DMax}$  is the maximum power dissipation in the amplifier (W)
- $T_{Max}$  is the absolute maximum junction temperature (°C)
- $T_A$  is the ambient temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- $\theta_{JC}$  is the thermal coefficient from the silicon junctions to the case (°C/W)
- $\theta_{CA}$  is the thermal coefficient from the case to ambient air (°C/W)

For systems where heat dissipation is more critical, the OPA1632 is offered in an HVSSOP-8 (DGN) PowerPAD integrated circuit package. The thermal coefficient for the PowerPAD integrated circuit package is substantially improved over the traditional SO package. Maximum power dissipation levels are depicted in [Figure 8-6](#) for the two packages. The data for the DGN package assume a board layout that follows the layout guidelines listed in [Section 8.4.1.1](#).

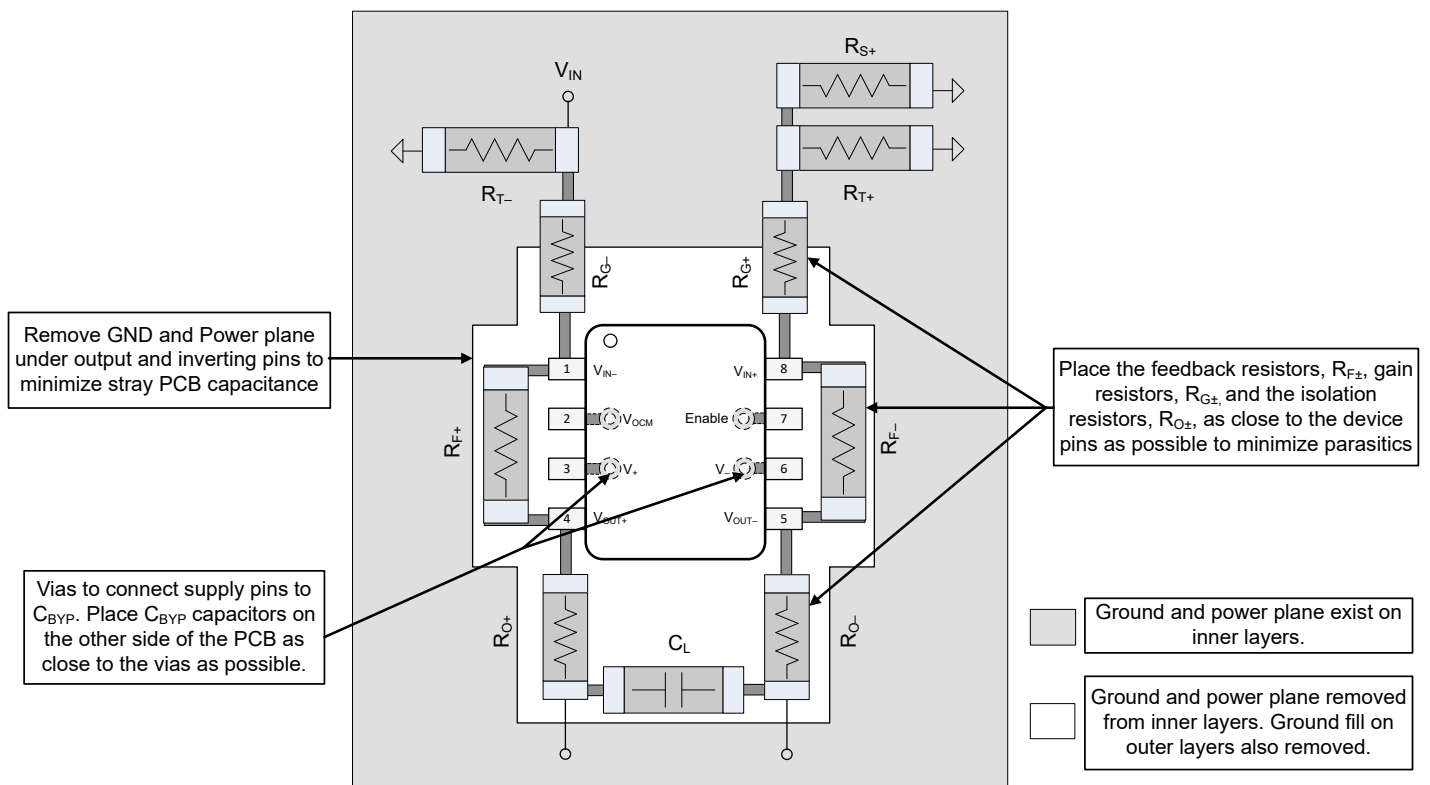


**Figure 8-6. Maximum Power Dissipation vs Ambient Temperature**

## 8.4.2 Layout Example



**Figure 8-7. Representative Schematic for Example Layout**



**Figure 8-8. Example Layout**

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Fully Differential Amplifiers application note](#)
- Texas Instruments, [TI Precision Labs - Fully Differential Amplifiers video series](#)
- Texas Instruments, [Maximizing Signal-Chain Distortion Performance Using High-Speed Amplifiers application note](#)
- Texas Instruments, [Analog Audio Amplifier Front-End Reference Design With Improved Noise and Distortion](#)
- Texas Instruments, [Public Announcement Audio Reference Design Utilizing Best in Class Boost Controller](#)
- Texas Instruments, [Motherboard/Controller for the AMC1210 reference design](#)
- Texas Instruments, [TPA6120A2 Stereo, 9.0-V to 33.0-V, Analog Input Headphone Amplifier With 128-dB Dynamic Range](#)
- Texas Instruments, [OPAx863 Low-Power, 110-MHz, Rail-to-Rail Input/Output Voltage-Feedback Op Amps](#)
- Texas Instruments, [OPA2834 50-MHz, 170- \$\mu\$ A, Negative-Rail In, Rail-to-Rail Out, Voltage-Feedback Amplifier](#)

#### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

#### 9.4 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.  
All trademarks are the property of their respective owners.

#### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">OPA1632D</a>    | Obsolete      | Production           | SOIC (D)   8     | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | OPA<br>1632         |
| <a href="#">OPA1632DGN</a>  | Obsolete      | Production           | HVSSOP (DGN)   8 | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | 1632                |
| <a href="#">OPA1632DGNR</a> | Active        | Production           | HVSSOP (DGN)   8 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | 1632                |
| OPA1632DGNR.B               | Active        | Production           | HVSSOP (DGN)   8 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | 1632                |
| <a href="#">OPA1632DR</a>   | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | OPA<br>1632         |
| OPA1632DR.B                 | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | OPA<br>1632         |
| OPA1632DRG4                 | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | OPA<br>1632         |
| OPA1632DRG4.A               | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | OPA<br>1632         |
| OPA1632DRG4.B               | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | OPA<br>1632         |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

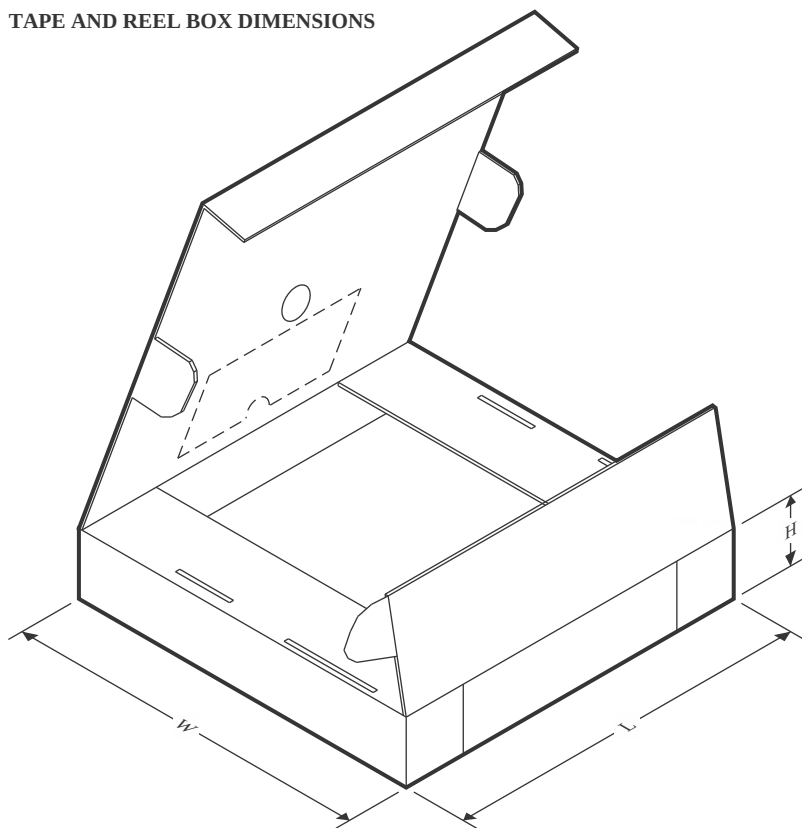
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| OPA1632DGNR | HVSSOP       | DGN             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| OPA1632DR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OPA1632DRG4 | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| OPA1632DGNR | HVSSOP       | DGN             | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| OPA1632DR   | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| OPA1632DRG4 | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |



## GENERIC PACKAGE VIEW

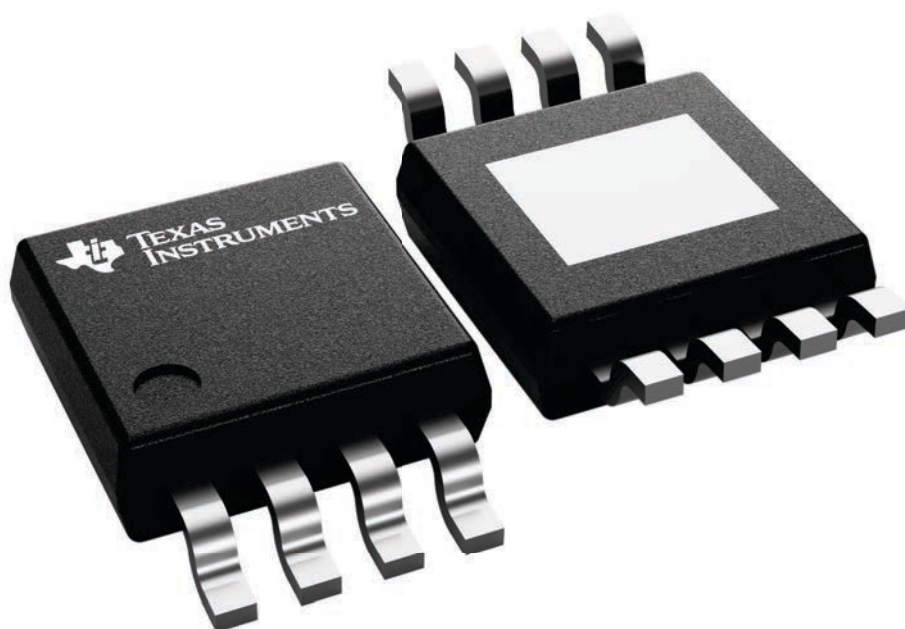
**DGN 8**

**PowerPAD™ HVSSOP - 1.1 mm max height**

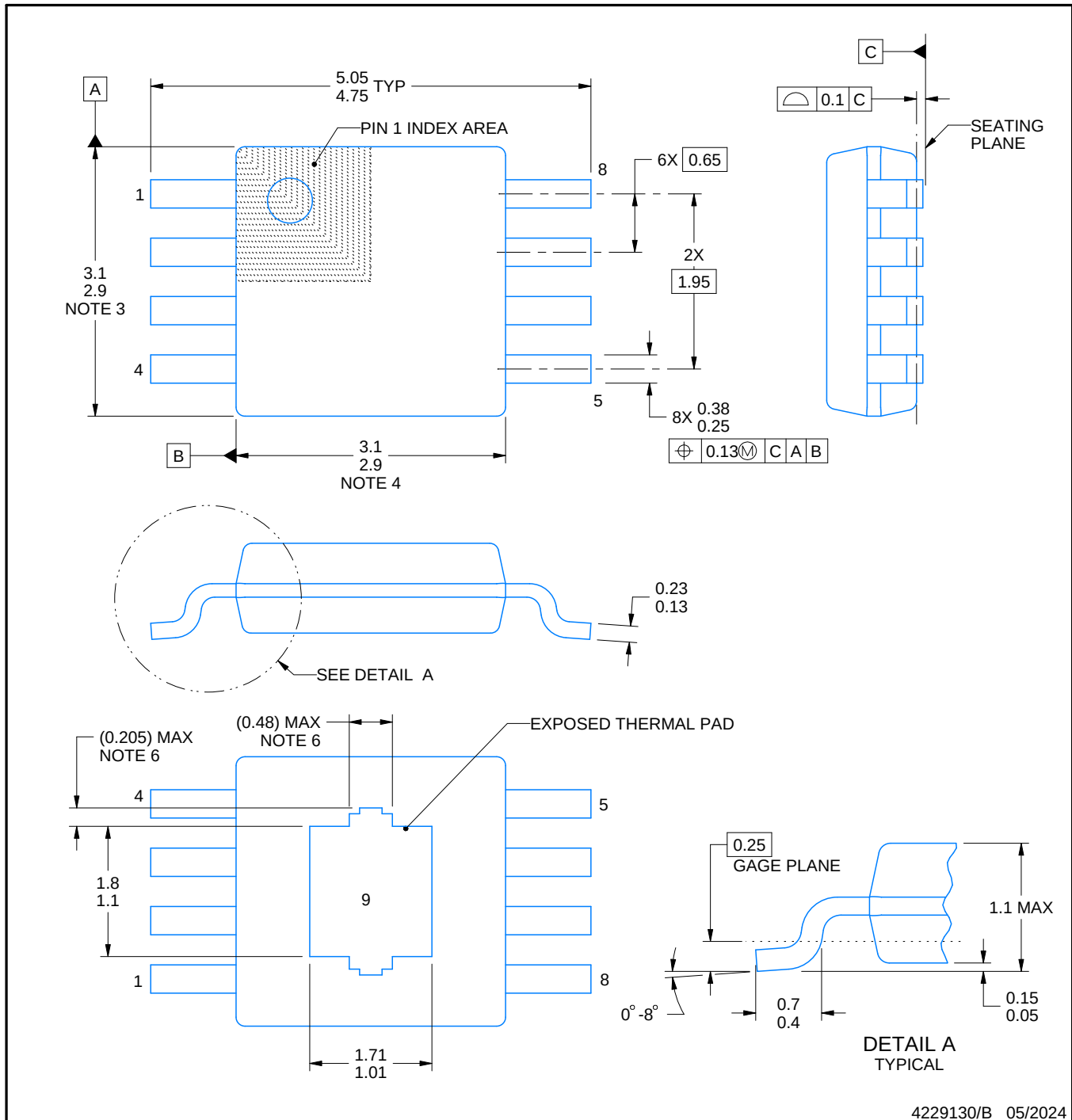
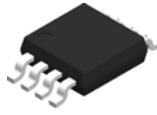
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225482/B



4229130/B 05/2024

## NOTES:

PowerPAD is a trademark of Texas Instruments.

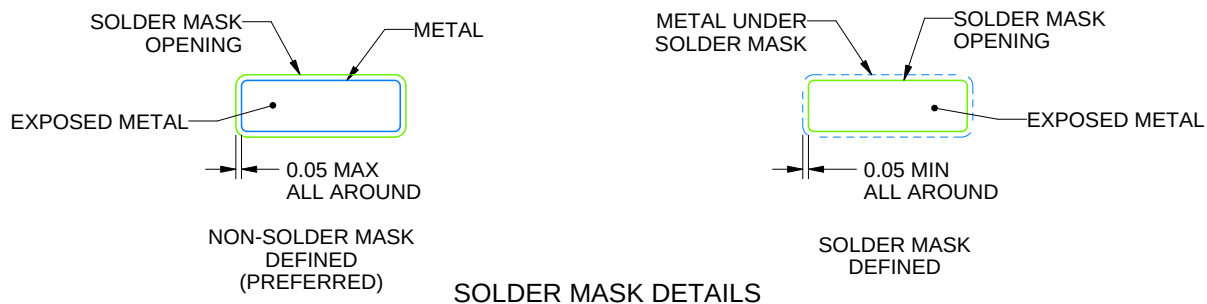
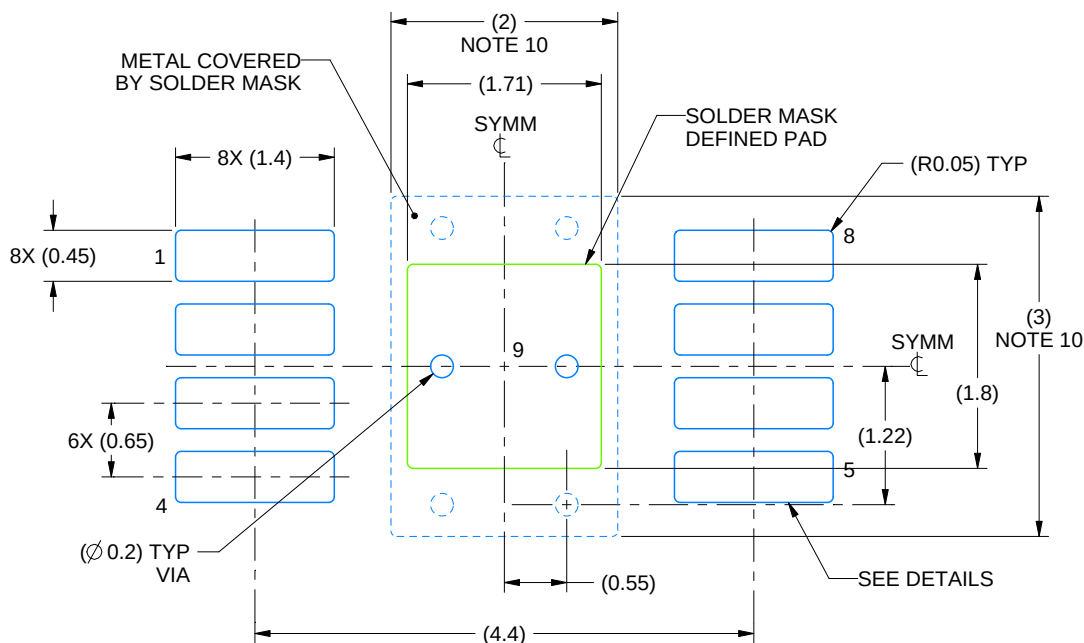
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4229130/B 05/2024

NOTES: (continued)

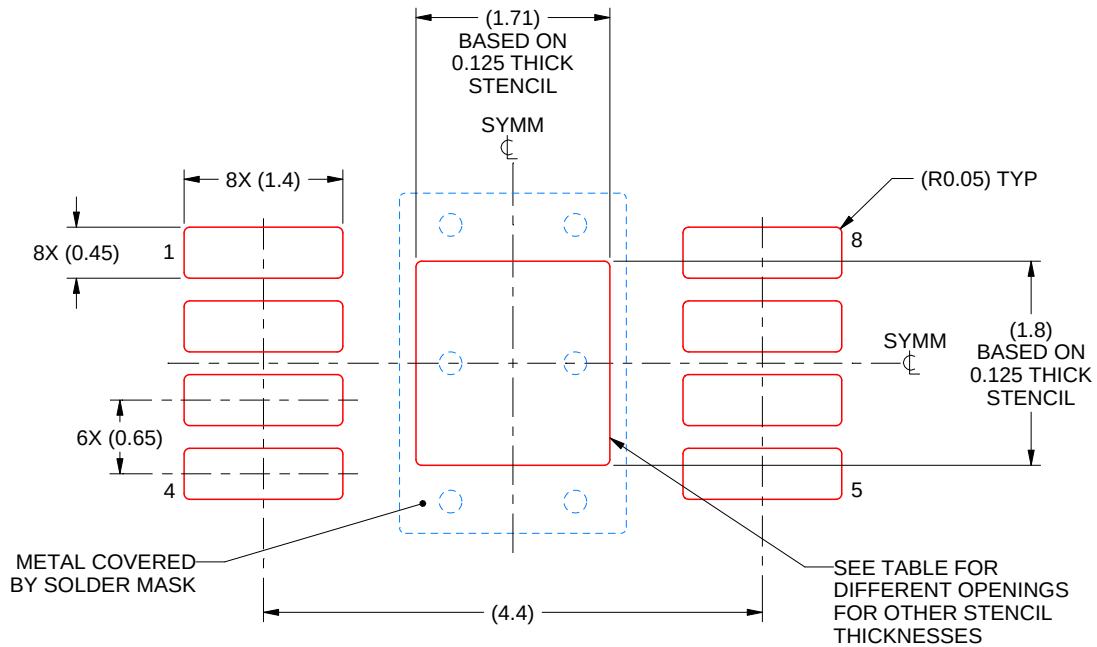
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
EXPOSED PAD 9:  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE: 15X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1               | 1.91 X 2.01            |
| 0.125             | 1.71 X 1.80 (SHOWN)    |
| 0.15              | 1.56 X 1.64            |
| 0.175             | 1.45 X 1.52            |

4229130/B 05/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



## PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

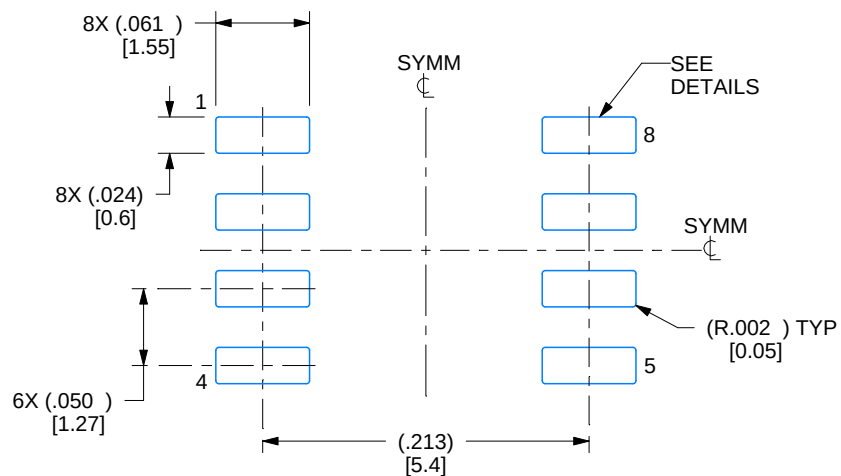


1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

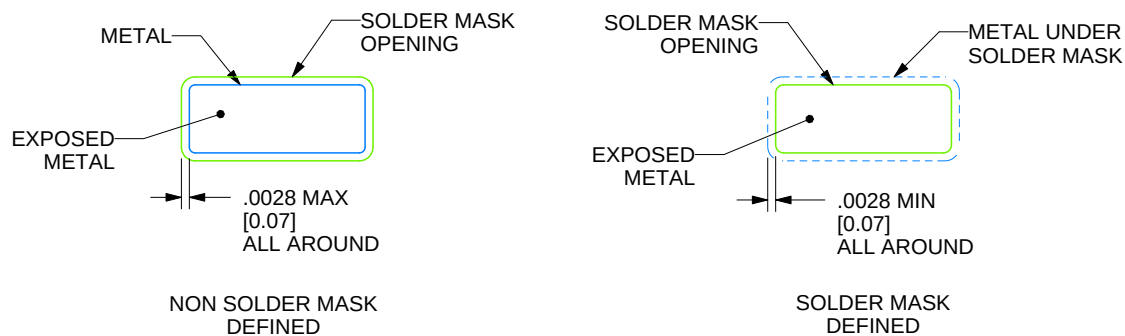
**D0008A**

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



## SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

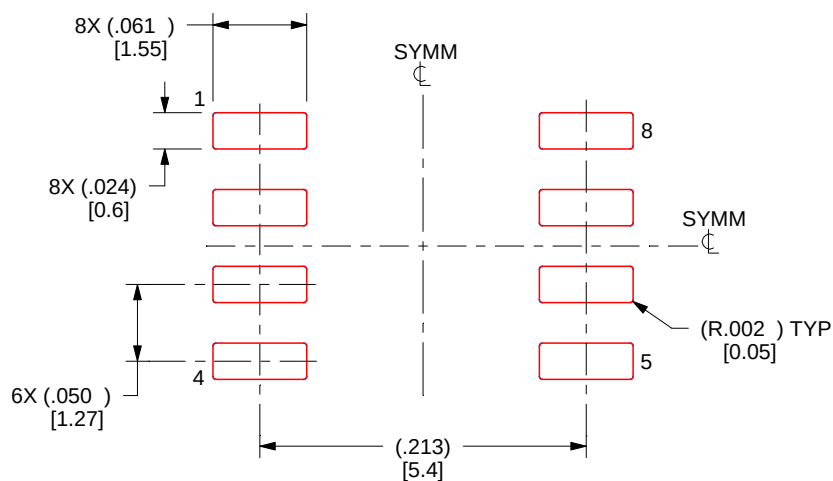
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated