

MSPM0C1105, MSPM0C1106 Mixed-Signal Microcontrollers

1 Features

Core

 Arm® 32-bit Cortex®-M0+ CPU with memory protection unit, frequency up to 32MHz

Operating characteristics

- Extended temperature: –40°C up to 125°C
- Wide supply voltage range: 1.62V to 3.6V

Memories

- Up to 64KB of flash memory
- 8KB of SRAM

High-performance analog peripherals

- 12-bit 1.6 Msps analog-to-digital converter (ADC), up to 27 external channels
- Configurable 1.4V or 2.5V internal shared voltage reference (VREF)
- Comparator (COMP) with 8-bit reference DAC
- Integrated temperature sensor

Optimized low-power modes

- RUN: 91µA/MHz (CoreMark)
- STANDBY 2µA and SRAM and registers fully retained
- SHUTDOWN: 68nA with I/O wake-up

Intelligent digital peripherals

- 3-channel DMA controller
- 7-channel event fabric signaling system
- Five timers supporting up to 18 PWM outputs, all operational down to STANDBY mode
 - One 16-bit advanced timer with deadband and the timer frequency up to 64Mhz
 - One 16-bit general purpose timer with 4 capture/compares
 - Three 16-bit general-purpose timers with 2 capture/compares
- Window-watchdog timer (WWDT)
- Independent watchdog timer (IWDT)
- RTC with alarm and calendar mode
- BEEPER generating 1/2/4/8kHz square wave to drive an external beeper

Communication interfaces

- Three UART modules, with one supporting LIN, IrDA, DALI, smart card, Manchester
- Two I²C modules supporting SMBus/PMBus and wakeup from STOP mode, supporting up to FM+ (1Mbps)
- One SPI module supporting up to 16Mbps

Clock system

- Internal 32MHz oscillator with -2.1% to 1.6% accuracy (SYSOSC)
- Internal 32kHz oscillator (LFOSC) with ±3% accuracy
- External 4MHz to 32MHz crystal oscillator (HFXT)
- External 32kHz crystal oscillator (LFXT)
- External Low Frequency (LF) and High Frequency (HF) digital clock inputs
- Digital clock output

Data integrity and encryption

Cyclic redundancy checker (CRC-16)

Flexible I/O features

- Up to 45 total GPIOs
- Two 5V-tolerant open-drain IOs

Development support

2-pin serial wire debug (SWD)

Package options 1

- 48-pin LQFP (PT), VQFN (RGZ), NFBGA (ZCM)
- 32-pin LQFP (VFC), VQFN (RHB)
- 28-pin VSSOP (DGS28)
- 24-pin VQFN (RGE)
- 20-pin WQFN (RUK), VSSOP (DGS20)

Family members (also see Device Comparison)

- MSPM0C1106: 64KB of flash, 8KB of RAM
- MSPM0C1105: 32KB of flash, 8KB of RAM
- MSP32G031C8: 64KB of flash, 8KB of RAM MSP32G031C6: 32KB of flash, 8KB of RAM
- MSP32C031C6: 32KB of flash, 8KB of RAM
- Development kits and software (also see Tools and Software)
 - LP-MSPM0C1106 LaunchPad[™] development
 - MSP Software Development Kit (SDK)

2 Applications

- Battery charging and management
- Power supplies and power delivery
- Personal electronics
- Building security and fire safety
- Connected peripherals and printers
- Grid infrastructure
- Smart metering
- Communication modules
- Medical and healthcare
- Lighting

^{1 32-}pin LQFP (VFC) and 48-pin NFBGA (ZCM) are preview

3 Description

MSPM0C1105/6 microcontrollers (MCUs) are part of MSP's highly integrated, ultra-low-power 32-bit MSPM0 MCU family based on the Arm® Cortex®-M0+ 32-bit core platform, operating at up to 32MHz frequency. These cost-optimized MCUs offer high-performance analog peripheral integration, support extended temperature ranges from -40°C to 125°C, and operate with supply voltages from 1.62V to 3.6V.

The MSPM0C1105/6 devices provide up to 64KB embedded flash program memory with 8KB SRAM. These MCUs incorporate a high-speed on-chip oscillator with an accuracy from -2.1% to +1.6%, eliminating the need for an external crystal. Additional features include a 3-channel DMA, CRC-16 accelerator, and a variety of high-performance analog peripherals such as one 12-bit 1.6 Msps ADC with VDD as the voltage reference, a comparator with 8-bit reference DAC and an on-chip temperature sensor. These devices also offer intelligent digital peripherals such as one 16-bit advanced timer with deadband and timer frequency up to 64MHz, four 16-bit general purpose timer, one windowed watchdog timer, and a variety of communication peripherals including three UART, one SPI, and two I2C. These communication peripherals offer protocol support for LIN, IrDA, DALI, Manchester, smart card, SMBus, and PMBus.

The TI MSPM0 family of low-power MCUs consists of devices with varying degrees of analog and digital integration allowing for customers to find the MCU that meets the project's needs. The MSPM0 MCU platform combines the Arm Cortex-M0+ platform with a holistic ultra-low-power system architecture, allowing system designers to increase performance while reducing energy consumption.

MSPM0C1105/6 MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get the design started quickly. Development kits include a LaunchPad available for purchase. TI also provides a free MSP Software Development Kit (SDK), which is available as a component of Code Composer Studio™ IDE desktop and cloud version within the TI Resource Explorer. MSPM0 MCUs are also supported by extensive online collateral, training with MSP Academy, and online support through the TI E2E™ support forums.

For complete module descriptions, see the MSPM0 C-Series Microcontrollers Technical Reference Manual.

PART NUMBER (1) (2) PACKAGE SIZE(3) (4) **PACKAGE** MSPM0C1106SPTR PT (LQFP, 48)⁽⁶⁾ 9mm × 9mm MSPM0C1105SPTR PT (LQFP, 48)(6) 9mm × 9mm MSPM0C1106SRGZR RGZ (VQFN, 48) 7mm × 7mm MSPM0C1105SRGZR RGZ (VQFN, 48) 7mm × 7mm 3.5mm × 3.5mm ZCM (NFBGA, 48)(5) MSPM0C1106SZCMR 3.5mm × 3.5mm ZCM (NFBGA, 48)(5) MSPM0C1105SZCMR MSPM0C1106SRHBR RHB (VQFN, 32) 5mm × 5mm MSPM0C1105SRHBR RHB (VQFN, 32) 5mm × 5mm MSPM0C1106SDGS28R DGS28 (VSSOP, 28) 7.1mm × 4.9mm MSPM0C1105SDGS28R DGS28 (VSSOP, 28) 7.1mm × 4.9mm MSPM0C1106SRGER RGE (VQFN, 24) $4mm \times 4mm$ MSPM0C1105SRGER RGE (VQFN, 24) 4mm × 4mm MSPM0C1106SDGS20R DGS20 (VSSOP. 20) 5.1mm × 4.9mm MSPM0C1105SDGS20R DGS20 (VSSOP, 20) 5.1mm × 4.9mm RUK (WQFN, 20) MSPM0C1106SRUKR 3mm × 3mm MSPM0C1105SRUKR RUK (WQFN, 20) 3mm × 3mm 9mm × 9mm MSP32C031C6SPTR PT (LQFP, 48)⁽⁶⁾ PT (LQFP, 48)(6) MSP32G031C6SPTR 9mm × 9mm MSP32G031C8SPTR PT (LQFP, 48)⁽⁶⁾ 9mm × 9mm VFC (LQFP, 32)(5) MSP32G031K6SVFCR 9mm × 9mm

Table 3-1. Package Information



Table 3-1. Package Information (continued)

PART NUMBER (1) (2)	PACKAGE	PACKAGE SIZE ⁽³⁾ (4)
MSP32C031K6SVFCR	VFC (LQFP, 32) ⁽⁵⁾	9mm × 9mm
MSP32G031K8SVFCR	VFC (LQFP, 32) ⁽⁵⁾	9mm × 9mm

- (1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum*, or see the TI website.
- (2) Please find more infromation about the device name in the Device Nomenclature section.
- (3) For more information, see Mechanical, Packaging, and Orderable Information.
- (4) The package size (length × width) is a nominal value and includes pins, where applicable.
- (5) 32-pin LQFP (VFC) and 48-pin NFBGA (ZCM) are preview.
- (6) There are two pin configurations for the PT (LQFP, 48) package. Refer to Section 6.2 for more information.

CAUTION

System-level ESD protection must be applied in compliance with the device-level ESD specification to prevent electrical overstress or disturbing of data or code memory. See *MSP430™ System-Level ESD Considerations* for more information. The principles in this application note are applicable to MSPM0 MCUs.



4 Functional Block Diagram

Figure 4-1 shows the functional block diagram.

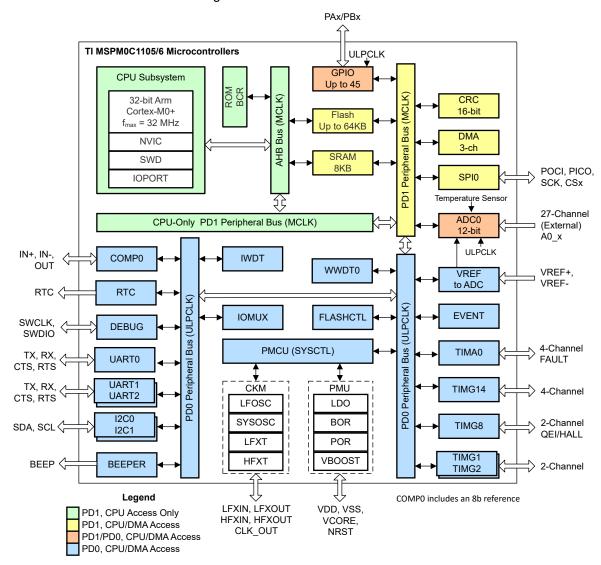


Figure 4-1. MSPM0C1105/6 Functional Block Diagram



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5 Device Comparison

Table 5-1. Device Comparison Table

				Compani		_		
DEVICE NAME (1)	FLASH / SRAM (KB)	ADC CHANNEL	UART / I2C / SPI	TIMG	TIMA	GPIO	COMP	PACKAGE (2)
MSPM0C1106SPTR	64 / 8	27	3 /2 / 1	4	1	45	1	48 LQFP
MSPM0C1105SPTR	32 / 8	21	3/2/1	4	1	45	1	(9mm × 9mm)
MSPM0C1106SRGZR	64 / 8	27	3 /2 / 1	4	1	45	1	48 VQFN
MSPM0C1105SRGZR (3)	32 / 8	21	3/2/1	4	'	45	'	(7mm × 7mm)
MSPM0C1106SZCMR (3)	64 / 8	27	3 /2 / 1	4	1	45	1	48 NFBGA
MSPM0C1105SZCMR (3)	32 / 8	21	3/2/1	4	'	45	'	(3.5mm × 3.5mm)
MSPM0C1106SRHBR	64 / 8	18	3 /2 / 1	4	1	29	1	32 VQFN
MSPM0C1105SRHBR	32 / 8	10	3/2/1	4	'	29	'	(5mm × 5mm)
MSPM0C1106SDGS28R	64 / 8	15	3 /2 / 1	4	1	25	1	28 VSSOP
MSPM0C1105SDGS28R	32 / 8	13	37271	-	'	25	'	(7.1mm × 4.9mm)
MSPM0C1106SRGER	64 / 8	13	3 /2 / 1	4	1	21	1	24 VQFN
MSPM0C1105SRGER	32 / 8	13	37271	-	'	21	'	(4mm × 4mm)
MSPM0C1106SDGS20R	64 / 8	12	3 /2 / 1	4	1	17	1	20 VSSOP
MSPM0C1105SDGS20R	32 / 8	12	3/2/1	4	'	17	'	(5.1mm × 4.9mm)
MSPM0C1106SRUKR	64 / 8	12	3 /2 / 1	4	1	17	1	20 WQFN
MSPM0C1105SRUKR	32 / 8	12	3/2/1	4	'	17	'	(3mm × 3mm)
MSP32C031C6SPTR	32 / 8							401.055
MSP32G031C6SPTR	32 / 8	27	3 /2 / 1	4	1	45	1	48 LQFP (9mm × 9mm)
MSP32G031C8SPTR	64 / 8							(3)
MSP32G031K6SVFCR (3)	32 / 8							001.055
MSP32C031K6SVFCR (3)	32 / 8	18	3 /2 / 1	4	1	29	1	32 LQFP (9mm × 9mm)
MSP32G031K8SVFCR (3)	64 / 8							(3)

⁽¹⁾ For the most current part, package, and ordering information for all available devices, see the Package Option Addendum, or see the TI website.

The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data*. 32-pin LQFP (VFC) and 48-pin NFBGA (ZCM) are preview



6 Pin Configuration and Functions

The System Configuration tool provides a graphical interface to enable, configurable, and generate initialization code for pin multiplexing and simplifying pin settings. The pin diagrams shown in the data sheet show the primary peripheral functions, some of the integrated device features, and available clock signals to simplify the device pinout.

For full descriptions of the pin functions, see the Pin Attributes and Signal Descriptions sections.

6.1 Pin Diagrams

Note

For full pin configuration and functions for each package option, refer to Pin Attributes and Signal Descriptions.

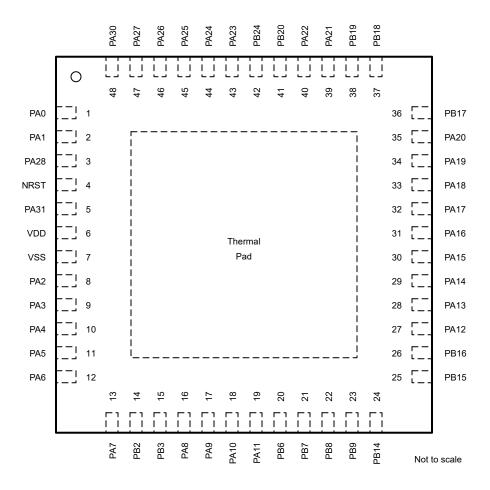


Figure 6-1. 48-pin RGZ (VQFN) Package



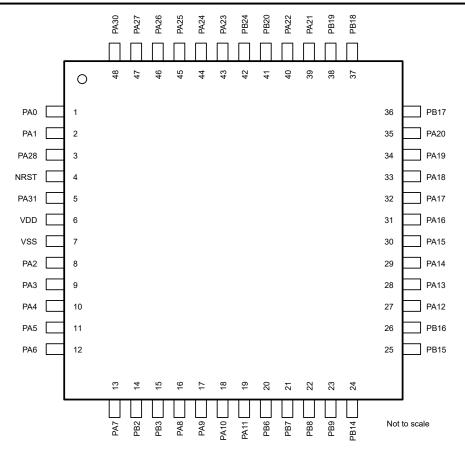


Figure 6-2. 48-pin PT (A) 48-pin PT (LQFP) Package

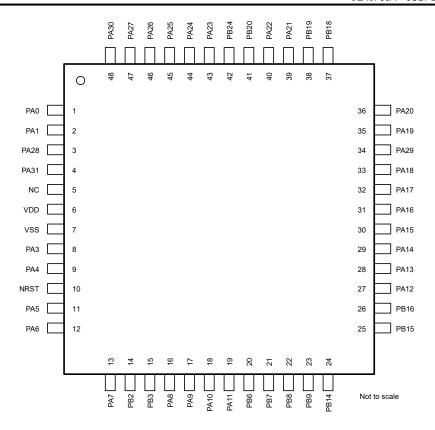


Figure 6-3. 48-pin PT (B) (LQFP) Package



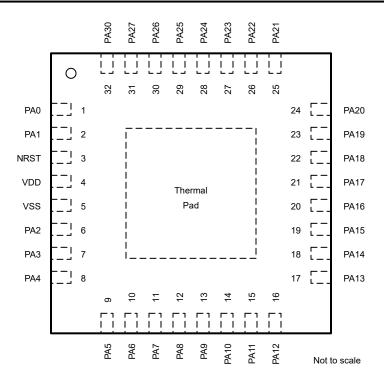


Figure 6-4. 32-pin RHB (VQFN) Package

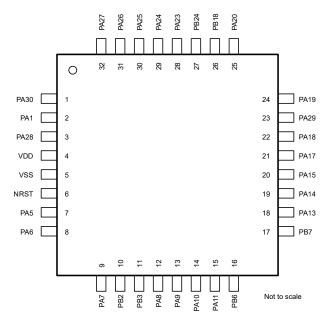


Figure 6-5. 32-pin VFC (LQFP)



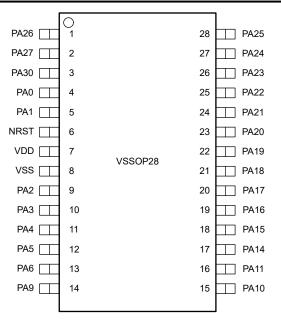


Figure 6-6. 28-pin DGS28 (VSSOP)

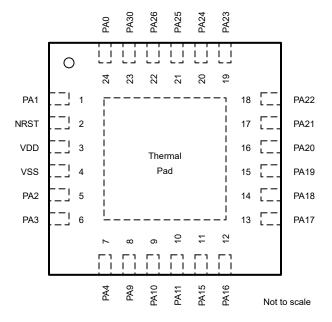


Figure 6-7. 24-pin RGE (VQFN) Package



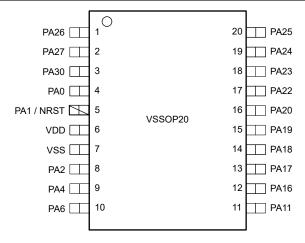


Figure 6-8. 20-pin DGS20 (VSSOP)

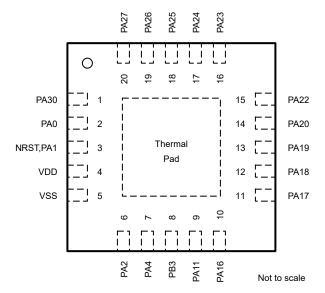


Figure 6-9. 20-pin RUK (WQFN)



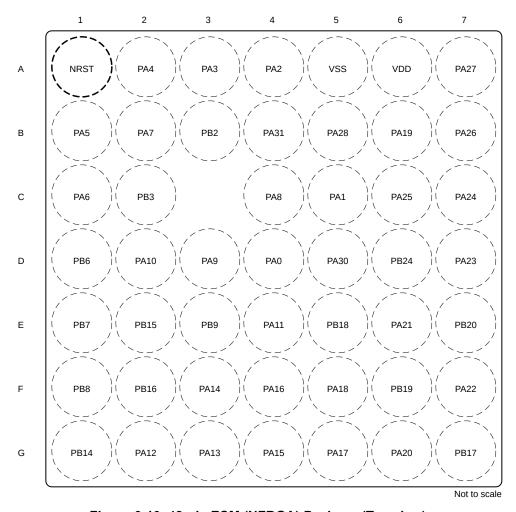


Figure 6-10. 48-pin ZCM (NFBGA) Package (Top view)



6.2 Pin Attributes

The following table describes the functions available on every pin for each device package.

Note

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) that lets users configure the desired *Pin Function* using the PINCM.PF control bits.

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) which allows users to configure the desired Pin Function using the PINCM.PF control bits. The IOMUX only supports connecting one IOMUX-managed digital function to the pin at the same time. The PINCM.PF and PINCM.PC in IOMUX are recommended to be set to 0 when non-IOMUX managed functions (such as analog connections) are intended to be used on a pin. However, non-IOMUX managed signals (such as analog inputs and WAKE inputs) can be enabled on a pin at the same time that an IOMUX managed digital function is enabled on the pin, provided there is no contention between the functions. In this case, the designer must verify that no contention exists between the functions enabled on each pin.

Table 6-1. Digital IO Features by IO Type

BUFFER TYPE	INVERSION CONTROL	DRIVE STRENGTH CONTROL	HYSTERESIS CONTROL	PULLUP RESISTOR	PULLDOWN RESISTOR	WAKEUP LOGIC
SDIO (standard drive)	Υ			Υ	Υ	
SDIO (standard drive) with wake1	Y			Υ	Y	Υ
ODIO (5V-tolerant open drain)	Y		Y		Y	Υ

1. Standard with Wake allows the I/O to wake up the device from the lowest low-power mode of SHUTDOWN. All I/O can be configured to wakeup the MCU from higher low-power modes. See section *GPIO FastWake* in the MSPM0 C-Series Microcontrollers Technical Reference Manual for details.

Note

There are two pin configurations for the 48 LQFP (PT) package denoted as PT (A) and PT (B). The following devices correspond to these respective configurations:

- PT (A): MSPM0C1105SPTR, & MSPM0C1106SPTR
- PT (B): MSP32C031C6SPTR, MSP32G031C6SPTR, & MSP32G031C8SPTR

Table 6-2. Pin Attributes (PT (A), ZCM, VFC, PT (B), RGZ, RHB, DGS28, RGE, DGS20, RUK Packages)

PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
4	A1	6	10	4	3	6	2	5	3	NRST	NRST	(Non-IOMUX 1) 0	RESET	RESET
											PA0	1	10	
											UART0_TX	2	0	
											I2C0_SDA	3	IOD	
											TIMA0_C0	4	10	
										PA0	TIMA_FAL1	5	I	ODIO
1	D4		1	1	1	4	24	4	2	PINCM1	FCC_IN	6	I	(5V-
'			·					·	_	0x40428000	TIMG8_C1	7	10	tol)with wake
											BEEP	8	0	
											TIMG14_C0	9	10	
											SPI0_CS1_MIS O1	10	Ю	
											RTC_OUT	12	0	



									unue					
PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
											PA1	1	10	
											UART0_RX	2	Ю	1
											I2C0_SCL	3	IOD	1
											TIMA0_C1	4	Ю	1
											TIMA_FAL2	5	I	1
										PA1	TIMG8_IDX	6	I	ODIO
2	C5	2	2	2	2	5	1	5	3	PINCM2	TIMG8_C0	7	Ю	(5V-
-	00	_	_	_	_		•			0x40428004	TIMG14_C1	9	Ю	tol)with wake
											SPI0_CS3_CD _MISO3	10	Ю	
											HFCLKIN	11	I	1
											UART0_TX	12	0	1
											UART1_RTS	13	0	1
											I2C0_SDA	14	IOD	1
											PA2	1	Ю	
											TIMG8_C1	2	Ю	1
									SPI0_CS0	3	Ю	1		
											TIMG2_C1	4	Ю	1
										PA2	TIMG8_IDX	5	I	SDIO
8	A4			8	6	9	5	8	6	PINCM5	TIMA0_C3N	6	0	(standar
										0x40428010	TIMA0_C2N	7	0	d)
											TIMA_FAL0	8	I	
											TIMA_FAL1	9	I	
											TIMA0_C0	11	Ю	
											I2C0_SCL	12	IOD	
											PA3	1	10	
											TIMG8_C0	2	10	
											SPI0_CS1_MIS O1	3	Ю	
											I2C1_SDA	4	IOD	1
											TIMA0_C1	5	Ю	1
										DAG	TIMG2_C0	7	Ю	1
9	А3		8	9	7	10	6			PA3	TIMA0_C2	8	Ю	SDIO (standar
3	AU			9	,	10	0			PINCM6 0x40428014	UART2_CTS	9	I	d)
											UART1_TX	10	0	1
											SPI0_CS3_CD _MISO3	11	Ю	
											I2C0_SDA	12	IOD	1
											COMP0_OUT	14	0	1
								LFXIN	(Non-IOMUX 1)	Α				



					1			(COII	tinue	u)				
PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
											PA4	1	10	
											TIMG8_C1	2	10	
											SPI0_POCI	3	Ю	
											I2C1_SCL	4	IOD	
											TIMA0_C1N	5	0	
											LFCLKIN	6	ı	
										PA4	TIMG2_C1	7	10	SDIO
10	A2		9	10	8	11	7	9	7	PINCM7	TIMA0_C3	8	Ю	(standar
										0x40428018	UART2_RTS	9	0	- d)
											UART1_RX	10	I	
											SPI0_CS0	11	Ю	
											TIMA0_C0N	12	0	
											HFCLKIN	13	I	
											LFXOUT	(Non-IOMUX 1)	Α	
											PA5	1	Ю	
											TIMG8_C0	2	Ю	
											SPI0_PICO	3	Ю	
											I2C1_SDA	4	IOD	
											TIMG14_C0	5	Ю	
										PA5	FCC_IN	6	I	SDIO
11	B1	7	11	11	9	12				PINCM8	TIMG1_C0	7	Ю	(standar
				••							0x4042801c	TIMA_FAL1	8	I
											UARTO_CTS	9	I	
											UART1_TX	11	0	
											TIMA0_C1	12	Ю	
											HFXIN	(Non-IOMUX 1)	Α	
											PA6	1	Ю	
											TIMG8_C1	2	10	
											SPI0_SCLK	3	IOD	
											I2C1_SCL	4	IOD	
											TIMG14_C1	5	Ю	1
											HFCLKIN	6	I	
										DAG	TIMG1_C1	7	Ю	
12	C1	8	12	12	10	13		10		PA6	TIMA_FAL0	8	I	SDIO (standar
'-			'-		.0	.5		.0		PINCM9 0x40428020	UARTO_RTS	9	0	d)
										TIMA0_C2N	10	0	1	
											UART1_RX	11	I	1
											TIMA0_C2	12	Ю	1
											I2C0_SDA	13	IOD	1
											BEEP	14	0	1
											HFXOUT	(Non-IOMUX 1)	Α	



									tinue	1				
PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
											PA7	1	Ю	
											CLK_OUT	2	0	
											TIMG8_C0	3	Ю	
											TIMA0_C2	4	Ю	
											TIMG8_IDX	5	I	
											TIMG2_C1	6	Ю	
										PA7	TIMA0_C1	7	Ю	SDIO
13	B2	9	13	13	11					PINCM10 0x40428024	SPI0_CS2_MIS O2	8	Ю	(standar d)
											FCC_IN	9	ı	1
											SPI0_POCI	10	Ю	1
											SPI0_PICO	11	Ю	1
											UART1_TX	12	0	1
											TIMG1_C0	13	10	1
											COMP0_OUT	14	0	1
											PA8	1	Ю	
											UART1_TX	2	0	1
								SPI0_CS0	3	10	1			
											I2C0_SDA	4	IOD	1
											TIMA0_C0	5	Ю	-
											TIMA_FAL2	6	1	1
			16							PA8	TIMA_FAL0	7	1	SDIO
16	C4	12		16	12					PINCM13 0x40428030	SPI0_CS3_CD _MISO3	8	Ю	(standar d)
											TIMG2_C1	9	Ю	
											HFCLKIN	10	ı	
											UART0_RTS	11	0	
											SPI0_SCLK	12	IOD	
											UART1_RX	13	ı	
											TIMA0_C3N	14	0	1
											PA9	1	Ю	
											UART1_RX	2	ı	
											SPI0_PICO	3	Ю	
											I2C0_SCL	4	IOD	
											TIMA0_C0N	5	0	
	17 D3									PA9	CLK_OUT	6	0	SDIO
17		13	17	17	13	14	8			PINCM14	TIMA0_C1	7	Ю	(standar
										0x40428034	RTC_OUT	8	0	d)
											TIMG2_C0	9	Ю]
											SPI0_POCI	10	Ю	
											UART0_CTS	11	I]
											TIMA_FAL1	12	I]
											TIMG1_C1	13	Ю]



								(COII	tinue	u)				
PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
											PA10	1	10	
											UART0_TX	2	0	
											SPI0_POCI	3	10	
											I2C0_SDA	4	IOD	
											TIMA0_C2	5	10	
										PA10	CLK_OUT	6	0	SDIO
18	D2	14	18	18	14	15	9			PINCM15	TIMG14_C0	7	10	(standar d)with
										0x40428038	I2C1_SDA	8	IOD	wake
											TIMA_FAL1	10	I	1
											TIMG2_C1	11	10	1
											TIMA0_C1N	12	0	1
											TIMG8_C1	13	Ю	
											SPI0_PICO	14	Ю	
											PA11	1	Ю	
											UART0_RX	2	Ю	
											SPI0_SCLK	3	IOD	
								12C0_SCL	4	IOD				
											TIMA0_C2N	5	0	
											UART1_RX	6	I	1
			15 19							PA11	TIMG14_C1	7	Ю	SDIO (standar
19	E4	15		19	15	16	10	11	9	PINCM16 0x4042803c	I2C1_SCL	8	IOD	d)with
										0X40428030	TIMA_FAL0	10	I	wake
											SPI0_CS0	12	Ю	
											COMP0_OUT	14	0	
											ADC0_25	(Non-IOMUX 1) 0	А	
											COMP0_DAC_ OUT	(Non-IOMUX 2)	А	
											PA12	1	Ю	
											SPI0_SCLK	2	IOD	1
											TIMA0_C3	4	Ю	1
											FCC_IN	5	I	1
											TIMG14_C0	6	10	
										PA12	SPI0_CS1_MIS O1	8	10	SDIO
27	G2		27	27	16					PINCM24	UART2_CTS	9	I	(standar
	21 G2									0x4042805c	UART1_CTS	10	I	d)
										TIMA0_C3N	11	0	1	
											I2C1_SCL	12	IOD	1
											TIMG2_C1	13	10	1
											COMP0_OUT	14	0	1
											ADC0_18	(Non-IOMUX 1)	А	



								(0011	tinue	u <i>j</i>				
PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
											PA13	1	Ю	
											UART0_RX	2	Ю	
											SPI0_POCI	3	Ю	
											TIMA0_C2N	4	0	
											TIMA0_C3N	5	0	
											RTC_OUT	6	0	
											TIMG14_C1	7	Ю	
											TIMG14_C3	8	Ю	
28	G3	18	28	28	17					PA13 PINCM25	SPI0_CS3_CD _MISO3	9	Ю	SDIO (standar
										0x40428060	UART2_TX	10	0	- d)
											UART1_RTS	11	0	
											SPI0_CS0	12	Ю	
											TIMG8_C1	13	Ю	
											TIMA0_C1	14	Ю	
											ADC0_17	(Non-IOMUX 1) 0	Α	
											COMP0_IN2-	(Non-IOMUX 2) 0	Α	
								PA14	1	Ю				
											UART0_CTS	2	I	
											SPI0_PICO	3	Ю	
											TIMG1_C0	4	Ю	
											CLK_OUT	6	0	
										PA14	SPI0_CS2_MIS O2	9	Ю	SDIO
29	F3	19	29	29	18	17				PINCM26	UART2_RX	10	I	(standar d)
										0x40428064	I2C0_SCL	12	IOD] u)
											UART0_TX	13	0	
											TIMA0_C2	14	Ю	
											ADC0_16	(Non-IOMUX 1) 0	Α	
											COMP0_IN2+	(Non-IOMUX 2) 0	Α	
											PA15	1	Ю	
											UART0_RTS	2	0	
										SPI0_CS2_MIS O2	3	Ю		
											I2C1_SCL	4	IOD	
										PA15	TIMA0_C2	5	Ю	SDIO
30	G4	20	30	30	19	18	11			PINCM27	TIMG8_IDX	7	I	(standar d)
										0x40428068	UART2_RTS	10	0] ",
											TIMG14_C1	12	Ю	
											ADC0_15	(Non-IOMUX 1) 0	Α	
							COMP0_IN3+	(Non-IOMUX 2) 0	А					



DT (A)	7014	VEO	DT (D)	P07	DUD	DGS2	POF	DGS2	tinue	PIN NAME/	CICNAL	IOMIN	SICNAL	DUEEEE	
PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	8 PIN	RGE PIN	0 PIN	RUK PIN	IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE	
											PA16	1	10		
											SPI0_POCI	3	10		
											I2C1_SDA	4	IOD		
										PA16	TIMA0_C2N	5	0	SDIO	
31	F4		31	31	20	19	12	12	10	PINCM28	FCC_IN	7	I	(standar	
										0x4042806c	UART2_CTS	10	I	d)	
											TIMG14_C2	12	10	_	
											COMP0_OUT	14	0		
											ADC0_14	(Non-IOMUX 1) 0	А		
											PA17	1	10	_	
											UART1_TX	2	0	_	
											TIMA0_C2	3	10		
											I2C1_SCL	4	IOD		
											TIMA0_C3	5	10		
											TIMG2_C0	6	IO	-	
										PA17	TIMG8_C0	7	10	SDIO	
32	G5	21	32	32	21	20	13	13	11	PINCM29	TIMA0_C0N	8	0	(standar	
										0x40428070	SPI0_CS1_MIS O1	9	Ю	d)	
											SPI0_SCLK	10	IOD		
											I2C0_SDA	11	IOD		
												UART0_RX	12	10	
												ADC0_13	(Non-IOMUX 1) 0	A	
											COMP0_IN1-	(Non-IOMUX 2) 0	A		
											PA18	1	10		
											UART1_RX	2	I		
											UART1_RTS	3	0		
											I2C1_SDA	4	IOD		
											TIMA0_C3N	5	0		
											TIMG2_C1	6	10		
											TIMG8_C1	7	10		
											SPI0_PICO	8	10		
										PA18	SPI0_CS0	9	10	SDIO	
33	F5	22	33	33	22	21	14	14	12	PINCM30	TIMA0_C1N	10	0	(standar d)	
										0x40428074	TIMA0_C0	11	10] u)	
											SPI0_POCI	12	10		
											TIMA_FAL2	13	I		
											CLK_OUT	14	0		
											ADC0_12	(Non-IOMUX 1) 0	А		
											COMP0_IN1+	(Non-IOMUX 2) 0	А		
										Table 6-4	(Non-IOMUX 2)	I			



PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
											PA19	1	Ю	
											SWDIO	2	IO	
											SPI0_SCLK	3	IOD	1
											I2C1_SDA	4	IOD	1
										DA40	TIMA0_C2	5	Ю	
34	В6	24	35	34	23	22	15	15	13	PA19 PINCM32	TIMG14_C0	6	Ю	SDIO (standar
	20			0.						0x4042807c	SPI0_POCI	7	Ю	d)
											UART0_CTS	8	I	
											UART1_RX	11	I	
											SPI0_PICO	13	Ю	
											ADC0_22	(Non-IOMUX 1) 0	Α	
											PA20	1	Ю	
											SWCLK	2	1	
											TIMA_FAL1	3	1	
											I2C1_SCL	4	IOD	
											TIMA0_C2N	5	0	
										PA20	TIMG14_C1	6	Ю	
35	G6	25	36	35	24	23	16	16	14	PINCM33	SPI0_PICO	7	Ю	SDIO (standar
										0x40428080	TIMA0_C0	8	Ю	` d)
											UART0_RTS	10	0	
											UART1_TX	11	0	
											SPI0_CS0	12	Ю	
											UART1_RX	13	1	
											ADC0_4	(Non-IOMUX 1) 0	Α	
											PA21	1	Ю	
											UART2_TX	2	0	
											SPI0_CS3_CD _MISO3	3	Ю	
											UART1_CTS	4	1	
											TIMA0_C0	5	Ю	
										PA21	TIMG1_C0	6	Ю	SDIO
39	E6		39	39	25	24	17			PINCM37	UART2_CTS	8	1	(standar d)
										0x40428090	TIMG8_C0	10	Ю] ",
											TIMA0_C0N	12	0	
											UART2_RX	13	1	
											ADC0_8	(Non-IOMUX 1) 0	Α	
											ADC0_VREF-	(Non-IOMUX 2) 0	Α	



								(COII	tinue	u <i>j</i>				
PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
											PA22	1	Ю	
											UART2_RX	2	1	
											SPI0_CS2_MIS O2	3	Ю	
											UART1_RTS	4	0	
											TIMA0_C0N	5	0	
											TIMG1_C1	6	Ю	
										PA22	TIMA0_C1	7	Ю	SDIO
40	F7		40	40	26	25	18	17	15	PINCM38 0x40428094	CLK_OUT	8	0	(standar d)
										0X40428094	I2C0_SCL	9	IOD	,
											TIMG8_C1	10	Ю	
											UART1_RX	11	Į	
											SPI0_POCI	12	Ю	
											UART2_TX	13	0	
											ADC0_7	(Non-IOMUX 1)	Α	
											PA23	1	Ю	
										UART2_TX	2	0		
											SPI0_CS3_CD _MISO3	3	Ю	
											TIMA0_C3	5	Ю	
											TIMG8_C0	6	Ю	
										PA23	TIMG2_C0	7	Ю	SDIO
43	D7	28	43	43	27	26	19	18	16	PINCM41	UART0_TX	8	0	(standar d)
										0x404280a0	TIMG14_C0	9	Ю	u)
											SPI0_POCI	12	Ю	
											UART0_CTS	13	I	
											ADC0_26	(Non-IOMUX 1) 0	Α	
											ADC0_VREF+	(Non-IOMUX 2) 0	Α	
											PA24	1	Ю	
											UART2_RX	2	1	
											SPI0_CS2_MIS O2	3	Ю	
											UART0_RTS	4	0	
										D	TIMA0_C3N	5	0	
44	C7 29 4	44	44	28	27	20	19	17	PA24	TIMG8_C1	6	Ю	SDIO (standar	
	0,	23			20		20	13	''	PINCM42 0x404280a4	TIMG2_C1	7	Ю	d)
											UART1_RX	8	I	
											TIMG14_C1	9	Ю	
											SPI0_PICO	12	Ю	
											I2C0_SDA	13	IOD	
											ADC0_3	(Non-IOMUX 1) 0	Α	



PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
											PA25	1	Ю	
											SPI0_PICO	2	10	
											SPI0_POCI	3	Ю	
											SPI0_SCLK	4	IOD	
											TIMA0_C3	5	Ю	
											TIMA0_C1N	6	0	
										PA25	TIMA0_C2	7	Ю	
45	C6	30	45	45	29	28	21	20	18	PINCM43	UART2_CTS	8	1	SDIO (standar
										0x404280a8	TIMG14_C0	9	Ю) d)
											TIMG1_C0	10	Ю	
											I2C0_SDA	11	IOD	
											UART0_TX	12	0	
											TIMA_FAL2	13	I	
											I2C0_SCL	14	IOD	
											ADC0_2	(Non-IOMUX 1) 0	Α	
											PA26	1	Ю	
											BEEP	2	0	
											SPI0_POCI	3	Ю	
											TIMG8_C0	4	Ю	
											TIMA_FAL0	5	I	
											TIMA0_C3N	6	0	
											TIMG2_C0	7	Ю	
										PA26	UART2_RTS	8	0	SDIO
46	В7	31	46	46	30	1	22	1	19	PINCM44	I2C0_SCL	9	IOD	(standar
										0x404280ac	TIMG1_C1	10	Ю	d)
											UART0_RX	11	Ю	
											TIMA0_C0	12	Ю	
										I2C0_SDA	13	IOD		
									UART1_CTS	14	I			
											ADC0_1	(Non-IOMUX 1) 0	Α	
											COMP0_IN0+	(Non-IOMUX 2) 0	Α	



						DGS2		DGS2	tinue	PIN NAME/				
PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	8 PIN	RGE PIN	0 PIN	RUK PIN	IOMUX REG/	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
											PA27	1	10	
											SPI0_CS3_CD _MISO3	2	Ю	
											TIMA0_C0N	3	0	
											TIMG8_C1	4	10	
											TIMA_FAL2	5	I	
											CLK_OUT	6	0	
										PA27	TIMG2_C1	7	Ю]
47	A7	32	47	47	31	2		2	20	PINCM45	RTC_OUT	8	0	SDIO (standar
		02		•••		_		_		0x404280b0	UART1_CTS	9	I	d)
											I2C0_SCL	10	IOD	
											UART0_TX	11	0	
											SPI0_POCI	12	Ю	
											COMP0_OUT	14	0	
											ADC0_0	(Non-IOMUX 1) 0	А	
											COMP0_IN0-	(Non-IOMUX 2) 0	А	
											PA28	1	10	
											UART0_TX	2	0	
										PA28	I2C0_SDA	3	IOD	SDIO
3	B5	3	3	3						PINCM3	TIMA0_C3	4	10	(standar
										0x40428008	TIMA_FAL0	5	Ţ	d)
											TIMG2_C0	6	Ю	
											TIMA0_C1	7	Ю	
										PA29	PA29	1	Ю	SDIO
		23	34							PINCM31	UART0_RTS	2	0	(standar
										0x40428078	SPI0_PICO	3	Ю	d)
											PA30	1	Ю	
											UART0_RX	4	Ю	
											TIMG8_IDX	5	1	
48	D5	1	48	48	32	3	23	3	1	PA30	TIMA0_C0	6	Ю	SDIO (standar
40	Do	'	40	40	32	3	20		'	PINCM46 0x404280b4	UART1_RTS	9	0	d)
											TIMG2_C1	10	Ю	
											TIMG14_C2	11	Ю	
											I2C0_SDA	12	IOD	
											PA31	1	Ю	
										PA31	UART0_RX	2	Ю	SDIO
5	B4		4	5						PINCM4	I2C0_SCL	3	IOD	(standar
										0x4042800c	TIMA0_C3N	4	0	d)
											CLK_OUT	6	0	



DT (A)	70M	VFC	DT (B)	DC7	RHB	DGS2	RGE	DGS2	RUK	PIN NAME/	SIGNAL	IOMUX	SICNAL	BUEEED
PT (A) PIN	ZCM PIN	PIN	PT (B) PIN	RGZ PIN	PIN	8 PIN	PIN	0 PIN	PIN	IOMUX REG/ IOMUX ADDR	NAME	PF	SIGNAL	BUFFER TYPE
											PB2	1	10	
											UART2_CTS	3	I	
											I2C1_SCL	4	IOD	
											TIMA0_C3	5	10	
										PB2	UART1_CTS	6	I	SDIO
14	В3	10	14	14						PINCM11	TIMG1_C0	7	10	(standar
										0x40428028	UART2_TX	8	0	d)
											HFCLKIN	10	I	
											SPI0_PICO	11	10	
											UART1_RX	12	I	
											TIMA0_C1N	13	0	
											PB3	1	10	
											TIMA_FAL0	2	I	
											UART2_RTS	3	0	
											I2C1_SDA	4	IOD	
								TIMA0_C3N	5	0				
								PB3	UART1_RTS	6	0			
15	C2	11	15	15					8	PINCM12	TIMG1_C1	7	10	SDIO (standar
	02									0x4042802c	UART2_RX	8	I	d)
											TIMG2_C1	9	10	
											TIMA0_C0	10	10	
											SPI0_SCLK	11	IOD	
											SPI0_CS0	12	10	
											UART1_TX	13	0	
											RTC_OUT	14	0	
											PB6	1	10	
											UART1_TX	2	0	
											TIMG8_C0	5	10	
											UART2_CTS	6	I	
											TIMG1_C0	7	10	
	0 D1 16 2								PB6	TIMA_FAL2	8	I	SDIO	
20		16	20	20						PINCM17 0x40428040	SPI0_CS1_MIS O1	9	10	(standar d)
										TIMA0_C3N	11	0		
										TIMG8_C1	12	10		
										TIMA0_C2N	13	0		
										UART0_TX	14 (Non-IOMUX 1)	0		
											ADC0_24	0	A	



								(COII	tinue	u)				
PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
											PB7	1	10	
											UART1_RX	2	I	1
											TIMG8_C1	5	10	1
											UART2_RTS	6	0	1
										PB7	TIMG1_C1	7	10	0010
21	E1	17	21	21						PINCM18 0x40428044	SPI0_CS2_MIS O2	9	Ю	SDIO (standar d)
										04.10.1200.1	BEEP	12	0	
											SPI0_SCLK	13	IOD	
											UART0_RX	14	10	
											ADC0_23	(Non-IOMUX 1) 0	А	
											PB8	1	Ю	
											UART1_CTS	2	I	
											TIMA0_C0	3	10	
											TIMG1_C0	5	Ю	1
										PB8	SPI0_SCLK	7	IOD	SDIO
22	F1		22	22						PINCM19	BEEP	8	0	(standar
										0x40428048	TIMG8_C0	9	10	d)
											UART0_RX	10	Ю	
											SPI0_POCI	11	10	
											I2C0_SCL	12	IOD	
											COMP0_OUT	14	0	
											PB9	1	IO	
											UART1_RTS	2	0	
											TIMA0_C0N	5	0	
											TIMA0_C1	6	IO	
										PB9	TIMG1_C1	7	IO	SDIO
23	E3		23	23						PINCM20	TIMG2_C0	8	10	(standar
										0x4042804c	SPI0_POCI	10	10	d)
											UART0_RX	11	Ю	
											I2C0_SCL	12	IOD	
											UART0_TX	13	0	
											I2C0_SDA	14	IOD	
											PB14	1	Ю	
											TIMA0_C0	5	Ю	1
											TIMG8_IDX	6	I	1
											SPI0_CS3_CD _MISO3	7	Ю	
									TIMG2_C1	8	Ю	1		
0.4	0.1			24			PB14	I2C0_SDA	9	IOD	SDIO			
24	G1		24	24				PINCM21 0x40428050	SPI0_PICO	10	Ю	(standar d)		
									0AT0720000	UART0_TX	11	0	1 ′	
										TIMA_FAL2	12	I	1	
										TIMA_FAL0	13	I	1	
											TIMG14_C2	14	Ю	1
											ADC0_21	(Non-IOMUX 1)	Α	1



						DGS2		DGS2	linue	PIN NAME/				
PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	8 PIN	RGE PIN	0 PIN	RUK PIN	IOMUX REG/	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
											PB15	1	Ю	
											UART2_TX	2	0	
											TIMG8_C0	5	Ю	
										PB15	TIMG2_C0	6	Ю	SDIO
25	E2		25	25						PINCM22	TIMA0_C1N	12	0	(standar
										0x40428054	UART1_TX	13	0	d)
											TIMG2_C1	14	10	
											ADC0_20	(Non-IOMUX 1)	Α	
											PB16	1	Ю	
											UART2_RX	2	I	
											TIMG8_C1	5	10	
										PB16	TIMG2_C1	6	Ю	SDIO
26	F2		26	26						PINCM23	TIMA0_C2N	12	0	(standar
										0x40428058	UART1_RX	13	I	- d)
											I2C1_SDA	14	IOD	
											ADC0_19	(Non-IOMUX 1)	А	
											PB17	1	10	
											UART2_TX	2	0	
											SPI0_PICO	3	10	
										DD47	I2C0_SCL	4	IOD]
36	G7			36						PB17 PINCM34	TIMA0_C2	5	10	SDIO (standar
	٥.									0x40428084	TIMG14_C0	6	10	d)
											TIMG1_C0	9	10	
											SPI0_CS0	10	10	
											ADC0_11	(Non-IOMUX 1)	А	
											PB18	1	Ю	
											UART2_RX	2	Ţ	
											SPI0_SCLK	3	IOD	
											I2C0_SDA	4	IOD	
										PB18	TIMA0_C2N	5	0	
37	E5	26	37	37	7			PINCM35	TIMG14_C1	6	Ю	SDIO (standar		
								0x40428088	SPI0_CS0	7	Ю	d)		
										TIMG1_C1	9	Ю		
											TIMA0_C1	12	Ю	
											UART0_RTS	13	0	
											ADC0_10	(Non-IOMUX 1)	Α	



									itinue					
PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
											PB19	1	10	
											SPI0_POCI	3	10	
											TIMG8_C1	4	Ю	
											UART0_CTS	5	I	
										PB19	TIMG2_C1	6	10	
38	F6		38	38						PINCM36	TIMG8_IDX	7	I	SDIO (standar
										0x4042808c	UART2_CTS	8	I	` d)
											TIMA0_C1N	12	0	
											UART2_RX	13	I	
											COMP0_OUT	14	0	
											ADC0_9	(Non-IOMUX 1) 0	А	
											PB20	1	10	
											SPI0_CS2_MIS O2	2	10	
											TIMA0_C2	5	10	
											TIMA_FAL1	6	I	
										PB20	TIMA0_C1	7	10	SDIO
41	E7		41	41						PINCM39	UART2_RTS	8	0	(standar
										0x40428098	I2C0_SDA	9	IOD	d)
											UART1_CTS	12	I	
											TIMA0_C2N	13	0	
											TIMG8_C1	14	10	
											ADC0_6	(Non-IOMUX 1) 0	А	
											PB24	1	10	
											SPI0_CS3_CD _MISO3	2	10	
											SPI0_CS1_MIS O1	3	Ю	
										PB24	TIMA0_C3	5	10	CDIO
42	D6	27	42	42						PINCM40	TIMA0_C1N	6	0	SDIO (standar
										0x4042809c	UART2_RTS	8	0	` d)
											SPI0_SCLK	12	IOD	
											TIMG14_C2	13	10	
											UART0_RTS	14	0	
											ADC0_5	(Non-IOMUX 1) 0	А	
6	A6	4	6	6	4	7	3	6	4	VDD	VDD	(Non-IOMUX 1) 0	PWR	PWR
7	A5	5	7	7	5	8	4	7	5	vss	VSS	(Non-IOMUX 1) 0	PWR	PWR

6.3 Signal Descriptions

Table 6-3. Analog to Digital Converter (ADC) Signal Descriptions

	Table	, 0-0. Alialog to Digital Col	IVCILC	י אסרעי	, Oigi	iai Des	cripti	0113			
SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	RGE PIN	DGS2 0 PIN	RUK PIN
ADC0_VREF+	А	ADC0 voltage reference (VREF) power supply	43	D7	28	43	43	27	19	18	16

Table 6-3. Analog to Digital Converter (ADC) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	RGE PIN	DGS2 0 PIN	RUK PIN
ADC0_VREF-	А	ADC0 voltage reference (VREF) ground supply	39	E6		39	39	25	17		
ADC0_0	А	ADC0 analog input channel 0	47	A7	32	47	47	31		2	20
ADC0_1	Α	ADC0 analog input channel 1	46	B7	31	46	46	30	22	1	19
ADC0_2	А	ADC0 analog input channel 2	45	C6	30	45	45	29	21	20	18
ADC0_3	А	ADC0 analog input channel 3	44	C7	29	44	44	28	20	19	17
ADC0_4	А	ADC0 analog input channel 4	35	G6	25	36	35	24	16	16	14
ADC0_5	Α	ADC0 analog input channel 5	42	D6	27	42	42				
ADC0_6	Α	ADC0 analog input channel 6	41	E7		41	41				
ADC0_7	А	ADC0 analog input channel 7	40	F7		40	40	26	18	17	15
ADC0_8	Α	ADC0 analog input channel 8	39	E6		39	39	25	17		
ADC0_9	Α	ADC0 analog input channel 9	38	F6		38	38				
ADC0_10	Α	ADC0 analog input channel 10	37	E5	26	37	37				
ADC0_11	Α	ADC0 analog input channel 11	36	G7			36				
ADC0_12	Α	ADC0 analog input channel 12	33	F5	22	33	33	22	14	14	12
ADC0_13	Α	ADC0 analog input channel 13	32	G5	21	32	32	21	13	13	11
ADC0_14	Α	ADC0 analog input channel 14	31	F4		31	31	20	12	12	10
ADC0_15	Α	ADC0 analog input channel 15	30	G4	20	30	30	19	11		
ADC0_16	Α	ADC0 analog input channel 16	29	F3	19	29	29	18			
ADC0_17	Α	ADC0 analog input channel 17	28	G3	18	28	28	17			
ADC0_18	Α	ADC0 analog input channel 18	27	G2		27	27	16			
ADC0_19	А	ADC0 analog input channel 19	26	F2		26	26				
ADC0_20	А	ADC0 analog input channel 20	25	E2		25	25				
ADC0_21	А	ADC0 analog input channel 21	24	G1		24	24				
ADC0_22	А	ADC0 analog input channel 22	34	B6	24	35	34	23	15	15	13
ADC0_23	Α	ADC0 analog input channel 23	21	E1	17	21	21				
ADC0_24	Α	ADC0 analog input channel 24	20	D1	16	20	20				
ADC0_25	А	ADC0 analog input channel 25	19	E4	15	19	19	15	10	11	9
ADC0_26	А	ADC0 analog input channel 26	43	D7	28	43	43	27	19	18	16

Table 6-4. Flash Bootstrap Loader (BSL) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
BSL_invoke (Flash)	I	Default Flash BSL invoke signal	33	F5	22	33	33	22	21	14	14	12

Table 6-5. Clock Module (CKM) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
CLK_OUT	0	CLK_OUT digital clock output from the PMCU	13, 17, 18, 29, 33, 40, 47, 5	A7, B2, B4, D2, D3, F3, F5,	13, 14, 19, 22, 32, 9	13, 17, 18, 29, 33, 4, 40, 47	13, 17, 18, 29, 33, 40, 47, 5	11, 13, 14, 18, 22, 26, 31	15,	14, 18, 8, 9	14, 17, 2	12, 15, 20



Table 6-5. Clock Module (CKM) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
FCC_IN	I	Frequency clock counter (FCC) input signal	1, 11, 13, 27, 31	B1, B2, D4, F4, G2	7, 9	1, 11, 13, 27, 31	1, 11, 13, 27, 31	1, 11, 16, 20, 9	12, 19, 4	12, 24	12, 4	10, 2
HFCLKIN	I	High frequency clock digital clock input signal	10, 12, 14, 16, 2	A2, B3, C1, C4, C5	10, 12, 2, 8	12, 14, 16, 2, 9	10, 12, 14, 16, 2	10, 12, 2, 8	11, 13, 5	1, 7	10, 5, 9	3, 7
HFXIN	А	High frequency crystal oscillator (HFXT) signal	11	B1	7	11	11	9	12			
HFXOUT	А	High frequency crystal oscillator (HFXT) signal	12	C1	8	12	12	10	13		10	
LFCLKIN	I	Low frequency clock digital clock input signal	10	A2		9	10	8	11	7	9	7
LFXIN	А	Low frequency crystal oscillator (LFXT) signal	9	A3		8	9	7	10	6		
LFXOUT	А	Low frequency crystal oscillator (LFXT) signal	10	A2		9	10	8	11	7	9	7

Table 6-6. Comparator (COMP) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
COMP0_DAC_OUT	Α	COMP0 DAC output	19	E4	15	19	19	15	16	10	11	9
COMP0_OUT	0	COMP0 output	13, 19, 22, 27, 31, 38, 47, 9	A3, A7, B2, E4, F1, F4, F6, G2	15, 32, 9	13, 19, 22, 27, 31, 38, 47, 8	13, 19, 22, 27, 31, 38, 47, 9	11, 15, 16, 20, 31, 7	10, 16, 19, 2	10, 12, 6	11, 12, 2	10, 20, 9
COMP0_IN0+	Α	COMP0 non-inverting input 0	46	B7	31	46	46	30	1	22	1	19
COMP0_IN0-	Α	COMP0 inverting input 0	47	A7	32	47	47	31	2		2	20
COMP0_IN1+	Α	COMP0 non-inverting input 1	33	F5	22	33	33	22	21	14	14	12
COMP0_IN1-	Α	COMP0 inverting input 1	32	G5	21	32	32	21	20	13	13	11
COMP0_IN2+	Α	COMP0 non-inverting input 2	29	F3	19	29	29	18	17			
COMP0_IN2-	Α	COMP0 inverting input 2	28	G3	18	28	28	17				
COMP0_IN3+	Α	COMP0 non-inverting input 3	30	G4	20	30	30	19	18	11		

Table 6-7. General Purpose Input Output Module Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
PA0	10	GPIO port A input/output 0	1	D4		1	1	1	4	24	4	2
PA1	10	GPIO port A input/output 1	2	C5	2	2	2	2	5	1	5	3
PA2	10	GPIO port A input/output 2	8	A4			8	6	9	5	8	6
PA3	10	GPIO port A input/output 3	9	A3		8	9	7	10	6		
PA4	Ю	GPIO port A input/output 4	10	A2		9	10	8	11	7	9	7



Table 6-7. General Purpose Input Output Module Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
PA5	Ю	GPIO port A input/output 5	11	B1	7	11	11	9	12			
PA6	Ю	GPIO port A input/output 6	12	C1	8	12	12	10	13		10	
PA7	Ю	GPIO port A input/output 7	13	B2	9	13	13	11				
PA8	Ю	GPIO port A input/output 8	16	C4	12	16	16	12				
PA9	Ю	GPIO port A input/output 9	17	D3	13	17	17	13	14	8		
PA10	Ю	GPIO port A input/output 10	18	D2	14	18	18	14	15	9		
PA11	Ю	GPIO port A input/output 11	19	E4	15	19	19	15	16	10	11	9
PA12	Ю	GPIO port A input/output 12	27	G2		27	27	16				
PA13	Ю	GPIO port A input/output 13	28	G3	18	28	28	17				
PA14	Ю	GPIO port A input/output 14	29	F3	19	29	29	18	17			
PA15	Ю	GPIO port A input/output 15	30	G4	20	30	30	19	18	11		
PA16	Ю	GPIO port A input/output 16	31	F4		31	31	20	19	12	12	10
PA17	Ю	GPIO port A input/output 17	32	G5	21	32	32	21	20	13	13	11
PA18	Ю	GPIO port A input/output 18	33	F5	22	33	33	22	21	14	14	12
PA19	Ю	GPIO port A input/output 19	34	B6	24	35	34	23	22	15	15	13
PA20	Ю	GPIO port A input/output 20	35	G6	25	36	35	24	23	16	16	14
PA21	Ю	GPIO port A input/output 21	39	E6		39	39	25	24	17		
PA22	Ю	GPIO port A input/output 22	40	F7		40	40	26	25	18	17	15
PA23	Ю	GPIO port A input/output 23	43	D7	28	43	43	27	26	19	18	16
PA24	Ю	GPIO port A input/output 24	44	C7	29	44	44	28	27	20	19	17
PA25	Ю	GPIO port A input/output 25	45	C6	30	45	45	29	28	21	20	18
PA26	Ю	GPIO port A input/output 26	46	B7	31	46	46	30	1	22	1	19
PA27	Ю	GPIO port A input/output 27	47	A7	32	47	47	31	2		2	20
PA28	Ю	GPIO port A input/output 28	3	B5	3	3	3					
PA29	Ю	GPIO port A input/output 29			23	34						
PA30	Ю	GPIO port A input/output 30	48	D5	1	48	48	32	3	23	3	1
PA31	Ю	GPIO port A input/output 31	5	B4		4	5					
PB2	Ю	GPIO port B input/output 2	14	В3	10	14	14					
PB3	Ю	GPIO port B input/output 3	15	C2	11	15	15					8
PB6	Ю	GPIO port B input/output 6	20	D1	16	20	20					
PB7	Ю	GPIO port B input/output 7	21	E1	17	21	21					
PB8	Ю	GPIO port B input/output 8	22	F1		22	22					
PB9	Ю	GPIO port B input/output 9	23	E3		23	23					
PB14	Ю	GPIO port B input/output 14	24	G1		24	24					
PB15	Ю	GPIO port B input/output 15	25	E2		25	25					
PB16	Ю	GPIO port B input/output 16	26	F2		26	26					
PB17	Ю	GPIO port B input/output 17	36	G7			36					
PB18	10	GPIO port B input/output 18	37	E5	26	37	37					
PB19	10	GPIO port B input/output 19	38	F6		38	38					
PB20	10	GPIO port B input/output 20	41	E7		41	41					
PB24	Ю	GPIO port B input/output 24	42	D6	27	42	42					



Table 6-8. I2C Signal Descriptions

	1	1able 6-8. I20		iai De	Script			1	1			
SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
12C0_SCL	IOD	I2C0 serial clock signal (SCL)	17, 19, 2, 22, 23, 29, 36, 40, 45, 46, 47, 5, 8	A4, A7, B4, B7, C5, C6, D3, E3, E4, F1, F3, F7, G7	13, 15, 19, 2, 30, 31, 32	17, 19, 2, 22, 23, 29, 4, 40, 45, 46, 47	17, 19, 2, 22, 23, 29, 36, 40, 45, 46, 47, 5, 8	13, 15, 18, 2, 26, 29, 30, 31, 6	1, 14, 16, 17, 2, 25, 28, 5, 9	1, 10, 18, 21, 22, 5, 8	1, 11, 17, 2, 20, 5, 8	15, 18, 19, 20, 3, 6, 9
I2C0_SDA	IOD	I2C0 serial data signal (SDA)	1, 12, 16, 18, 2, 23, 24, 3, 32, 37, 41, 44, 45, 46, 48, 9	A3, B5, B7, C1, C4, C5, C6, C7, D2, D4, D5, E3, E5, E7, G1,	1, 12, 14, 2, 21, 26, 29, 3, 30, 31, 8	1, 12, 16, 18, 2, 23, 24, 3, 32, 37, 41, 44, 45, 46, 48, 8	1, 12, 16, 18, 2, 23, 24, 3, 32, 37, 41, 44, 45, 46, 48, 9	1, 10, 12, 14, 2, 21, 28, 29, 30, 32, 7	1, 10, 13, 15, 20, 27, 28, 3, 4, 5	1, 13, 20, 21, 22, 23, 24, 6, 9	1, 10, 13, 19, 20, 3, 4, 5	1, 11, 17, 18, 19, 2, 3
I2C1_SCL	IOD	I2C1 serial clock signal (SCL)	10, 12, 14, 19, 27, 30, 32, 35	A2, B3, C1, E4, G2, G4, G5, G6	10, 15, 20, 21, 25, 8	12, 14, 19, 27, 30, 32, 36, 9	10, 12, 14, 19, 27, 30, 32, 35	10, 15, 16, 19, 21, 24, 8	11, 13, 16, 18, 20, 23	10, 11, 13, 16, 7	10, 11, 13, 16, 9	11, 14, 7, 9
I2C1_SDA	IOD	I2C1 serial data signal (SDA)	11, 15, 18, 26, 31, 33, 34, 9	A3, B1, B6, C2, D2, F2, F4, F5	11, 14, 22, 24, 7	11, 15, 18, 26, 31, 33, 35, 8	11, 15, 18, 26, 31, 33, 34, 9	14, 20, 22, 23, 7, 9	10, 12, 15, 19, 21, 22	12, 14, 15, 6, 9	12, 14, 15	10, 12, 13, 8

Table 6-9. Real-time Clock (RTC) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A)	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
RTC_OUT	0	Real-time clock output signal		A7, C2, D3, D4, G3	11, 13, 18, 32	1, 15, 17,	17,	1, 13, 17, 31		24, 8	2, 4	2, 20,



Table 6-10. Serial Peripheral Interface (SPI) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
SPI0_PICO	IO	SPI0 peripheral in controller out signal	11, 13, 14, 17, 18, 24, 29, 33, 34, 35, 36, 44, 45	B1, B2, B3, B6, C6, C7, D2, D3, F3, F5, G1, G6, G7	10, 13, 14, 19, 22, 23, 24, 25, 29, 30, 7, 9	11, 13, 14, 17, 18, 24, 29, 33, 34, 35, 36,	11, 13, 14, 17, 18, 24, 29, 33, 34, 35, 36, 44, 45	11, 13, 14, 18, 22, 23, 24, 28, 29, 9	12, 14, 15, 17, 21, 22, 23, 27, 28	14, 15, 16, 20, 21, 8,	14, 15, 16, 19, 20	12, 13, 14, 17, 18
SPI0_POCI	Ю	SPI0 peripheral out controller in signal	10, 13, 17, 18, 22, 23, 28, 31, 33, 34, 38, 40, 43, 445, 46, 47	A2, A7, B2, B6, B7, C6, D2, D3, D7, E3, F1, F4, F5, F6, F7, G3	13, 14, 18, 22, 24, 28, 30, 31, 32, 9	13, 17, 18, 22, 23, 28, 31, 33, 35, 38, 40, 43, 45, 46, 47, 9	10, 13, 17, 18, 22, 23, 28, 31, 33, 34, 40, 43, 445, 46, 47	11, 13, 14, 17, 20, 22, 23, 26, 27, 29, 30, 31, 8	1, 11, 14, 15, 19, 2, 21, 22, 25, 26, 28	12, 14, 15, 18, 19, 21, 22, 7, 8, 9	1, 12, 14, 15, 17, 18, 2, 20, 9	10, 12, 13, 15, 16, 18, 19, 20, 7
SPI0_SCLK	IOD	SPI0 serial clock	12, 15, 16, 19, 21, 22, 27, 32, 34, 37, 42, 45	B6, C1, C2, C4, C6, D6, E1, E4, E5, F1, G2,	11, 12, 15, 17, 21, 24, 26, 27, 30, 8	12, 15, 16, 19, 21, 22, 27, 32, 35, 37, 42, 45	12, 15, 16, 19, 21, 22, 27, 32, 34, 37, 42, 45	10, 12, 15, 16, 21, 23, 29	13, 16, 20, 22, 28	10, 13, 15, 21	10, 11, 13, 15, 20	11, 13, 18, 8, 9
SPI0_CS0	Ю	SPI0 chip-select 0 signal	10, 15, 16, 19, 28, 33, 35, 36, 37, 8	A2, A4, C2, C4, E4, E5, F5, G3, G6,	11, 12, 15, 18, 22, 25, 26	15, 16, 19, 28, 33, 36, 37, 9	10, 15, 16, 19, 28, 33, 35, 36, 37, 8	12, 15, 17, 22, 24, 6,	11, 16, 21, 23, 9	10, 14, 16, 5, 7	11, 14, 16, 8, 9	12, 14, 6, 7, 8, 9
SPI0_CS1_MISO1	Ю		1, 20, 27, 32, 42, 9	A3, D1, D4, D6, G2, G5	16, 21, 27	1, 20, 27, 32, 42, 8	1, 20, 27, 32, 42, 9	1, 16, 21, 7	10, 20, 4	13, 24, 6	13, 4	11, 2



Table 6-10. Serial Peripheral Interface (SPI) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
SPI0_CS2_MISO2	Ю		13, 21, 29, 30, 40, 41, 44	B2, C7, E1, E7, F3, F7, G4	17, 19, 20, 29, 9	13, 21, 29, 30, 40, 41, 44	13, 21, 29, 30, 40, 41, 44	11, 18, 19, 26, 28	17, 18, 25, 27	11, 18, 20	17, 19	15, 17
SPI0_CS3_CD_MIS O3	Ю		16, 2, 24, 28, 39, 42, 43, 47, 9	A3, A7, C4, C5, D6, D7, E6, G1,	12, 18, 2, 27, 28, 32	16, 2, 24, 28, 39, 42, 43, 47, 8	16, 2, 24, 28, 39, 42, 43, 47, 9	12, 17, 2, 25, 27, 31, 7	10, 2, 24, 26, 5	1, 17, 19, 6	18, 2, 5	16, 20, 3

Table 6-11. Serial Wire Debug (SWD) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
SWCLK	I	Serial wire debug interface clock input signal	35	G6	25	36	35	24	23	16	16	14
SWDIO	10	Serial wire debug interface data input/output signal	34	B6	24	35	34	23	22	15	15	13

Table 6-12. System Controller (SYSCTL) Signal Descriptions

		ubic o 12. Oyotoiii contit			_, _,	<u> </u>	••••					
SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
BEEP	0	Beep output	1, 12, 21, 22, 46	B7, C1, D4, E1, F1	17, 31, 8	1, 12, 21, 22, 46	1, 12, 21, 22, 46	1, 10, 30	1, 13,	22, 24	1, 10, 4	19, 2
NRST	RESET	Active-low reset signal (must be logic high for the device to start)	4	A1	6	10	4	3	6	2	5	3
VDD	PWR	VDD supply	6	A6	4	6	6	4	7	3	6	4
VSS	PWR	VSS (ground)	7	A5	5	7	7	5	8	4	7	5

Table 6-13. Timer (TIMx) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
TIMA0_C0	Ю	TIMA0 capture/compare 0 signal	1, 15, 16, 22, 24, 33, 35, 39, 46, 48, 8	A4, B7, C2, C4, D4, D5, E6, F1, F5, G1,	1, 11, 12, 22, 25, 31	1, 15, 16, 22, 24, 33, 36, 39, 46, 48	1, 15, 16, 22, 24, 33, 35, 39, 46, 48, 8	1, 12, 22, 24, 25, 30, 32, 6	1, 21, 23, 24, 3, 4, 9	14, 16, 17, 22, 23, 24, 5	16, 3, 4, 8	1, 12, 14, 19, 2, 6, 8



Table 6-13. Timer (TIMx) Signal Descriptions (continued)

		Table 6-13. Timer (TIMx		ai Des	Lipu			ieu)				
SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
TIMA0_C1	Ю	TIMA0 capture/compare 1 signal	11, 13, 17, 2, 23, 28, 3, 37, 40, 41, 9	A3, B1, B2, B5, C5, D3, E3, E5, E7, F7, G3	13, 18, 2, 26, 3, 7, 9	11, 13, 17, 2, 23, 28, 3, 37, 40, 41, 8	11, 13, 17, 2, 23, 28, 3, 37, 40, 41, 9	11, 13, 17, 2, 26, 7, 9	10, 12, 14, 25, 5	1, 18, 6, 8	17, 5	15, 3
TIMA0_C2	Ю	TIMA0 capture/compare 2 signal	12, 13, 18, 29, 30, 32, 34, 36, 41, 45, 9	A3, B2, B6, C1, C6, D2, E7, F3, G4, G5, G7	14, 19, 20, 21, 24, 30, 8, 9	12, 13, 18, 29, 30, 32, 35, 41, 45, 8	12, 13, 18, 29, 30, 32, 34, 36, 41, 45, 9	10, 11, 14, 18, 19, 21, 23, 29, 7	10, 13, 15, 17, 18, 20, 22, 28	11, 13, 15, 21, 6, 9	10, 13, 15, 20	11, 13, 18
TIMA0_C3	Ю	TIMA0 capture/compare 3 signal	10, 14, 27, 3, 32, 42, 43, 45	A2, B3, B5, C6, D6, D7, G2, G5	10, 21, 27, 28, 3, 30	14, 27, 3, 32, 42, 43, 45, 9	10, 14, 27, 3, 32, 42, 43, 45	16, 21, 27, 29, 8	11, 20, 26, 28	13, 19, 21, 7	13, 18, 20, 9	11, 16, 18, 7
TIMA0_C0N	0	TIMA0 capture/compare 0 complementary output	10, 17, 23, 32, 39, 40, 47	A2, A7, D3, E3, E6, F7, G5	13, 21, 32	17, 23, 32, 39, 40, 47, 9	10, 17, 23, 32, 39, 40, 47	13, 21, 25, 26, 31, 8	11, 14, 2, 20, 24, 25	13, 17, 18, 7, 8	13, 17, 2, 9	11, 15, 20, 7
TIMA0_C1N	0	TIMA0 capture/compare 1 complementary output	10, 14, 18, 25, 33, 38, 42, 45	A2, B3, C6, D2, D6, E2, F5,	10, 14, 22, 27, 30	14, 18, 25, 33, 38, 42, 45, 9	10, 14, 18, 25, 33, 38, 42, 45	14, 22, 29, 8	11, 15, 21, 28	14, 21, 7, 9	14, 20, 9	12, 18, 7
TIMA0_C2N	0	TIMA0 capture/compare 2 complementary output	12, 19, 20, 26, 28, 31, 35, 37, 41, 8	A4, C1, D1, E4, E5, E7, F2, F4, G3, G6	15, 16, 18, 25, 26, 8	12, 19, 20, 26, 28, 31, 36, 37, 41	12, 19, 20, 26, 28, 31, 35, 37, 41, 8	10, 15, 17, 20, 24, 6	13, 16, 19, 23, 9	10, 12, 16, 5	10, 11, 12, 16, 8	10, 14, 6, 9



Table 6-13. Timer (TIMx) Signal Descriptions (continued)

		Table 6-13. Timer (TIMX)) Signa	ai Des	criptio	ons (c	Ontini	uea)				
SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
TIMA0_C3N	0	TIMA0 capture/compare 3 complementary output	15, 16, 20, 27, 28, 33, 44, 46, 5, 8	A4, B4, B7, C2, C4, C7, D1, F5, G2, G3	11, 12, 16, 18, 22, 29, 31	15, 16, 20, 27, 28, 33, 4, 44, 46	15, 16, 20, 27, 28, 33, 44, 46, 5, 8	12, 16, 17, 22, 28, 30, 6	1, 21, 27, 9	14, 20, 22, 5	1, 14, 19, 8	12, 17, 19, 6, 8
TIMA_FAL0	ı	TIMA fault input 0	12, 15, 16, 19, 24, 3, 46, 8	A4, B5, B7, C1, C2, C4, E4, G1	11, 12, 15, 3, 31, 8	12, 15, 16, 19, 24, 3, 46	12, 15, 16, 19, 24, 3, 46, 8	10, 12, 15, 30, 6	1, 13, 16, 9	10, 22, 5	1, 10, 11, 8	19, 6, 8, 9
TIMA_FAL1	I	TIMA fault input 1	1, 11, 17, 18, 35, 41, 8	A4, B1, D2, D3, D4, E7, G6	13, 14, 25, 7	1, 11, 17, 18, 36, 41	1, 11, 17, 18, 35, 41, 8	1, 13, 14, 24, 6, 9	12, 14, 15, 23, 4, 9	16, 24, 5, 8, 9	16, 4, 8	14, 2, 6
TIMA_FAL2	I	TIMA fault input 2	16, 2, 20, 24, 33, 45, 47	A7, C4, C5, C6, D1, F5,	12, 16, 2, 22, 30, 32	16, 2, 20, 24, 33, 45, 47	16, 2, 20, 24, 33, 45, 47	12, 2, 22, 29, 31	2, 21, 28, 5	1, 14, 21	14, 2, 20, 5	12, 18, 20, 3
TIMG8_IDX	I	TIMG8 quadrature encoder index pulse signal	13, 2, 24, 30, 38, 48, 8	A4, B2, C5, D5, F6, G1,	1, 2, 20, 9	13, 2, 24, 30, 38, 48	13, 2, 24, 30, 38, 48, 8	11, 19, 2, 32, 6	18, 3, 5, 9	1, 11, 23, 5	3, 5, 8	1, 3, 6
TIMG14_C0	Ю	TIMG14 capture/compare 0 signal	1, 11, 18, 27, 34, 36, 43, 45	B1, B6, C6, D2, D4, D7, G2, G7	14, 24, 28, 30, 7	1, 11, 18, 27, 35, 43, 45	18, 27, 34,	1, 14, 16, 23, 27, 29, 9	12, 15, 22, 26, 28, 4	15, 19, 21, 24, 9	15, 18, 20, 4	13, 16, 18, 2
TIMG14_C1	Ю	TIMG14 capture/compare 1 signal	12, 19, 2, 28, 30, 35, 37, 44	C1, C5, C7, E4, E5, G3, G4, G6	15, 18, 2, 20, 25, 26, 29, 8	12, 19, 2, 28, 30, 36, 37, 44	12, 19, 2, 28, 30, 35, 37, 44	10, 15, 17, 19, 2, 24, 28	13, 16, 18, 23, 27, 5	1, 10, 11, 16, 20	10, 11, 16, 19, 5	14, 17, 3, 9
TIMG14_C2	Ю	TIMG14 capture/compare 2 signal	24, 31, 42, 48	D5, D6, F4, G1	1, 27	24, 31, 42, 48	24, 31, 42, 48	20, 32	19, 3	12, 23	12, 3	1, 10



Table 6-13. Timer (TIMx) Signal Descriptions (continued)

Table 6-13. Timer (TIMx) Signal Descriptions (continued)												
SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
TIMG14_C3	Ю	TIMG14 capture/compare 3 signal	28	G3	18	28	28	17				
TIMG1_C0	Ю	TIMG1 capture/compare 0 signal	11, 13, 14, 20, 22, 29, 36, 39, 45	B1, B2, B3, C6, D1, E6, F1, F3, G7	10, 16, 19, 30, 7, 9	11, 13, 14, 20, 22, 29, 39, 45	11, 13, 14, 20, 22, 29, 36, 39, 45	11, 18, 25, 29, 9	12, 17, 24, 28	17, 21	20	18
TIMG1_C1	Ю	TIMG1 capture/compare 1 signal	12, 15, 17, 21, 23, 37, 40, 46	B7, C1, C2, D3, E1, E3, E5,	11, 13, 17, 26, 31, 8	12, 15, 17, 21, 23, 37, 40, 46	12, 15, 17, 21, 23, 37, 40, 46	10, 13, 26, 30	1, 13, 14, 25	18, 22, 8	1, 10, 17	15, 19, 8
TIMG2_C0	Ю	TIMG2 capture/compare 0 signal	17, 23, 25, 3, 32, 43, 46, 9	A3, B5, B7, D3, D7, E2, E3, G5	13, 21, 28, 3, 31	17, 23, 25, 3, 32, 43, 46, 8	17, 23, 25, 3, 32, 43, 46, 9	13, 21, 27, 30, 7	1, 10, 14, 20, 26	13, 19, 22, 6, 8	1, 13, 18	11, 16, 19
TIMG2_C1	Ю	TIMG2 capture/compare 1 signal	10, 13, 15, 16, 18, 24, 25, 26, 27, 33, 38, 44, 47, 48, 8	A2, A4, A7, B2, C2, C4, C7, D2, D5, E2, F2, F5, F6, G1,	1, 11, 12, 14, 22, 29, 32, 9	13, 15, 16, 18, 24, 25, 26, 27, 33, 38, 44, 47, 48, 9	10, 13, 15, 16, 18, 24, 25, 26, 27, 33, 38, 44, 47, 48, 8	11, 12, 14, 16, 22, 28, 31, 32, 6, 8	11, 15, 2, 21, 27, 3, 9	14, 20, 23, 5, 7, 9	14, 19, 2, 3, 8, 9	1, 12, 17, 20, 6, 7, 8
TIMG8_C0	Ю	TIMG8 capture/compare 0 signal	11, 13, 2, 20, 22, 25, 32, 39, 43, 46, 9	A3, B1, B2, B7, C5, D1, D7, E2, E6, F1,	16, 2, 21, 28, 31, 7, 9	11, 13, 2, 20, 22, 25, 32, 39, 43, 46, 8	11, 13, 2, 20, 22, 25, 32, 39, 43, 46, 9	11, 2, 21, 25, 27, 30, 7, 9	1, 10, 12, 20, 24, 26, 5	1, 13, 17, 19, 22, 6	1, 13, 18, 5	11, 16, 19, 3



Table 6-13. Timer (TIMx) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
TIMG8_C1	Ю	TIMG8 capture/compare 1 signal	1, 10, 12, 18, 20, 21, 26, 28, 33, 38, 40, 41, 44,	A2, A4, A7, C1, C7, D1, D2, D4, E1, E7, F2, F6, F7, G3	14, 16, 17, 18, 22, 29, 32, 8	1, 12, 18, 20, 21, 26, 28, 33, 38, 40, 41, 44, 47, 9	1, 10, 12, 18, 20, 21, 26, 28, 33, 38, 40, 41, 44, 47, 8	1, 10, 14, 17, 22, 26, 28, 31, 6, 8	11, 13, 15, 2, 21, 25, 27, 4, 9	14, 18, 20, 24, 5, 7, 9	10, 14, 17, 19, 2, 4, 8, 9	12, 15, 17, 2, 20, 6, 7

Table 6-14. Universal Asynchronous Receiver Transmitter (UART) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
UARTO_CTS	I	UART0 clear to send signal	11, 17, 29, 34, 38, 43	B1, B6, D3, D7, F3, F6	13, 19, 24, 28, 7	11, 17, 29, 35, 38, 43	11, 17, 29, 34, 38, 43	13, 18, 23, 27, 9	12, 14, 17, 22, 26	15, 19, 8	15, 18	13, 16
UARTO_RTS	0	UART0 ready to send signal	12, 16, 30, 35, 37, 42, 44	C1, C4, C7, D6, E5, G4, G6	12, 20, 23, 25, 26, 27, 29, 8	12, 16, 30, 34, 36, 37, 42, 44	12, 16, 30, 35, 37, 42, 44	10, 12, 19, 24, 28	13, 18, 23, 27	11, 16, 20	10, 16, 19	14, 17
UARTO_RX	Ю	UART0 receive signal (RXD)	19, 2, 21, 22, 23, 28, 32, 46, 48, 5	B4, B7, C5, D5, E1, E3, E4, F1, G3, G5	1, 15, 17, 18, 2, 21, 31	19, 2, 21, 22, 23, 28, 32, 4, 46, 48	19, 2, 21, 22, 23, 28, 32, 46, 48, 5	15, 17, 2, 21, 30, 32	1, 16, 20, 3, 5	1, 10, 13, 22, 23	1, 11, 13, 3, 5	1, 11, 19, 3, 9
UARTO_TX	0	UART0 transmit signal (TXD)	1, 18, 2, 20, 23, 24, 29, 3, 43, 45, 47	A7, B5, C5, C6, D1, D2, D4, D7, E3, F3, G1	14, 16, 19, 2, 28, 3, 30, 32	1, 18, 2, 20, 23, 24, 29, 3, 43, 45, 47	1, 18, 2, 20, 23, 24, 29, 3, 43, 45, 47	1, 14, 18, 2, 27, 29, 31	15, 17, 2, 26, 28, 4, 5	1, 19, 21, 24, 9	18, 2, 20, 4, 5	16, 18, 2, 20, 3



Table 6-14. Universal Asynchronous Receiver Transmitter (UART) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
UART1_CTS	I	UART1 clear to send signal	14, 22, 27, 39, 41, 46, 47	A7, B3, B7, E6, E7, F1, G2	10, 31, 32	27, 39, 41,	14, 22, 27, 39, 41, 46, 47	16, 25, 30, 31	1, 2, 24	17, 22	1, 2	19, 20
UART1_RTS	0	UART1 ready to send signal	15, 2, 23, 28, 33, 40, 48	C2, C5, D5, E3, F5, F7, G3	1, 11, 18, 2, 22	15, 2, 23, 28, 33, 40, 48	15, 2, 23, 28, 33, 40, 48	17, 2, 22, 26, 32	21, 25, 3, 5	1, 14, 18, 23	14, 17, 3, 5	1, 12, 15, 3, 8
UART1_RX	I	UART1 receive signal (RXD)	10, 12, 14, 16, 17, 19, 21, 26, 33, 34, 35, 40, 44	A2, B3, B6, C1, C4, C7, D3, E1, E4, F2, F5, F7, G6	10, 12, 13, 15, 17, 22, 24, 25, 29, 8	12, 14, 16, 17, 19, 21, 26, 33, 35, 36, 40, 44, 9	10, 12, 14, 16, 17, 19, 21, 26, 33, 34, 35, 40, 44	10, 12, 13, 15, 22, 23, 24, 26, 28, 8	11, 13, 14, 16, 21, 22, 23, 25, 27	10, 14, 15, 16, 18, 20, 7,	10, 11, 14, 15, 16, 17, 19, 9	12, 13, 14, 15, 17, 7, 9
UART1_TX	0	UART1 transmit signal (TXD)	11, 13, 15, 16, 20, 25, 32, 35, 9	A3, B1, B2, C2, C4, D1, E2, G5, G6	11, 12, 16, 21, 25, 7, 9	11, 13, 15, 16, 20, 25, 32, 36, 8	11, 13, 15, 16, 20, 25, 32, 35, 9	11, 12, 21, 24, 7, 9	10, 12, 20, 23	13, 16, 6	13, 16	11, 14, 8
UART2_CTS	I	UART2 clear to send signal	14, 20, 27, 31, 38, 39, 45, 9	A3, B3, C6, D1, E6, F4, F6,	10, 16, 30	14, 20, 27, 31, 38, 39, 45, 8	14, 20, 27, 31, 38, 39, 45, 9	16, 20, 25, 29, 7	10, 19, 24, 28	12, 17, 21, 6	12, 20	10, 18
UART2_RTS	0	UART2 ready to send signal	10, 15, 21, 30, 41, 42, 46	A2, B7, C2, D6, E1, E7, G4	11, 17, 20, 27, 31	15, 21, 30, 41, 42, 46, 9	10, 15, 21, 30, 41, 42, 46	19, 30, 8	1, 11, 18	11, 22, 7	1, 9	19, 7, 8
UART2_RX	I	UART2 receive signal (RXD)	15, 26, 29, 37, 38, 39, 40, 44	C2, C7, E5, E6, F2, F3, F6,	11, 19, 26, 29	15, 26, 29, 37, 38, 39, 40, 44	15, 26, 29, 37, 38, 39, 40, 44	18, 25, 26, 28	17, 24, 25, 27	17, 18, 20	17, 19	15, 17, 8



Table 6-14. Universal Asynchronous Receiver Transmitter (UART) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT (A) PIN	ZCM PIN	VFC PIN	PT (B) PIN	RGZ PIN	RHB PIN	DGS2 8 PIN	RGE PIN	DGS2 0 PIN	RUK PIN
UART2_TX	0	UART2 transmit signal (TXD)	14, 25, 28, 36, 39, 40, 43	E2, E6, F7,	18, 28	28, 39, 40, 43	36,	17, 25, 26, 27	24, 25, 26	1 1	17, 18	15, 16

6.4 Connections for Unused Pins

Table 6-15 lists the correct termination of unused pins.

Table 6-15. Connection of Unused Pins

PIN ⁽¹⁾	POTENTIAL	COMMENT
PAx and PBx	Open	Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unused pins to output low or input with internal pullup/pulldown resistor.
NRST		NRST is an active-low reset signal; it must be pulled high to VCC or the device will not start, for more information refer to Section 9.1

(1) Any unused pin with a function that is shared with general-purpose I/O should follow the "PAx and PBx" unused pin connection guidelines.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VDD	Supply voltage	At VDD pin, with respect to VSS	-0.3	4.1	V
VI	Input voltage	Applied to any 5-V tolerant open-drain pins	-0.3	5.5	V
VI	Input voltage	Applied to any common tolerance pins	-0.3	V _{DD} + 0.3 (4.1 MAX)	V
(3)	Current into VDD pin	-40°C ≤ Tj ≤ 130°C		80	mA
I _{VDD} ⁽³⁾	(source)	-40°C ≤ Tj ≤ 85°C		100	mA
. (3)	Current out of VSS pin	-40°C ≤ Tj ≤ 130°C		80	mA
I _{VSS} ⁽³⁾	(sink)	-40°C ≤ Tj ≤ 85°C		100	mA
	Current for SDIO pin	Current sunk or sourced by SDIO pin		6	mA
I _{IO}	Current for ODIO pin	Current sunk by ODIO pin		20	mA
I _D	Supported diode current	Diode current at any device pin		±2	mA
Tj	Junction temperature		-40	130	°C
T _{stg}	Storage temperature ⁽²⁾		-40	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±2000	V
V _(ESD)	Liectrostatic discriatge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage (3)	1.62 ⁽⁴⁾		3.6	V
C _{VDD}	Capacitor placed between VDD and VSS (1)		10		uF
T _A	Ambient temperature	-40		125	°C
TJ	Max junction temperature			130	°C
f	MCLK, CPUCLK, ULPCLK frequency with 1 flash wait state (2)			32	MHz
f _{MCLK}	MCLK, CPUCLK, ULPCLK frequency with 0 flash wait states (2)			24	IVITIZ

⁽¹⁾ Connect C_{VDD} between VDD/VSS as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of ±20% or better is required for C_{VDD}.

⁽²⁾ Higher temperatures may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

⁽³⁾ For applications operating at VDD=1.62V, I VDD/I VSS<=20mA is required to ensure device functionality

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

⁽²⁾ Wait states are managed automatically by the system controller (SYSCTL) and do not need to be configured by application software.

⁽³⁾ There is no dependency on MCLK frequency with respect to VDD recommended operating range.

⁽⁴⁾ Functionality is guaranteed down to V_{BOR0-(min)}.



7.4 Thermal Information

R _{BJC(bot)} Junction-to-case (bottom) thermal resistance 9.1 °C/W R _{BJA} Junction-to-ambient thermal resistance 80.6 °C/W R _{BJB} Junction-to-case (top) thermal resistance 39.9 °C/W W _{JT} Junction-to-board thermal resistance 42.6 °C/W W _{JB} Junction-to-board characterization parameter 42.6 °C/W R _{BJC(bot)} Junction-to-board characterization parameter 42.2 °C/W R _{BJC(bot)} Junction-to-case (bottom) thermal resistance N/A °C/W R _{BJC(bot)} Junction-to-case (bottom) thermal resistance 47.1 °C/W R _{BJC(bot)} Junction-to-board thermal resistance 47.1 °C/W W _{JT} Junction-to-coase (bottom) thermal resistance 23.7 °C/W R _{BJC(bot)} Junction-to-case (bottom) thermal resistance 93.3 °C/W R _{BJC(bot)} Junction-to-case (bottom) thermal resistance 93.8 °C/W R _{BJC(bot)} Junction-to-board characterization parameter VSSOP-20 (DGS20) 49.6 °C/W W _{JT} Junction-to-board		THERMAL METRIC(1)	PACKAGE	VALUE	UNIT
R _{3LC(top)} Junction-to-case (top) thermal resistance 35.1 *C/W R _{3LB} Junction-to-top characterization parameter 50.7 *C/W Ψ _{3L} Junction-to-board characterization parameter 50.1 *C/W R _{3LC(top)} Junction-to-case (bottom) thermal resistance N/A *C/W R _{3LR} Junction-to-case (top) thermal resistance 34.6 *C/W R _{3LR} Junction-to-choard thermal resistance 25.4 *C/W R _{3LR} Junction-to-choard thermal resistance 25.4 *C/W R _{3LR} Junction-to-board thermal resistance 25.4 *C/W R _{3LR} Junction-to-choard characterization parameter *P. *C/W *P. *C/W R _{3LR} Junction-to-choard characterization parameter *P. *C/W *P. *C/W R _{3LR} Junction-to-choare (top) themal resistance *P. *C/W *P. *C/W R _{3LC(top)} Junction-to-choare (top) themal resistance *P. *C/W R _{3LC(top)} Junction-to-choare (tot) themal resistance *P. *C/W R _{3LR} Junction-to-coare (tot) themal resistance *P. *C/W <	$R_{\theta JA}$	Junction-to-ambient thermal resistance		78.8	°C/W
R _{9,16} Junction-to-board thermal resistance LOFP-48 (PT) 3.5 "CW W _{1,17} Junction-to-board characterization parameter N/A 3.5 "CW R _{QLC(bcd)} Junction-to-case (bottom) thermal resistance N/IA "CW R _{QLC(bcd)} Junction-to-case (bottom) thermal resistance 25.4 "CW R _{QLC(bcd)} Junction-to-board thermal resistance 25.4 "CW R _{QLC(bcd)} Junction-to-board thermal resistance 27.5 "CW W _{1,17} Junction-to-board characterization parameter 17.5 "CW R _{QLC(bcd)} Junction-to-board characterization parameter 9.0 "CW R _{QLC(bcd)} Junction-to-case (bottom) thermal resistance 38.7 "CW R _{QLC(bcd)} Junction-to-case (bottom) thermal resistance 9.1 "CW R _{QLC(bcd)}		Junction-to-case (top) thermal resistance		35.1	°C/W
Ψ ₁₇ Junction-to-top characterization parameter 3.5 *C/W R _{GC(bot)} Junction-to-board characterization parameter N/A *C/W R _{GC(bot)} Junction-to-case (bottom) thermal resistance 3.4.6 *C/W R _{GC(bot)} Junction-to-case (fop) thermal resistance 25.4 *C/W R _{BB} Junction-to-case (fop) thermal resistance 25.4 *C/W Ψ ₁₇ Junction-to-case (totom) thermal resistance 71.75 *C/W R _{SC(bot)} Junction-to-board characterization parameter 9.0 *C/W R _{SC(bot)} Junction-to-case (bottom) thermal resistance 9.0 *C/W R _{SC(bot)} Junction-to-case (bottom) thermal resistance 38.7 *C/W R _{SC(bot)} Junction-to-board thermal resistance 38.7 *C/W R _{SC(bot)} Junction-to-board characterization parameter *QFN-32 (RHB) *18.7 *C/W Ψ ₁₇ Junction-to-board characterization parameter *QFN-32 (RHB) *QFN-32		Junction-to-board thermal resistance	1.05D 40 (DT)	50.7	°C/W
R _{BLC(Dot0)} Junction-to-case (bottom) thermal resistance N/A °C/W R _{BA} Junction-to-case (top) thermal resistance 34.6 °C/W R _{BA} Junction-to-case (top) thermal resistance 25.4 °C/W W _{JT} Junction-to-board thermal resistance 17.5 °C/W W _{JT} Junction-to-board characterization parameter 17.5 °C/W R _{BLC(Dot0)} Junction-to-case (bottom) thermal resistance 9.0 °C/W R _{BLC(Dot0)} Junction-to-case (top) thermal resistance 38.7 °C/W R _{BLC(Dot0)} Junction-to-board thermal resistance 38.7 °C/W R _{BLC(Dot0)} Junction-to-board characterization parameter 18.7 °C/W R _{BLC(Dot0)} Junction-to-case (bottom) thermal resistance 9.1 °C/W R _{BLC(Dot0)} Junction-to-case (bottom) thermal resistance 80.6 °C/W R _{BLC(Dot0)} Junction-to-case (bottom) thermal resistance 42.6 °C/W R _{BLC(Dot0)} Junction-to-case (bottom) thermal resistance 42.2 °C/W R _{BLC(Dot0)} Junction-to-case (bottom) therma	Ψ_{JT}	Junction-to-top characterization parameter	LQFP-48 (P1)	3.5	°C/W
R _{BLC} (both) Junction-to-ambient thermal resistance 25.4 °C/W R _{BC(Dipo)} Junction-to-case (top) thermal resistance 25.4 °C/W R _{BU} Junction-to-board thermal resistance 47.75 °C/W Ψ _{JT} Junction-to-board characterization parameter 11.6 °C/W R _{BUC(Dot)} Junction-to-case (bottom) thermal resistance 9.0 °C/W R _{BU} Junction-to-case (top) thermal resistance 38.7 °C/W R _{BUC(Dot)} Junction-to-board thermal resistance 31.1 °C/W R _{BU} Junction-to-board thermal resistance 31.1 °C/W R _{BUC(Dot)} Junction-to-board thermal resistance 11.6 °C/W R _{BUC(Dot)} Junction-to-board thermal resistance 31.1 °C/W R _{BUC(Dot)} Junction-to-case (bottom) thermal resistance 9.1 °C/W R _{BUC(Dot)} Junction-to-case (bottom) thermal resistance 9.1 °C/W R _{BUC(Dot)} Junction-to-case (bottom) thermal resistance 42.6 °C/W W _{JT} Junction-to-board characterization parameter 42.2 °C/W R _{BUC(Dot)} Junction-to-board thermal resistance 47.1 °C/W R _{BUC(Dot)} Junction-t	Ψ_{JB}	Junction-to-board characterization parameter		50.1	°C/W
R _{BLC} (both) Junction-to-ambient thermal resistance 25.4 °C/W R _{BC(Dipo)} Junction-to-case (top) thermal resistance 25.4 °C/W R _{BU} Junction-to-board thermal resistance 47.75 °C/W Ψ _{JT} Junction-to-board characterization parameter 11.6 °C/W R _{BUC(Dot)} Junction-to-case (bottom) thermal resistance 9.0 °C/W R _{BU} Junction-to-case (top) thermal resistance 38.7 °C/W R _{BUC(Dot)} Junction-to-board thermal resistance 31.1 °C/W R _{BU} Junction-to-board thermal resistance 31.1 °C/W R _{BUC(Dot)} Junction-to-board thermal resistance 11.6 °C/W R _{BUC(Dot)} Junction-to-board thermal resistance 31.1 °C/W R _{BUC(Dot)} Junction-to-case (bottom) thermal resistance 9.1 °C/W R _{BUC(Dot)} Junction-to-case (bottom) thermal resistance 9.1 °C/W R _{BUC(Dot)} Junction-to-case (bottom) thermal resistance 42.6 °C/W W _{JT} Junction-to-board characterization parameter 42.2 °C/W R _{BUC(Dot)} Junction-to-board thermal resistance 47.1 °C/W R _{BUC(Dot)} Junction-t	R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance		N/A	°C/W
R _{BLCItop} Junction-to-case (top) thermal resistance 25.4 °C/W R _{BB} Junction-to-board thermal resistance 40.7 Junction-to-top characterization parameter 17.5 °C/W R _{BLCIbot1} Junction-to-board characterization parameter 17.5 °C/W R _{BLCIbot2} Junction-to-case (bottom) thermal resistance 9.0 °C/W R _{BLCIbot3} Junction-to-case (top) thermal resistance 38.7 °C/W R _{BLCIbot3} Junction-to-case (top) thermal resistance 38.7 °C/W R _{BLCIbot3} Junction-to-case (top) thermal resistance 18.7 °C/W R _{BLCIbot3} Junction-to-case (bottom) thermal resistance 9.1 °C/W R _{BLCIbot3} Junction-to-case (bottom) thermal resistance 80.6 °C/W R _{BLCIbot3} Junction-to-case (bottom) thermal resistance 80.6 °C/W R _{BLCIbot3} Junction-to-case (bottom) thermal resistance 80.6 °C/W R _{BLCIbot3} Junction-to-board characterization parameter 42.2 °C/W R _{BLCIbot3} Junction-to-case (bottom) thermal resistance N/A °C/W <td></td> <td>Junction-to-ambient thermal resistance</td> <td></td> <td>34.6</td> <td>°C/W</td>		Junction-to-ambient thermal resistance		34.6	°C/W
R _{B,IB} Junction-to-board thermal resistance VGFN-48 (RGZ) 17.5 °C/W Ψ _{JB} Junction-to-to-pot haracterization parameter 1.6 °C/W Ψ _{JB} Junction-to-board characterization parameter 17.5 °C/W R _{BLC(Det)} Junction-to-case (bottom) thermal resistance 9.0 °C/W R _{BLC} (Det) Junction-to-case (top) thermal resistance 38.7 °C/W R _{BLD} Junction-to-case (top) thermal resistance 38.7 °C/W R _{BLD} Junction-to-board thermal resistance 18.7 °C/W R _{BLD} Junction-to-case (bottom) thermal resistance 9.1 °C/W R _{BLC} (Det) Junction-to-case (bottom) thermal resistance 80.6 °C/W R _{BLC} (Det) Junction-to-board thermal resistance 39.9 °C/W W _{JB} Junction-to-case (bottom) thermal resistance N/A °C/W R _{BLC} (Det) Junction-to-case (bottom) thermal resistance N/A °C/W R _{BLC} (Det) Junction-to-case (bottom) thermal resistance N/A °C/W R _{BLC} (Det) Junction-to-case (bottom) therma		Junction-to-case (top) thermal resistance		25.4	°C/W
Ψ _{JT} Junction-to-to-top characterization parameter 1.6 °C/W Ψ _{JB} Junction-to-board characterization parameter 17.5 °C/W R _{LIA} Junction-to-board characterization parameter 9.0 °C/W R _{LIA} Junction-to-case (bottom) thermal resistance 38.7 °C/W R _{LIA} Junction-to-case (top) thermal resistance 38.7 °C/W R _{LIA} Junction-to-board thermal resistance 18.7 °C/W R _{LIC} (bor) Junction-to-to-poard characterization parameter 18.7 °C/W R _{LIC} (bor) Junction-to-board characterization parameter 9.1 °C/W R _{LIC} (bor) Junction-to-case (bottom) thermal resistance 80.6 °C/W R _{LIC} (bor) Junction-to-board thermal resistance 42.6 °C/W W _{JB} Junction-to-board thermal resistance 42.6 °C/W R _{LIC} (bor) Junction-to-case (bottom) thermal resistance N/A °C/W R _{LIC} (bor) Junction-to-case (bottom) thermal resistance 47.1 °C/W R _{LIC} (bor) Junction-to-board characterization parameter		Junction-to-board thermal resistance) (OFN 40 (DOZ)	17.5	°C/W
R _{BLC(bot)} Junction-to-case (bottom) thermal resistance 9.0 °C/W R _{BLA} Junction-to-case (top) thermal resistance 38.7 °C/W R _{BUB} Junction-to-case (top) thermal resistance 31.1 °C/W W _{JB} Junction-to-board thermal resistance 18.7 °C/W W _{JB} Junction-to-board characterization parameter 18.7 °C/W R _{BLC(bot)} Junction-to-board characterization parameter 18.7 °C/W R _{BLC(bot)} Junction-to-board characterization parameter 9.1 °C/W R _{BLC(bot)} Junction-to-case (bottom) thermal resistance 80.6 °C/W R _{BLC(bot)} Junction-to-case (bottom) thermal resistance 39.9 °C/W R _{BLC(bot)} Junction-to-board characterization parameter 42.6 °C/W R _{BLC(bot)} Junction-to-case (bottom) thermal resistance N/A °C/W R _{BLC(bot)} Junction-to-case (bottom) thermal resistance 47.1 °C/W R _{BLC} Junction-to-board thermal resistance 40.4 °C/W W _{JB} Junction-to-board thermal resistance	Ψ_{JT}	Junction-to-top characterization parameter	VQFN-48 (RGZ)	1.6	°C/W
R _{BLA} Junction-to-ambient thermal resistance 38.7 °CM R _{BLIC(top)} Junction-to-case (top) thermal resistance 31.1 °CM R _{BLIB} Junction-to-board thermal resistance 18.7 °CM Ψ _{JT} Junction-to-loop characterization parameter 18.7 °CM Ψ _{JB} Junction-to-board characterization parameter 18.7 °CM R _{BLA} Junction-to-board characterization parameter 9.1 °CM R _{BLA} Junction-to-ambient thermal resistance 80.6 °CM R _{BLA} Junction-to-board thermal resistance 39.9 °CM R _{BLA} Junction-to-board thermal resistance 39.9 °CM R _{BLA} Junction-to-board characterization parameter 42.6 °CM Ψ _{JT} Junction-to-board characterization parameter 42.2 °CM R _{BLC(bot)} Junction-to-board thermal resistance 40.4 °CM R _{BLC(bot)} Junction-to-board characterization parameter 23.7 °CM R _{BLC(bot)} Junction-to-board thermal resistance 92.8 °CM	Ψ_{JB}	Junction-to-board characterization parameter		17.5	°C/W
R _{BLA} Junction-to-ambient thermal resistance 38.7 °CM R _{BLIC(top)} Junction-to-case (top) thermal resistance 31.1 °CM R _{BLIB} Junction-to-board thermal resistance 18.7 °CM Ψ _{JT} Junction-to-loop characterization parameter 18.7 °CM Ψ _{JB} Junction-to-board characterization parameter 18.7 °CM R _{BLA} Junction-to-board characterization parameter 9.1 °CM R _{BLA} Junction-to-ambient thermal resistance 80.6 °CM R _{BLA} Junction-to-board thermal resistance 39.9 °CM R _{BLA} Junction-to-board thermal resistance 39.9 °CM R _{BLA} Junction-to-board characterization parameter 42.6 °CM Ψ _{JT} Junction-to-board characterization parameter 42.2 °CM R _{BLC(bot)} Junction-to-board thermal resistance 40.4 °CM R _{BLC(bot)} Junction-to-board characterization parameter 23.7 °CM R _{BLC(bot)} Junction-to-board thermal resistance 92.8 °CM	R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance		9.0	°C/W
R _{0,UC(top)} Junction-to-board thermal resistance 31.1 °C/W R _{0,UB} Junction-to-board thermal resistance 18.7 °C/W Ψ _{JT} Junction-to-board characterization parameter 18.7 °C/W Ψ _{JB} Junction-to-board characterization parameter 18.7 °C/W R _{0,UC(top)} Junction-to-case (bottom) thermal resistance 80.6 °C/W R _{0,UC} (top) Junction-to-case (top) thermal resistance 80.6 °C/W R _{0,UC} (top) Junction-to-board thermal resistance 39.9 °C/W W _{JT} Junction-to-board characterization parameter 42.6 °C/W R _{0,UC} (top) Junction-to-case (bottom) thermal resistance 42.6 °C/W R _{0,UC} (top) Junction-to-case (bottom) thermal resistance N/A °C/W R _{0,UC} (top) Junction-to-case (top) thermal resistance 40.4 °C/W R _{0,UC} (top) Junction-to-board characterization parameter 40.4 °C/W W _{1,T} Junction-to-case (bottom) thermal resistance 9.3 °C/W R _{0,UC} (top) Junction-to-board characterization param		Junction-to-ambient thermal resistance		38.7	°C/W
R _{BJB} Junction-to-board thermal resistance V _{JT} Junction-to-top characterization parameter V _A F 18.7 °C/W W _{JB} Junction-to-bop characterization parameter 18.7 °C/W R _{BJC(bpo)} Junction-to-case (bottom) thermal resistance 9.1 °C/W R _{BJA} Junction-to-case (top) thermal resistance 80.6 °C/W R _{BJB} Junction-to-board thermal resistance 39.9 °C/W W _{JT} Junction-to-board thermal resistance 42.6 °C/W R _{BJC(bpo)} Junction-to-board characterization parameter 42.2 °C/W R _{BJC(bpo)} Junction-to-case (bottom) thermal resistance 47.1 °C/W R _{BJC(bpo)} Junction-to-case (top) thermal resistance 47.1 °C/W R _{BJC(bpo)} Junction-to-board thermal resistance 40.4 °C/W W _{JT} Junction-to-board characterization parameter 23.7 °C/W W _{JB} Junction-to-case (bottom) thermal resistance 92.8 °C/W R _{BLC(bpo)} Junction-to-case (bottom) thermal resistance 92.8 °C/W		Junction-to-case (top) thermal resistance		31.1	°C/W
Ψ _{JT} Junction-to-top characterization parameter VGPN-32 (RRB) 1.6 °C/W Ψ _{JB} Junction-to-board characterization parameter 18.7 °C/W R _{B,JC(bot)} Junction-to-case (bottom) thermal resistance 9.1 °C/W R _{B,JC(bot)} Junction-to-case (top) thermal resistance 80.6 °C/W R _{B,JC(bot)} Junction-to-board thermal resistance 42.6 °C/W R _{B,JC(bot)} Junction-to-top characterization parameter 42.6 °C/W W _{JB} Junction-to-board characterization parameter 42.2 °C/W R _{B,JA} Junction-to-case (bottom) thermal resistance N/A °C/W R _{B,JA} Junction-to-case (top) thermal resistance 47.1 °C/W R _{B,JA} Junction-to-board characterization parameter 40.4 °C/W W _{JT} Junction-to-board characterization parameter 23.7 °C/W R _{B,JC(bot)} Junction-to-case (bottom) thermal resistance 9.3 °C/W R _{B,JC(bot)} Junction-to-case (top) thermal resistance 92.8 °C/W R _{B,JC(bot)} Junction-to-ca		Junction-to-board thermal resistance		18.7	°C/W
R _{BJA} (C(toot)) Junction-to-case (bottom) thermal resistance 9.1 °C/W R _{BJA} Junction-to-ambient thermal resistance 80.6 °C/W R _{BJB} Junction-to-case (top) thermal resistance 39.9 °C/W W _{JT} Junction-to-board thermal resistance 42.6 °C/W W _{JB} Junction-to-top characterization parameter 42.6 °C/W R _{BJC(toot)} Junction-to-board characterization parameter 42.2 °C/W R _{BJC(toot)} Junction-to-case (bottom) thermal resistance N/A °C/W R _{BJA} Junction-to-ambient thermal resistance 47.1 °C/W R _{BJB} Junction-to-board characterization parameter 23.7 °C/W W _{JT} Junction-to-board characterization parameter 23.6 °C/W R _{BJA} Junction-to-case (bottom) thermal resistance 9.3 °C/W R _{BJA} Junction-to-case (bottom) thermal resistance 92.8 °C/W R _{BJA} Junction-to-board thermal resistance 92.8 °C/W R _{BJA} Junction-to-board characterization parameter YSSOP-20 (DGS20)		Junction-to-top characterization parameter	VQFN-32 (RHB)	1.6	°C/W
R _{BJA} (C(toot)) Junction-to-case (bottom) thermal resistance 9.1 °C/W R _{BJA} Junction-to-ambient thermal resistance 80.6 °C/W R _{BJB} Junction-to-case (top) thermal resistance 39.9 °C/W W _{JT} Junction-to-board thermal resistance 42.6 °C/W W _{JB} Junction-to-top characterization parameter 42.6 °C/W R _{BJC(toot)} Junction-to-board characterization parameter 42.2 °C/W R _{BJC(toot)} Junction-to-case (bottom) thermal resistance N/A °C/W R _{BJA} Junction-to-ambient thermal resistance 47.1 °C/W R _{BJB} Junction-to-board characterization parameter 23.7 °C/W W _{JT} Junction-to-board characterization parameter 23.6 °C/W R _{BJA} Junction-to-case (bottom) thermal resistance 9.3 °C/W R _{BJA} Junction-to-case (bottom) thermal resistance 92.8 °C/W R _{BJA} Junction-to-board thermal resistance 92.8 °C/W R _{BJA} Junction-to-board characterization parameter YSSOP-20 (DGS20)	Ψ_{JB}	Junction-to-board characterization parameter		18.7	°C/W
R _{BJA} Junction-to-ambient thermal resistance 80.6 °C/W R _{BJC(top)} Junction-to-case (top) thermal resistance 39.9 °C/W W _{JT} Junction-to-board thermal resistance 42.6 °C/W W _{JB} Junction-to-top characterization parameter 42.2 °C/W R _{BJC(top)} Junction-to-board characterization parameter N/A °C/W R _{BJC(top)} Junction-to-ambient thermal resistance 47.1 °C/W R _{BJA} Junction-to-case (top) thermal resistance 40.4 °C/W R _{BLC(top)} Junction-to-board thermal resistance 23.7 °C/W R _{BJA} Junction-to-board characterization parameter 23.6 °C/W W _{JT} Junction-to-board characterization parameter 93.3 °C/W R _{BJA} Junction-to-case (bottom) thermal resistance 92.8 °C/W R _{BJA} Junction-to-case (top) thermal resistance 92.8 °C/W R _{BJA} Junction-to-board thermal resistance 92.8 °C/W W _{JT} Junction-to-board characterization parameter YSSOP-20 (DGS20) <		Junction-to-case (bottom) thermal resistance		9.1	°C/W
Re _{BJB} Junction-to-board thermal resistance VSOP-28 (DGS28) 42.6 °C/W V _{JT} Junction-to-top characterization parameter 42.2 °C/W Re _{BJC} (bot) Junction-to-case (bottom) thermal resistance N/A °C/W Re _{BJC} (top) Junction-to-case (top) thermal resistance 47.1 °C/W Re _{BJC} (top) Junction-to-case (top) thermal resistance 47.1 °C/W 40.4		Junction-to-ambient thermal resistance		80.6	°C/W
R _{BUB} Junction-to-board thermal resistance VSOP-28 (DGS28) 42.6 °C/W Ψ _{JT} Junction-to-board characterization parameter 3.5 °C/W Ψ _{JB} Junction-to-board characterization parameter 42.2 °C/W R _{BJA} Junction-to-case (bottom) thermal resistance N/A °C/W R _{BJA} Junction-to-ambient thermal resistance 47.1 °C/W R _{BJB} Junction-to-board thermal resistance 40.4 °C/W W _{JT} Junction-to-board thermal resistance 23.7 °C/W W _{JB} Junction-to-board characterization parameter 23.6 °C/W R _{BJC} (bot) Junction-to-case (bottom) thermal resistance 92.8 °C/W R _{BJA} Junction-to-board thermal resistance 92.8 °C/W R _{BJB} Junction-to-board characterization parameter 49.6 °C/W W _{JT} Junction-to-board characterization parameter 49.6 °C/W R _{BJC} (top) Junction-to-case (bottom) thermal resistance N/A °C/W R _{BJA} Junction-to-ambient thermal resistance 49.6 °C/W R _{BJC} (top) Junction-to-ambient the	R _{θJC(top)}	Junction-to-case (top) thermal resistance		39.9	°C/W
Ψ _{JT} Junction-to-top characterization parameter VSSP-28 (DGS28) 3.5 °C/W Ψ _{JB} Junction-to-board characterization parameter 42.2 °C/W R _{BJC(bot)} Junction-to-case (bottom) thermal resistance N/A °C/W R _{BJA} Junction-to-asse (top) thermal resistance 47.1 °C/W R _{BJB} Junction-to-board thermal resistance 40.4 °C/W W _{JT} Junction-to-board characterization parameter 23.7 °C/W W _{JT} Junction-to-board characterization parameter 23.6 °C/W R _{BJA} Junction-to-case (bottom) thermal resistance 9.3 °C/W R _{BJA} Junction-to-case (top) thermal resistance 92.8 °C/W R _{BJB} Junction-to-board thermal resistance 49.6 °C/W W _{JT} Junction-to-board characterization parameter 49.6 °C/W W _{JB} Junction-to-board characterization parameter 49.6 °C/W R _{BJA} Junction-to-case (bottom) thermal resistance N/A °C/W R _{BJA} Junction-to-case (top) thermal resistance 49.6 °C/W R _{BJA} Junction-to-board t		Junction-to-board thermal resistance	\(\(\text{VOOOD 00 (DOOON)}\)	42.6	°C/W
Relochot Junction-to-case (bottom) thermal resistance N/A °C/W RelA Junction-to-case (top) thermal resistance 47.1 °C/W RelA Junction-to-case (top) thermal resistance 40.4 °C/W RelAB Junction-to-board thermal resistance 23.7 °C/W WJT Junction-to-board characterization parameter 23.6 °C/W RelAC(bot) Junction-to-case (bottom) thermal resistance 9.3 °C/W RelAC(bot) Junction-to-case (top) thermal resistance 92.8 °C/W RelAC(bop) Junction-to-case (top) thermal resistance 35.5 °C/W RelAB Junction-to-board thermal resistance 49.6 °C/W WJT Junction-to-case (bottom) thermal resistance N/A °C/W RelAC(bot) Junction-to-case (bottom) thermal resistance N/A °C/W RelAC(bot) Junction-to-case (bottom) thermal resistance N/A °C/W RelAC(top) Junction-to-case (bottom) thermal resistance 49.6 °C/W RelAC(top) Junction-to-case (top) thermal resistance 49.6 °C/W RelAC(top) Junction-to-case (top) thermal r		Junction-to-top characterization parameter	VSSUP-28 (DGS28)	3.5	°C/W
$\begin{array}{llllllllllllllllllllllllllllllllllll$	Ψ_{JB}	Junction-to-board characterization parameter		42.2	°C/W
$\begin{array}{llllllllllllllllllllllllllllllllllll$	R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$\begin{array}{cccccccccccccccccccccccccccccccccccc$		Junction-to-ambient thermal resistance		47.1	°C/W
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		40.4	°C/W
$\begin{array}{c} \Psi_{JT} & \text{Junction-to-top characterization parameter} \\ \Psi_{JB} & \text{Junction-to-board characterization parameter} \\ \Psi_{JB} & \text{Junction-to-board characterization parameter} \\ R_{\theta,JC(bot)} & \text{Junction-to-case (bottom) thermal resistance} \\ R_{\theta,JA} & \text{Junction-to-case (top) thermal resistance} \\ R_{\theta,JC(top)} & \text{Junction-to-case (top) thermal resistance} \\ \Psi_{JT} & \text{Junction-to-board thermal resistance} \\ \Psi_{JB} & \text{Junction-to-board characterization parameter} \\ R_{\theta,JC(bot)} & \text{Junction-to-board characterization parameter} \\ R_{\theta,JC(bot)} & \text{Junction-to-case (bottom) thermal resistance} \\ R_{\theta,JA} & \text{Junction-to-case (bottom) thermal resistance} \\ R_{\theta,JA} & \text{Junction-to-case (top) thermal resistance} \\ R_{\theta,JA} & \text{Junction-to-case (top) thermal resistance} \\ R_{\theta,JC(top)} & \text{Junction-to-case (top) thermal resistance} \\ R_{\theta,JB} & \text{Junction-to-board thermal resistance} \\ R_{\theta,JB} & \text{Junction-to-board thermal resistance} \\ W_{JT} & \text{Junction-to-board characterization parameter} \\ W_{JB} & \text{Junction-to-board characterization parameter} \\ \end{array} \begin{array}{c} 2.4 & ^{\circ}C/W \\ 23.6 & ^{\circ}C/$	$R_{\theta JB}$	Junction-to-board thermal resistance	\(\OFN 24 \(\mathred{POF}\)	23.7	°C/W
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Ψ_{JT}	Junction-to-top characterization parameter	VQFN-24 (RGE)	2.4	°C/W
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	Ψ_{JB}	Junction-to-board characterization parameter		23.6	°C/W
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance		9.3	°C/W
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	$R_{\theta JA}$	Junction-to-ambient thermal resistance		92.8	°C/W
$\begin{array}{cccccccccccccccccccccccccccccccccccc$		Junction-to-case (top) thermal resistance		35.5	°C/W
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	$R_{\theta JB}$	Junction-to-board thermal resistance	V660B 30 (DC630)	49.6	°C/W
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Ψ_{JT}	Junction-to-top characterization parameter	V330F-20 (DG320)	1.3	°C/W
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Ψ_{JB}	Junction-to-board characterization parameter		49.1	°C/W
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
R _{θJB} Junction-to-board thermal resistance Ψ _{JT} Junction-to-top characterization parameter Ψ _{JB} Junction-to-board characterization parameter 23.6 °C/W 1.4 °C/W 23.6 °C/W	$R_{\theta JA}$	Junction-to-ambient thermal resistance		49.6	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance WQFN-20 (RUK) 23.6 °C/W Ψ _{JT} Junction-to-top characterization parameter 1.4 °C/W Ψ _{JB} Junction-to-board characterization parameter 23.6 °C/W	R _{θJC(top)}	Junction-to-case (top) thermal resistance		48.9	°C/W
$\Psi_{ m JT}$ Junction-to-top characterization parameter 1.4 °C/W $\Psi_{ m JB}$ Junction-to-board characterization parameter 23.6 °C/W	$R_{\theta JB}$	Junction-to-board thermal resistance	MOEN 30 (BLIK)	23.6	°C/W
	Ψ_{JT}	Junction-to-top characterization parameter	VVQFIN-20 (NON)	1.4	°C/W
R _{eJC(bot)} Junction-to-case (bottom) thermal resistance 9.2 °C/W	Ψ_{JB}	Junction-to-board characterization parameter		23.6	°C/W
	$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		9.2	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.



7.5 Supply Current Characteristics

7.5.1 RUN/SLEEP Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled.

	PARAMETER	MCLK	-40	°C	25	°C	85	°C	105	5°C	125	s°C	UNIT
	PARAMETER	WICLK	TYP	MAX	UNII								
RUN Mode													
IDD _{RUN}	MCLK=SYSOSC, CoreMark, execute from flash	32MHz	2.9		2.9		2.9		2.9		2.9		mA
IDD _{RUN} ,	MCLK=SYSOSC, While(1), execute from flash	32MHz	52	58	53	59	53	59	54	60	54	60	uA/Mhz
per MHz	MCLK=SYSOSC, CoreMark, execute from flash	SZIVIFIZ	90		91		91		91		91		UAVIVITIZ
SLEEP Mod	de												
IDD _{SLEEP}	MCLK=SYSOSC, CPU is halted	32MHz	1332	1455	1346	1468	1358	1479	1362	1486	1370	1490	uA
IDD _{SLEEP}	MCLK=LFCLK, CPU is halted	32kHz	524	591	529	595	542	643	549	650	558	660	uA

7.5.2 STOP/STANDBY Modes

VDD=3.3V unless otherwise noted. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals not noted are disabled.

	PARAMETER	ULPCLK	-40	°C	25	°C	85	°C	10	5°C	125	s°C	UNIT
	FARAMETER	OLFOLK	TYP	MAX	ONII								
STOP Mod	e		•										
IDD _{STOP0}	SYSOSC=32MHz, DISABLESTOP=0	4MHz	415	456	422	459	431	473	434	476	436	481	uA
IDD _{STOP2}	SYSOSC off, DISABLESTOP=1, ULPCLK=LFCLK	32kHz	81	91	84	93	93	118	96	121	99	127	uA
STANDBY	Mode		•										
	LFXT and RTC enabled		2.6	4.1	2.7	4.1	7.9	27	11	30	16	34	uA
	LFOSC and IWDT enabled		2.4	3.8	2.5	3.8	7.6	27	10	30	13	35	uA
IDD _{STBY0}	LFXT and RTC enabled, IWDT enabled		2.6	4.1	2.7	4.1	8.0	27	11	30	16	34	uA
	STOPCLKSTBY=0, TIMG0 enabled		2.3	3.9	2.4	3.9	7.6	27	10	29	15	35	
IDD	STOPCLKSTBY=1, TIMG0 enabled	32kHz	2.1	3.4	2.2	3.4	7.1	26	10	29	15	34	uA
IDD _{STBY1}	STOPCLKSTBY=1, GPIOA enabled		2.0	2.6	2.1	2.6	7.1	26	10	29	13	34	

7.5.3 SHUTDOWN Mode

VDD=3.3V unless otherwise noted. All inputs tied to 0V or VDD. Outputs do not source or sink any current. Core regulator is powered down.

PARAMETER		-40°C		25°C		85°C		105°C		125°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	ONIT
IDD _{SHDN}	Supply current in SHUTDOWN mode	54		68		255		524		1362		nA

7.6 Power Supply Sequencing

7.6.1 Power Supply Ramp

Figure 7-1 gives the relationship of POR- POR+, BOR0-, and BOR0+ during power-up and power-down.



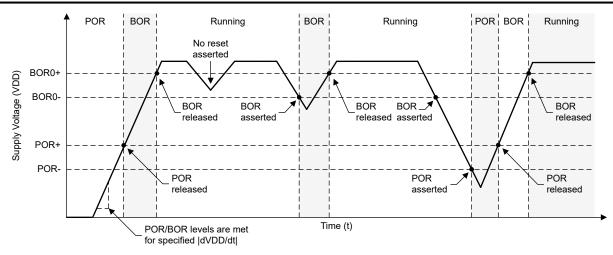


Figure 7-1. Power Cycle POR/BOR Conditions - VDD

7.6.2 POR and BOR

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		Rising			0.1	V/us
dVDD/dt	VDD (supply voltage) slew rate	Falling (1)			0.01	v/uS
		Falling, STANDBY			0.1	V/ms
V _{POR+}	Power-on reset voltage level	Rising	0.95	1.3	1.59	V
V _{POR-}	Power-off reset voltage level	Falling	0.9	1.25	1.54	V
V _{HYS, POR}	POR hysteresis		30	58	74	mV
V _{BOR0+,}		-40 °C ≤ Ta ≤ 25 °C, Cold start, rising	1.50	1.56	1.63	
COLD	Brown-out reset voltage level 0 (default level)	25 °C ≤ Ta ≤ 125 °C, Cold start, rising	1.51	1.58	1.65	V
V _{BOR0+}	Drown out 1999t voltage level o (acidalit level)	Rising (1)	1.56	1.59	1.62	·
V _{BOR0-}		Falling (1)	1.55	1.58	1.61	
V _{BOR0, STBY}		STANDBY mode	1.51	1.56	1.61	
V _{BOR1+}		Rising (1)	2.13	2.17	2.21	
V _{BOR1} -	Brown-out-reset voltage level 1	Falling (1)	2.10	2.14	2.18	V
V _{BOR1, STBY}		STANDBY mode	2.06	2.13	2.20	
V _{BOR2+}		Rising (1)	2.73	2.77	2.82	
V _{BOR2} -	Brown-out-reset voltage level 2	Falling (1)	2.7	2.74	2.79	V
V _{BOR2, STBY}		STANDBY mode	2.62	2.71	2.8	
V _{BOR3+}		Rising (1)	2.88	2.96	3.04	
V _{BOR3} -	Brown-out-reset voltage level 3	Falling (1)	2.85	2.93	3.01	V
V _{BOR3, STBY}		STANDBY mode	2.82	2.92	3.02	
\ /	Duranta and march burstons in	Level 0		15	21	
$V_{HYS,BOR}$	Brown-out reset hysteresis	Levels 1-3		34	40	mV
T _{PD, BOR}	BOR propagation delay	RUN/SLEEP/STOP mode			5	us
· FD, DOK		STANDBY mode			100	us

(1) Device operating in RUN, SLEEP, or STOP mode.

7.7 Flash Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
VDD _{PGM/ERASE}	Program and erase supply voltage		1.62		3.6	V
IDD _{ERASE}	Supply current from VDD during erase operation	Supply current delta		2		mA
IDD _{PGM}	Supply current from VDD during program operation	Supply current delta		2.5		mA
Endurance						
NWEC _(LOWER)	Erase/program cycle endurance (lower 32kB flash) (1)		100			k cycles
NWEC _(UPPER)	Erase/program cycle endurance (remaining flash) (1)		10			k cycles
NE _(MAX)	Total erase operations before failure (2)		802			k erase operations
NW _(MAX)	Write operations per word line before sector erase ⁽³⁾				83	write operations
Retention						
t _{RET_85}	Flash memory data retention	-40°C ≤T _j ≤ 85°C	60			years
t _{RET_105}	Flash memory data retention	-40°C ≤T _j ≤ 105°C	11.4			years
Program and Era	ase Timing					
t _{PROG (WORD, 64)}	Program time for flash word (4) (6)			50	275	μs
t _{PROG} (SEC, 64)	Program time for 1kB sector (5) (6)			6.4		ms
t _{ERASE} (SEC)	Sector erase time	≤2k erase/program cycles, T _j ≥25°C		4	20	ms
t _{ERASE} (SEC)	Sector erase time	≤10k erase/program cycles, T _j ≥25°C		20	150	ms
t _{ERASE} (SEC)	Sector erase time	≤10k erase/program cycles		20	200	ms
t _{ERASE (BANK)}	Bank erase time	≤10k erase/program cycles		22	220	ms

- (1) The lower 32kB flash address space supports higher erase/program endurance to enable EEPROM emulation applications. On devices with <=32kB flash memory, the entire flash memory supports NWEC_(LOWER) erase/program cycles.
- (2) Total number of cumulative erase operations supported by the flash before failure. A sector erase or bank erase operation is considered to be one erase operation.
- (3) Maximum number of write operations allowed per word line before the word line must be erased. If additional writes to the same word line are required, a sector erase is required once the maximum number of write operations per word line is reached.
- (4) Program time is defined as the time from when the program command is triggered until the command completion interrupt flag is set in the flash controller.
- (5) Sector program time is defined as the time from when the first word program command is triggered until the final word program command completes and the interrupt flag is set in the flash controller. This time includes the time needed for software to load each flash word (after the first flash word) into the flash controller during programming of the sector.
- (6) Flash word size is 64 data bits (8 bytes). On devices with ECC, the total flash word size is 72 bits (64 data bits plus 8 ECC bits).

7.8 Timing Characteristics

VDD=3.3V, T_a=25 °C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT		
Wakeup Timing							
t _{WAKE} , SLEEP	Wakeup time from SLEEP to RUN (1)		2		cycles		
t _{WAKE,} STOP0	Wakeup time from STOP0 to RUN (SYSOSC enabled) (1)		14		us		
t _{WAKE} , STOP2	Wakeup time from STOP2 to RUN (SYSOSC disabled) (1)		13		us		



VDD=3.3V, T_a=25 °C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
t _{WAKE} , STBY0	Wakeup time from STANDBY to RUN		15		us
t _{WAKE} ,	Wakeup time from SHUTDOWN to RUN	Fast boot enabled	255		us
t _{WAKE} ,	Wakeup time from SHUTDOWN to RUN	Fast boot disabled	265		us
Asynchr	onous Fast Clock Request Timing				
t _{DELAY}	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is SLEEP2	0.9		us
t _{DELAY}	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STOP0	2.4		us
t _{DELAY}	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STOP2	0.9		us
t _{DELAY}	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STANDBY1	3.2		us
Startup 7	Гiming				
t _{START,}	Device cold start-up time from reset/	Fast boot enabled	241		us
RESET	power-up ⁽²⁾	Fast boot disabled	284		us
NRST Ti	ming				
t _{RST.}	Minimum pulse length on NRST pin to	ULPCLK≥4MHz	2		us
BOOTRST	generate BOOTRST	ULPCLK=32kHz	100		us
t _{RST, POR}	Minimum pulse length on NRST pin to generate POR		1		s

⁽¹⁾ The wake-up time is measured from the edge of an external signal (GPIO wake-up event) to the time that the first CPU instruction is executed, with the GPIO glitch filter disabled (FILTEREN=0x0) and fast wake enabled (FASTWAKEONLY=1)

7.9 Clock Specifications

7.9.1 System Oscillator (SYSOSC)

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{SYSOSC}	Factory trimmed SYSOSC frequency	SYSOSCCFG.FREQ=00 (BASE)		32		MHz
	SYSOSC frequency accuracy when	SETUSEFCL=1, T _a = 25 °C	0		1.0	
	frequency correction loop (FCL) is enabled ⁽¹⁾ ⁽²⁾	SETUSEFCL=1, -40 °C ≤ T _a ≤ 125 °C	-2.1		1.6	%
f _{SYSOSC}	SYSOSC accuracy when frequency correction loop (FCL) is disabled, 32MHz (1) (2)	SETUSEFCL=0, SYSOSCCFG.FREQ=00, -40 °C \leq T _a \leq 125 °C	-2.6		1.8	%
t _{settle,} sysosc	Settling time to target accuracy (3)	SETUSEFCL=1			30	us

⁽¹⁾ SYSOSC accuracy is measured in the default power-up state, with MCLK = SYSOSC and the CPU running a while(1) loop.

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⁽²⁾ The start-up time is measured from the time that VDD crosses VBOR0+ (cold start-up) to the time that the first instruction of the user program is executed.

⁽²⁾ SYSOSC is measured with the internal FCC counter using an external 1ms pulse as the measurement trigger.

⁽³⁾ When SYSOSC is waking up (for example, when exiting a low power mode) and FCL is enabled, the SYSOSC will initially undershoot the target frequency f_{SYSOSC} by an additional error of up to f_{settle,SYSOSC} for the time t_{settle,SYSOSC}, after which the target accuracy is achieved.

7.9.2 Low Frequency Oscillator (LFOSC)

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{i FOSC}	LFOSC frequency			32768		Hz
	LFOSC accuracy	-40 °C ≤ T _a ≤ 125 °C	-5		5	%
		-40 °C ≤ T _a ≤ 85 °C	-3		3	%
I _{LFOSC}	LFOSC current consumption			300		nA
t _{start,} LFOSC	LFOSC start-up time			1		ms

7.9.3 Low Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low frequen	cy crystal oscillator (LFXT)					
f _{LFXT}	LFXT frequency			32768		Hz
DC _{LFXT}	LFXT duty cycle		30 70		70	%
OA _{LFXT}	LFXT crystal oscillation allowance		419			kΩ
C _{L, eff}	Integrated effective load capacitance ⁽¹⁾			1		pF
t _{start, LFXT}	LFXT start-up time			1000		ms
I _{LFXT}	LFXT current consumption	XT1DRIVE=0, LOWCAP=1	300			nA
Low frequen	cy digital clock input (LFCLK_IN)					
f _{LFIN}	LFCLK_IN frequency (2)	SETUSEEXLF=1	29491	32768	36045	Hz
DC _{LFIN}	LFCLK_IN duty cycle (2)	SETUSEEXLF=1	40		60	%
LFCLK Moni	tor				'	
f _{FAULTLF}	LFCLK monitor fault frequency (3)	MONITOR=1	2800	4200	8400	Hz

⁽¹⁾ This includes parasitic bond and package capacitance (≈2pF per pin), calculated as C_{LFXIN}×C_{LFXOUT}/(C_{LFXIN}+C_{LFXOUT}), where C_{LFXIN} and C_{LFXOUT} are the total capacitance at LFXIN and LFXOUT, respectively.

7.9.4 High Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP MA	X UNIT
High frequen	cy crystal oscillator (HFXT)				
f _{HFXT}	HFXT frequency	HFXTRSEL=00	4		8 MHz
f _{HFXT}	HFXT frequency	HFXTRSEL=01	8.01	1	6 MHz
f _{HFXT}	HFXT frequency	HFXTRSEL=10	16.01	3	2 MHz
DC _{HFXT}	HFXT duty cycle	HFXTRSEL=00	40	6	5 %
DC _{HFXT}	HFXT duty cycle	HFXTRSEL=01	40	6	0 %
DC _{HFXT}	HFXT duty cycle	HFXTRSEL=10	40	6	0 %
OA _{HFXT}	HFXT crystal oscillation allowance	HFXTRSEL=00 (4 to 8MHz range)		2	kΩ
C _{L, eff}	Integrated effective load capacitance (1)			1	pF
t _{start, HFXT}	HFXT start-up time ⁽²⁾	HFXTRSEL=11, 32MHz crystal		0.5	ms

⁽²⁾ The digital clock input (LFCLK_IN) accepts a logic level square wave clock.

⁽³⁾ The LFCLK monitor may be used to monitor the LFXT or LFCLK_IN. It will always fault below the MIN fault frequency, and will never fault above the MAX fault frequency.



over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{HFXT}	HFXT current consumption ⁽²⁾	f_{HFXT} =4MHz, R_m =300 Ω , C_L =12pF		100		uA
I _{HFXT}	HFXT current consumption ⁽²⁾	$\begin{split} &f_{HFXT}{=}32MHz,\\ &R_{m}{=}30\Omega,\\ &C_{L}{=}12pF,\\ &C_{m}{=}6.26fF,\\ &L_{m}{=}1.76mH \end{split}$	600		uA	
High frequency	digital clock input (HFCLK_IN)					
f _{HFIN}	HFCLK_IN frequency (3)	USEEXTHFCLK =1	4		32	MHz
DC _{HFIN}	HFCLK_IN duty cycle (3)	USEEXTHFCLK =1	40		60	%

- (1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as C_{HFXIN}×C_{HFXOUT}/(C_{HFXIN}+C_{HFXOUT}), where C_{HFXIN} and C_{HFXOUT} are the total capacitance at HFXIN and HFXOUT, respectively.
- (2) The HFXT startup time (t_{start, HFXT}) is measured from the time the HFXT is enabled until stable oscillation for a typical crystal. Start-up time is dependent upon crystal frequency and crystal specifications. Current consumption increases with higher RSEL and start up time is decreases with higher RSEL.
- (3) The digital clock input (HFCLK_IN) accepts a logic level square wave clock.

7.10 Digital IO

7.10.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		ODIO (1)	VDD≥1.62V	0.7*VDD		5.5	V
V _{IH}	High level input voltage	ODIO (1)	VDD≥2.7V	2		5.5	V
- 111	, ng. rever input vertage	All I/O except ODIO & Reset	VDD≥1.62V	0.7*VDD		5.5	V
		ODIO	VDD≥1.62V	-0.3		5.5 5.5 VDD+0.3 0.3*VDD 0.8 0.3*VDD	V
V _{IL}	Low level input voltage	ODIO	VDD≥2.7V	-0.3		0.8	V
- 12		All I/O except ODIO & Reset	VDD≥1.62V	D≥1.62V -0.3 0.05*VDD 0.1*VDD		0.3*VDD	V
		ODIO		0.05*VDD			V
V _{HYS}	Hysteresis	All I/O except ODIO		0.1*VDD			V
I _{lkg}	High-Z leakage current	SDIO ⁽²⁾ (3)				50 ⁽⁴⁾	nA
R _{PU}	Pull up resistance	All I/O except ODIO			40		kΩ
R _{PD}	Pull down resistance				40		kΩ
Cı	Input capacitance				5		pF
V	Low level output voltage	SDIO	VDD≥2.7V, I _{IO} _{,max} =6mA VDD≥1.71V, I _{IO} _{,max} =2mA			0.4	V
V _{OL}	Low level output voltage	ODIO	VDD≥2.7V, I _{OL,max} =8mA VDD≥1.71V, I _{OL,max} =4mA			0.5	v
V	High level output voltage	SDIO	VDD ≥ 2.7V, I _{OH,max} = 6mA	VDD-0.5			V
V _{OH}	i ligit level output voltage	3010	VDD ≥ 1.71V, I _{OH,max} = 2mA	VDD-0.4			V

- (1) I/O Types: ODIO = 5V Tolerant Open-Drain, SDIO = Standard-Drive
- (2) The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
- (3) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

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This value is for SDIO not muxed with any analog inputs. If the SDIO is muxed with analog inputs then the leakage can be as high as 100nA.

7.10.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP MAX	UNIT
		SDIO (1)	VDD ≥ 1.71V, C _L = 20pF		16	
f _{max}	Port output frequency ODIO	3010 (7	VDD ≥ 2.7V, CL= 20pF		32	MHz
		ODIO	VDD ≥ 1.71V, FM ⁺ , CL= 20pF - 100pF		1	
t _r ,t _f	Output rise/fall time	SDIO	VDD ≥ 1.71V, C _L = 20pF		3.5	ns
t_r, t_f	Output rise/fall time	SDIO	VDD ≥ 2.7V, C _L = 20pF		6.6	ns
t _f	Output fall time	ODIO	VDD ≥ 1.71V, FM ⁺ , CL= 20pF-100pF	20*VDD/5.5	120	ns

(1) I/O Types: ODIO = 5V Tolerant Open-Drain , SDIO = Standard-Drive

7.11 Analog Mux VBOOST

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{VBST}		MCLK/ULPCLK is LFCLK		0.8		
		MCLK/ULPCLK is not LFCLK, SYSOSC frequency is 32MHz		20		uA
t _{START,VBST}	VBOOST startup time			12		us

7.12 ADC

7.12.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Vin _(ADC)	Analog input voltage range ⁽¹⁾	Applies to all ADC analog input pins	0		VDD	V	
		V _{R+} sourced from VDD		VDD		V	
V_{R+}	Positive ADC reference voltage	V _{R+} sourced from external reference pin (VREF+)	1.4		VDD	V	
		V _{R+} sourced from internal reference (VREF)		VREF		V	
V _{R-}	Negative ADC reference voltage			0		V	
Fs	ADC sampling frequency	RES = 0x0 (12-bit mode), External Reference			1.6	Msps	
F _S	ADC sampling frequency	RES = 0x1 (10-bit mode), External Reference			1.7	Msps	
Fs	ADC sampling frequency	RES = 0x2 (8-bit mode), External Reference			1.9	Msps	
	Operating supply current into VDD terminal	F _S = 1.6MSPS, External reference, V _{R+} = VDD		350			
I _(ADC)		F _S = 500ksps, Internal reference, V _{R+} = VREF = 2.5V		300		μA	
C _{S/H}	ADC sample-and-hold capacitance			0.22		pF	
Rin	ADC sampling switch resistance			15		kΩ	
ENOB	Effective number of bits	Internal reference, V _{R+} = VREF = 2.5V, F _{in} = 10KHz	9.4	10.2		bit	
ENOB	Effective number of bits	External reference, F _{in} = 10KHz ⁽²⁾	10	10.6		DIL	
ENOB	Effective number of bits	External reference, hardware averaging enabled (16 samples), F _{in} = 10KHz ⁽²⁾		11.8		bit	
CND	Ci	External reference (2)		67		-ID	
SNR	Signal-to-noise ratio	Internal reference, V _{R+} = VREF = 2.5V		64		dB	
SNR	Signal-to-noise ratio	External reference ⁽²⁾ , hardware averaging enabled (16 samples)		75		dB	



over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		External reference ⁽²⁾ , VDD = VDD _(min) to VDD _(max)		68		
PSRR _{DC}	Power supply rejection ratio, DC	VDD = VDD _(min) to VDD _(max) Internal reference, V_{R+} = VREF = 2.5V		61		dB
	Power supply rejection ratio, AC	External reference ⁽²⁾ , ΔVDD = 0.1 V at 1 kHz		61		
PSRR _{AC}		ΔVDD = 0.1 V at 1 kHz Internal reference, V _{R+} = VREF = 2.5V		49		dB
T _{wakeup}	ADC Wakeup Time	Assumes internal reference is active			5	us
V _{SupplyMon}	Supply Monitor voltage divider (VDD/3) accuracy	ADC input channel: Supply Monitor (3)	-1.5		+1.5	%
I _{SupplyMon}	Supply Monitor voltage divider current consumption	ADC input channel: Supply Monitor		10		uA

- (1) The analog input voltage range must be within the selected ADC reference voltage range V_{R+} to V_{R-} for valid conversion results.
- (2) All external reference specifications are measured with V_{R+} = VREF+ = VDD = 3.3V and V_{R-} = VREF- = VSS = 0V and external 1uF cap on VREF+ pin
- (3) Analog power supply monitor. Analog input on channel 15 is disconnected and is internally connected to the voltage divider which is VDD/3.

7.12.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TE	EST CONDITIONS	MIN	TYP	MAX	UNIT
f _{ADCCLK}	ADC clock frequency					32	MHz
t _{ADC trigger}	Software trigger minimum width		3			ADCCLK cycles	
t _{Sample_step}	Sampling time for step input	12-bit mode, R _S	= 50Ω, C _{pext} = 10pF	0.188			μs
t _{Sample_VREF}	Sample time with internal VREF input		ADC CHANNEL=29,12-bit mode, VDD as reference	10			μs
t _{Sample_SupplyMon}	Sample time with Supply Monitor (VDD/3)	12-bit mode		5			μs

7.12.3 Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all linearity parameters are measured using 12-bit resolution mode (unless otherwise noted)

	•	- ,		•	
	PARAMETER	TEST CONDITIONS	MIN	TYP MAX	UNIT
Eı	Integral linearity error (INL)	External reference (1)	-2.0	+2.0	LSB
E _D	Differential linearity error (DNL) Guaranteed no missing codes	External reference, 12-bit (1)	-1.0	+1.0	LSB
Eo	Offset error	External reference (1)	-5	5	mV
E _G	Gain error	External reference (1)	-6	6	LSB

(1) All external reference specifications are measured with VR+ = VREF+ = VDD = 3.3V and VR- = VREF- = VSS = 0V and external 1uF cap on VREF+ pin



7.12.4 Typical Connection Diagram

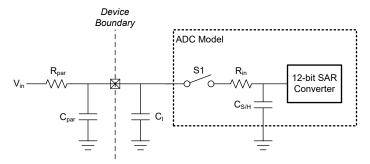


Figure 7-2. ADC Input Network

- 1. Refer to Electrical Characteristics for the values of Rin and CS/H
- 2. Refer to Electrical Characteristics for the value of C₁
- C_{par} and R_{par} represent the parasitic capacitance and resistance of the external ADC input circuitry

Use the following equations to solve for the minimum sampling time (T) required for an ADC conversion:

- $\begin{aligned} &\text{Tau} = (\mathsf{R}_{\mathsf{par}} + \mathsf{R}_{\mathsf{in}})^* \ \mathsf{C}_{\mathsf{S}/\mathsf{H}} + \mathsf{R}_{\mathsf{par}}^* (\mathsf{C}_{\mathsf{par}} + \mathsf{C}_{\mathsf{I}}) \\ &\mathsf{K} = \mathsf{In}(2^{\mathsf{n}}/\mathsf{Settling} \ \mathsf{error}) \mathsf{In}((\mathsf{C}_{\mathsf{par}} + \mathsf{C}_{\mathsf{I}})/\mathsf{C}_{\mathsf{S}/\mathsf{H}}) \end{aligned}$
- T (Min sampling time) = K*Tau

7.13 Temperature Sensor

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	ETER TEST CONDITIONS		TYP	MAX	UNIT
TS _{TRIM}	Factory trim temperature ⁽¹⁾	ADC and VREF configuration: RES=0 (12-bit mode), VRSEL=2h (internal VREF), BUFCONFIG=1h (1.4V VREF), ADC t _{Sample} =10µs	27 30 33		°C	
TS _c	Temperature coefficient		-2.05	-1.89	-1.75	mV/°C
t _{SET, TS}	Temperature sensor settling time (2)			2.5	10	us

- Higher absolute accuracy may be achieved through user calibration.
- This is the maximum time required for the temperature sensor to settle when measured by the ADC. It may be used to specify the minimum ADC sample time when measuring the temperature sensor.



7.14 VREF

7.14.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{VREF}	VREF operating supply current	BUFCONFIG = {0, 1}, No load		80	100	μA
TC _{VREF}	Temperature coefficient of VREF (1)	BUFCONFIG = {0, 1}			75	ppm/°C
TC _{drift}	Long term VREF drift	Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25°C			300	ppm
PSRR _{DC}	VREF Power supply rejection ratio, DC	VDD = 1.7 V to VDDmax, BUFCONFIG = 1	60	70		dB
FORKDC		VDD = 2.7 V to VDDmax, BUFCONFIG = 0	49	60		ub
\/	RMS noise at VREF output (0.1 Hz	BUFFCONFIG = 1		500		μVrms
V _{noise}	to 100 MHz)	BUFFCONFIG = 0		900		μνιιιιδ
ADC F _S	Max supported ADC sampling frequency	Using VREF as ADC reference			515	ksps
T _{startup}	VREF startup time	BUFCONFIG = {0, 1}, VDD = 2.8 V			30	us

⁽¹⁾ The temperature coefficient of the VREF output is the sum of TC_{VRBUF} and the temperature coefficient of the internal bandgap reference.

7.14.2 Voltage Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD .	Minimum supply voltage needed for	BUFCONFIG = 1	1.62			\/
VDD _{min}	VREF operation	BUFCONFIG = 0	2.7			V
VREF	Voltago reference output voltago	BUFCONFIG = 1	1.38	1.4	1.42	\/
VKEF	Voltage reference output voltage	BUFCONFIG = 0	2.46	2.5	2.54	V

7.15 Comparator (COMP)

7.15.1 Comparator Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Comparat	or Electrical Characteristics					
Vcm	Common mode input range		0		VDD	V
V _{offset}	Input offset voltage		-20		20	mV
		HYST=00h		0.4		
V	DC input bustanais	HYST=01h		10		ma\ /
V _{hys}	DC input hysteresis	HYST=02h		20		mV
		HYST=03h		30		
	Propagation delay, response	Output Filter off, Overdrive = 100 mV, High Speed Mode		32	50	ns
₹ _{PD_Is}	time	Output Filter off, Overdrive = 100 mV, Low Power Mode		1.2	4	μs
	Compositor analysis	Startup time to reach propagation delay specification, High Speed Mode			5	μs
t _{en}	Comparator enable time	Startup time to reach propagation delay specification, Low Power Mode			10	μs



over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, High Speed Mode		130	200	μА
I _{comp}	Comparator current consumption.	Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, Low Power Mode		0.85	2.7	μА
		Vcm = VDD/2, 100mV overdrive, comparator only. High Speed Mode		120	180	μΑ
		Vcm = VDD/2, 100mV overdrive, comparator only, Low Power Mode		0.7	2.1	μΑ
8-bit DAC El	ectrical Characteristics					
V _{dac}	DAC output range		0		VDD	V
V _{dac-code}	8-bit DAC output voltage for a given code	VIN = reference voltage into 8-bit DAC, code n = 0 to 255	(1	VIN × n+1) / 256		V
INL	Integral nonlinearity of 8-bit D	AC	-1		1	LSB
DNL	Differential nonlinearity of 8-bi	it DAC	-1		1	LSB
Gain error	Gain error of 8-bit DAC	Reference voltage = VDD	-2		2	% of FSR
Offset error	Offset error of 8-bit DAC		-5		5	mV
Output Impedance	8-bit DAC output impedance			50		kΩ
t _{dac_settle}	8-bit DAC settling time in static mode	DACCODE0 = 0 → 255, DAC output accurate to 1 LSB, DAC output on pin PA11, Cload = 15pF		6		μs
t _{dac_settle}	8-bit DAC settling time in static mode	DACCODE0 = 0 → 255, DAC output accurate to 1 LSB		1.5		μs

7.16 I2C

7.16.1 I2C Characteristics

over operating free-air temperature range (unless otherwise noted)

	DADAMETERS	TEST CONDITIONS	Standard	mode	Fast me	ode	Fast mod	e plus	UNIT
	PARAMETERS	TEST CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNII
f _{I2C}	I2C input clock frequency	I2C in Power Domain0	2	32	8	32	20	32	MHz
f _{SCL}	SCL clock frequency			0.1		0.4		1	MHz
t _{HD,STA}	Hold time (repeated) START		4		0.6		0.26		us
t _{LOW}	Low period of the SCL clock		4.7		1.3		0.5		us
t _{HIGH}	High period of the SCL clock		4		0.6		0.26		us
t _{SU,STA}	Setup time for a repeated START		4.7		0.6		0.26		us
t _{HD,DAT}	Data hold time		0		0		0		ns
t _{SU,DAT}	Data setup time		250		100		50		ns
t _{SU,STO}	Setup time for STOP		4		0.6		0.26		us
t _{BUF}	Bus free time between a STOP and START condition		4.7		1.3		0.5		us
t _{VD;DAT}	Data valid time			3.45		0.9		0.45	us
t _{VD;ACK}	Data valid acknowledge time			3.45		0.9		0.45	us



7.16.2 I2C Filter

over operating free-air temperature range (unless otherwise noted)

	PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
IOD		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

7.16.3 I²C Timing Diagram

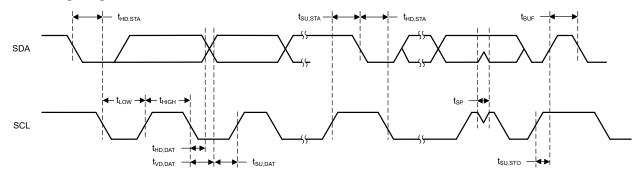


Figure 7-3. I2C Timing Diagram

7.17 SPI

7.17.1 SPI

over operating free-air temperature range (unless otherwise noted)

	PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI					•	
f _{SPI}	SPI clock frequency	Clock max speed = 32MHz 1.62 < VDD < 3.6V Controller mode			16	MHz
f _{SPI}	SPI clock frequency	Clock max speed = 32MHz 1.62 < VDD < 3.6V Peripheral mode			16	MHz
DC _{SCK}	SCK Duty Cycle		40	50	60	%
Controller			•		•	
t _{SCLK_H/L}	SCLK High or Low time		(tSPI/2) - 1	tSPI / 2	(tSPI/2) + 1	ns
t _{CS.LEAD}	CS lead-time, CS active to clock		1 SPI Clock			ns
t _{CS.LAG}	CS lag time, Last clock to CS inactive		1 SPI Clock			ns
t _{CS.ACC}	CS access time, CS active to PICO data out				1/2 SPI Clock	ns
t _{CS.DIS}	CS disable time, CS inactive to PICO high inpedance				1 SPI Clock	ns
4	POCL input data actus time (1)	2.7 < VDD < 3.6V, delayed sampling enabled	1			no
t _{su.cı}	POCI input data setup time (1)	1.62 < VDD < 2.7V, delayed sampling enabled	8			ns
4	POCI input data setup time (1)	2.7 < VDD < 3.6V, no delayed sampling	30			no
t _{su.cı}	POGI input data setup time (1)	1.62 < VDD < 2.7V, no delayed sampling	39			ns

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{HD.CI}	POCI input data hold time	No delayed sampling	0			ns
t _{VALID.CO}	PICO output data valid time (2)				16	ns
t _{HD.CO}	PICO output data hold time (3)		1			ns
Peripheral					'	
t _{CS.LEAD}	CS lead-time, CS active to clock		13.5			ns
t _{CS.LAG}	CS lag time, Last clock to CS inactive		1			ns
t _{CS.ACC}	CS access time, CS active to POCI data out				40	ns
t _{CS.DIS}	CS disable time, CS inactive to POCI high impedance				40	ns
t _{SU.PI}	PICO input data setup time		15			ns
t _{HD.PI}	PICO input data hold time		2.5			ns
t _{VALID.PO}	POCI output data valid time(2)	2.7 < VDD < 3.6V			31	ns
t _{VALID.PO}	POCI output data valid time ⁽²⁾	1.62 < VDD < 2.7V			40	ns
t _{HD.PO}	POCI output data hold time ⁽³⁾		5.5			ns

- (1) The POCI input data setup time can be fully compensated when delayed sampling feature is enabled.
- (2) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
- (3) Specifies how long data on the output is valid after the output changing SCLK clock edge

7.17.2 SPI Timing Diagram

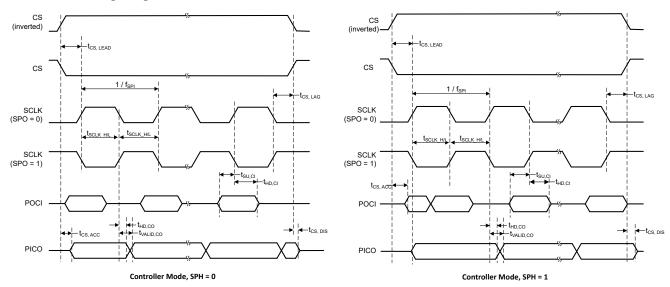


Figure 7-4. SPI Timing Diagram - Controller Mode



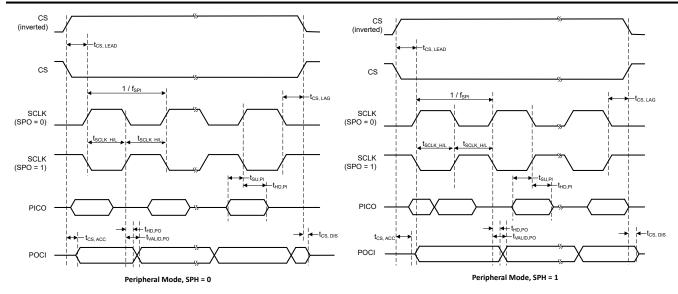


Figure 7-5. SPI Timing Diagram - Peripheral Mode

7.18 UART

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{UART}	UART input clock frequency				32	MHz
f _{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)				4	MHz
		AGFSELx = 0		6		ns
	Pulse duration of spikes	AGFSELx = 1		14	35	ns
t _{SP}	suppressed by input filter	AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

7.19 TIMx

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP MAX	UNIT
		f _{TIMxCLK} = 64MHz	15.625		ns
t _{res}	Timer resolution time	f _{TIMxCLK} = 32MHz	31.25		ns
			1		t _{TIMxCLK}
		f _{TIMxCLK} = 64MHz	0.01563	1024	us
t _{COUNTER}	16-bit counter clock period	f _{TIMxCLK} = 32MHz	0.03125	2048	us
			1	65536	t _{TIMxCLK}

7.20 Emulation and Debug

7.20.1 SWD Timing

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{SWD}	SWD frequency				10	MHz



8 Detailed Description

The following sections describe all of the components that make up the devices in this data sheet. The peripherals integrated into these devices are configured by software through Memory Mapped Registers (MMRs). For more details, see the corresponding chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.



8.1 Overview

MSPM0C1105/6 microcontrollers (MCUs) are part of MSP's highly integrated, ultra-low-power 32-bit MSPM0 MCU family based on the Arm® Cortex®-M0+ 32-bit core platform, operating at up to 32MHz frequency. These costoptimized MCUs offer high-performance analog peripheral integration, support extended temperature ranges from -40°C to 125°C, and operate with supply voltages from 1.62V to 3.6V.

The MSPM0C1105/6 devices provide up to 64KB embedded flash program memory with 8KB SRAM. These MCUs incorporate a high-speed on-chip oscillator with an accuracy from -2.1% to +1.6%, eliminating the need for an external crystal. Additional features include a 3-channel DMA, CRC-16 accelerator, and a variety of high-performance analog peripherals such as one 12-bit 1.6Msps ADC with VDD as the voltage reference, a comparator with 8-bit reference DAC and an on-chip temperature sensor. These devices also offer intelligent digital peripherals such as one 16-bit advanced timer with deadband and timer frequency up to 64MHz, four 16-bit general purpose timer, one windowed watchdog timer, and a variety of communication peripherals including three UART, one SPI, and two I2C. These communication peripherals offer protocol support for LIN, IrDA, DALI, Manchester, smart card, SMBus, and PMBus.

The TI MSPM0 family of low-power MCUs consists of devices with varying degrees of analog and digital integration allowing for customers find the MCU that meets their project's needs. The MSPM0 MCU platform combines the Arm Cortex-M0+ platform with a holistic ultra-low-power system architecture, allowing system designers to increase performance while reducing energy consumption.

For complete module descriptions, see the MSPM0 C-Series Microcontrollers Technical Reference Manual.

8.2 CPU

The CPU subsystem (MCPUSS) implements an Arm Cortex-M0+ CPU, an instruction pre-fetch/cache, a system timer, and interrupt management features. The Arm Cortex-M0+ is a cost-optimized, 32-bit CPU which delivers high performance and low power to embedded applications. Key features of the CPU Sub System include:

- Arm Cortex-M0+ CPU supporting clock frequencies up to 32MHz
 - ARMv6-M Thumb instruction set (little endian) with 32-cycle 32x32 multiply instruction
- · Pre-fetch logic to improve sequential code execution, and I-cache with two 64-bit cache lines
- System timer (SysTick) with 24-bit down counter and automatic reload
- · Nested vectored interrupt controller (NVIC) with 4 programmable priority levels and tail-chaining

8.3 Operating Modes

MSPM0 MCUs provide five main operating modes (power modes) to allow for optimization of the device power consumption based on application requirements. In order of decreasing power, the modes are: RUN, SLEEP, STOP, STANDBY, and SHUTDOWN. The CPU is active executing code in RUN mode. Peripheral interrupt events can wake the device from SLEEP, STOP, or STANDBY mode to the RUN mode. SHUTDOWN mode completely disables the internal core regulator to minimize power consumption, and wake is only possible via NRST, SWD, or a logic level match on certain IOs. RUN, SLEEP, STOP, and STANDBY modes also include several configurable policy options (for example, RUN.x) for balancing performance with power consumption.

To further balance performance and power consumption, MSPM0 devices implement two power domains: **PD1** (for the CPU, memories, and high performance peripherals), and **PD0** (for low speed, low power peripherals).

- PD1 is always powered in RUN and SLEEP modes, but is disabled in all other modes.
- PD0 is always powered in RUN, SLEEP, STOP, and STANDBY modes.
- PD1 and PD0 are both disabled in SHUTDOWN mode.

8.3.1 Functionality by Operating Mode

Supported functionality in each operating mode is given in Supported Functionality by Operating Mode.

Functional key:

• **EN**: The function is enabled in the specified mode.



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- **DIS**: The function is disabled (either clock or power gated) in the specified mode, but the function's configuration is retained.
- **OPT**: The function is optional in the specified mode, and remains enabled if configured to be enabled.
- **NS**: The function is not automatically disabled in the specified mode but is not supported.
- **OFF**: The function is fully powered off in the specified mode, and no configuration information is retained. When waking up from an OFF state, all module registers must be re-configured to the desired settings by application software.

Table 8-1. Supported Functionality by Operating Mode

			RUN			SLEEP	- Сро. и	ST	OP	STAI	NDBY	SHUTD
Operati	ng Mode	RUNO	RUN1	RUN2	SLEEPO	SLEEP1	SLEEP2	STOP0	STOP2	STANDBYO	STANDBY1	OWN
	SYSOSC	EN	EN	DIS	EN	EN	DIS	OPT ⁽¹⁾	DIS	DIS	DIS	OFF
Oscillators	LFOSC or LFXT					Е	N					OFF
	HFXT	EN	DIS	DIS	OPT			D	IS			OFF
	CPUCLK	32M	32k	32k				DIS				OFF
	MCLK to PD1	32M	32k	32k	32M	32k	32k		D	IS		OFF
	ULPCLK to PD0	32M	32k	32k	32M	32k	32k	4M ⁽¹⁾	32	2k	DIS	OFF
	ULPCLK to TIMG14/8	32M	32k	32k	32M	32k	32k	4M ⁽¹⁾		32k		OFF
Oleveler	RTCCLK					32	2k					OFF
Clocks	MFCLK	OPT	D	IS	OPT	D	IS	OPT		DIS		OFF
	LFCLK				-	32k					DIS	OFF
	LFCLK to TIMG14/8					32	2k				1	OFF
	MCLK Monitor					OPT					DIS	OFF
	LFCLK Monitor					Ol	PT					OFF
	POR Monitor						EN					
PMU	BOR Monitor					Е	N					OFF
I WIO	Core Regulator			FULL	DRIVE				REDUCED LOW DRIVE			OFF
	CPU		EN					DIS		I		OFF
	DMA			0	PT			NS	S (triggers	supporte	ed)	OFF
Core Functions	Flash			Е	:N			OPT		D	IS	OFF
	SRAM			Е	:N			OI	PT	D	IS	OFF
5545	SPI0			0	PT				D	IS		OFF
PD1 Peripherals	CRC			0	PT				D	IS		OFF
	TIMG14/8					OI	PT					OFF
	TIMG1/2					OPT					DIS	OFF
	TIMA0					OPT					DIS	OFF
	UART0/1/2					OPT					DIS	OFF
PD0 Peripherals	I2C0/1					OPT					DIS	OFF
	GPIOA/B					OPT					OPT ²	OFF
	WWDT0					OPT					OPT ⁽²⁾	OFF
	IWDT					Ol	PT				1	OFF
	RTC_B					Ol	PT					OFF



Table 8-1. Supported Functionality by Operating Mode (continued)

			RUN			SLEEP		ST	ОР	STAN	IDBY	SHUTD
Opera	ting Mode	RUNO	RUN1	RUN2	SLEEPO	SLEEP1	SLEEP2	STOP0	STOP2	STANDBY0	STANDBY1	OWN
	ADC0				OPT				NS (tri	ggers sup	ported)	OFF
	COMP					Ol	PT T					OFF
Analog	VREF				OPT				NS			OFF
	Temperature Sensor		OPT					OI	FF	OFF		
IOMUX and IO Wakeup		EN							DIS w/ WAKE			
Wake Sources			N/A			ANY IRQ			PD0	IRQ		IOMUX, NRST, SWD

- (1) If STOP0 is entered from RUN1 (SYSOSC enabled but MCLK sourced from LFCLK), SYSOSC remains enabled as it was in RUN1, and ULPCLK remains at 32kHz as it was in RUN1. If STOP0 is entered from RUN2 (SYSOSC was disabled and MCLK was sourced from LFCLK), SYSOSC remains disabled as it was in RUN2, and ULPCLK remains at 32kHz as it was in RUN2.
- (2) When using the STANDBY1 policy for STANDBY, only specific peripherals (TIMG14, TIMG8, IWDT, and RTC) are clocked. Other PD0 peripherals can generate an asynchronous fast clock request upon external activity but are not actively clocked.

8.4 Power Management Unit (PMU)

The power management unit (PMU) generates the internally regulated core supplies for the device and provides supervision of the external supply (VDD). The PMU also contains the bandgap voltage reference used by the PMU itself as well as analog peripherals. Key features of the PMU include:

- Power-on reset (POR) supply monitor
- Brown-out reset (BOR) supply monitor with early warning capability using three programmable thresholds
- Core regulator with support for RUN, SLEEP, STOP, and STANDBY mode to dynamically balance performance with power consumption
- Parity-protected trim to immediately generate a power-on reset (POR) in the event that a power management trim is corrupted
- 4 bytes of shutdown memory

For more details, see the PMU chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.

8.5 Clock Module (CKM)

The clock module provides the following oscillators:

- LFOSC: Internal low-frequency oscillator (32kHz)
- SYSOSC: Internal high-frequency oscillator (32MHz with factory trim)
- LFXT/LFCKIN: low-frequency external crystal oscillator or digital clock input (32kHz)
- HFXT/HFCKIN: high-frequency external crystal oscillator or digital clock input (4MHz to 32MHz)

The following clocks are distributed by the clock module for use by the processor, bus, and peripherals:

- MCLK: Main system clock for PD1 peripherals, derived from SYSOSC, LFCLK, or HSCLK, active in RUN and SLEEP modes
- CPUCLK: Clock for the processor (derived from MCLK), active in RUN mode
- ULPCLK: Ultra-low power clock for PD0 peripherals, active in RUN, SLEEP, STOP, and STANDBY modes
- MFCLK: 4MHz fixed mid-frequency clock for peripherals, available in RUN, SLEEP, and STOP modes
- LFCLK: 32kHz fixed low-frequency clock for peripherals or MCLK, active in RUN, SLEEP, STOP, and STANDBY modes
- ADCCLK: ADC clock, available in RUN, SLEEP and STOP modes

- RTCCLK: Fixed 32kHz clock direct to RTC
- CLK_OUT: Used to output a clock externally, available in RUN, SLEEP, STOP, and STANDBY modes
- HFCLK: High frequency clock derived from HFXT or HFCLK_IN, available in RUN and SLEEP mode
- HSCLK: High speed clock derived from HFCLK, available in RUN and SLEEP mode

For more details, see the CKM chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.

8.6 DMA B

The direct memory access (DMA) controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA can be used to move data from ADC conversion memory to SRAM. The DMA reduces system power consumption by allowing the CPU to remain in low power mode, without having to awaken to move data to or from a peripheral.

The DMA_B in these devices support the following key features:

- · 3 DMA transfer channel
 - 2 full-feature channels, supporting repeated transfer modes
 - 1 basic channel, supporting single transfer mode
- Configurable DMA channel priorities
- Direct peripheral to DMA trigger is supported from ADC, UART, SPI or timer triggers.
- Byte (8-bit), short word (16-bit) and word (32-bit) or mixed byte and word transfer capability
- Transfer counter block size supports up to 64k transfers of any data type
- Configurable DMA transfer trigger selection
- Active channel interruption to service other channels
- · Early interrupt generation for ping-pong buffer architecture
- · Cascading channels upon completion of activity on another channel
- · Stride mode to support data re-organization, such as 3-phase metering applications
- · Gather mode

Table 8-2 shows the DMA features that are supported and the corresponding DMA channel numbers.

Table 8-2. DMA B Channel Features

Table 0-2. DIMA_B Chainlei i eatales								
DMA Feature	DM	A_B						
DINA Feature	Full-Feature Channel	Basic Channel						
Channel Number	0, 1	2						
Repeated mode	✓	-						
Table & fill mode	✓	_						
Gather mode	✓	_						
Early IRQ notification	✓	-						
Auto enable	✓	✓						
Long long (128-bit) transfer	✓	✓						
Stride mode	✓	✓						
Cascading channel support	✓	✓						

Table 8-3 lists the available triggers for the DMA which are configured using the DMATCTL.DMATSEL control bits in the DMA memory mapped registers.

Table 8-3. DMA Trigger Mapping

DMACTL.DMATSEL	TRIGGER SOURCE
0	Software
1	Generic Subscriber 0 (FSUB_0)
2	Generic Subscriber 0 (FSUB_1)
3	I2C0 PUBLISHER 1
4	I2C0 PUBLISHER 2
5	I2C1 PUBLISHER 1



Table 8-3. DMA Trigger Mapping (continued)

DMACTL.DMATSEL	TRIGGER SOURCE
6	I2C1 PUBLISHER 2
7	SPI0 PUBLISHER 1
8	SPI0 PUBLISHER 2
9	UARTO PUBLISHER 1
10	UARTO PUBLISHER 2
11	UART1 PUBLISHER 1
12	UART1 PUBLISHER 2
13	UART2 PUBLISHER 1
14	UART2 PUBLISHER 2
15	ADC0 DMA Trigger

8.7 Events

The event manager transfers digital events from one entity (for example, a peripheral) to another (for example, a second peripheral, the DMA, or the CPU). The event manager implements event transfer through a defined set of event publishers (generators) and subscribers (receivers) which are interconnected through an event fabric containing a combination of static and programmable routes.

Events which are transferred by the event manager include:

- Peripheral event transferred to the CPU as an interrupt request (IRQ) (Static Event)
 - Example: RTC interrupt is sent to the CPU
- Peripheral event transferred to the DMA as a DMA trigger (DMA Event)
 - Example: UART data receive trigger to DMA to request a DMA transfer
- Peripheral event transferred to another peripheral to directly trigger an action in hardware (Generic Event)
 - Example: TIMx timer peripheral publishes a periodic event to the ADC subscriber port, and the ADC uses the event to trigger start-of-sampling

For more details, see the EVENT chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.

Table 8-4. Generic Event Channels

A generic route is either a point-to-point (1:1) route or a point-to-two (1:2) splitter route in which the peripheral publishing the event is configured to use one of several available generic route channels to publish its event to another entity (or entities, in the case of a splitter route), where an entity may be another peripheral, a generic DMA trigger event, or a generic CPU event.

CHANID	Generic Route Channel Selection	Channel Type
0	No generic event channel selected	N/A
1	Generic event channel 1 selected	1 : 1
2	Generic event channel 2 selected	1 : 1
3	Generic event channel 3 selected	1 : 1
4	Generic event channel 4 selected	1 : 1
6	Generic event channel 5 selected	1:1
7	Generic event channel 5 selected	1 : 2 (splitter)
8	Generic event channel 6 selected	1 : 2 (splitter)

8.8 Memory

8.8.1 Memory Organization

Table 8-5 summarizes the memory map of the devices. For more information about the memory region detail, see the *Platform Memory Map* section in the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

Table 8-5. Memory Organization

Table 0-3. Memory Organization						
Memory Region	Subregion	MSPM0C1105	MSPM0C1106			
Code (Flash)	Flash	32KB ⁽¹⁾ 0x0000.0000 to 0x0000.7FFF	64KB ⁽¹⁾ 0x0000.0000 to 0x0000.FFFF			
SRAM (SRAM)	SRAM	8KB 0x2000.0000 to 0x2000.1FFF	8KB 0x2000.0000 to 0x2000.1FFF			
	Peripherals	0x4000.0000 to 0x40FF.FFFF	0x4000.0000 to 0x40FF.FFFF			
	Flash	0x0040.0000 to 0x0040.7FFF	0x0040.0000 to 0x0040.9FFF			
Peripheral	Configuration NVM	512 bytes 0x41C0.0000 to 0x41C0.0200	512 bytes 0x41C0.0000 to 0x41C0.0200			
	FACTORY	0x41C4.0000 to 0x41C4.0080	0x41C4.0000 to 0x41C4.0080			
Subsystem		0x6000.0000 to 0x7FFF.FFFF	0x6000.0000 to 0x7FFF.FFF			
System PPB		0xE000.0000 to 0xE00F.FFFF	0xE000.0000 to 0xE00F.FFFF			

⁽¹⁾ First 32KB flash memory (address 0x0000.0000 to 0x0000.8000) has up to 100000 program/erase cycles.

8.8.2 Peripheral File Map

Table 8-6 lists the available peripherals and the register base address for each.

Table 8-6. Peripherals Summary

		SIZE			
PERIPHERAL NAME	BASE ADDRESS				
COMP0	0x40008000	0x00001F0			
VREF	0x40030000	0x00001F0			
WWDT0	0x40080000	0x0000150			
TIMG14	0x40084000	0x00001F0			
TIMG1	0x40086000	0x00001F0			
TIMG2	0x40088000	0x00001F0			
TIMG8	0x40090000	0x00001F0			
LFSS	0x40094000	0x0000160			
RTC_B	0x40094000	0x0000160			
IWDT	0x40094000	0x0000160			
GPIOA	0x400A0000	0x00001F0			
GPIOB	0x400A2000	0x00001F0			
SYSCTL	0x400AF000	0x0000310			
DEBUGSS	0x400C7000	0x00001F0			
EVENTLP	0x400C9000	0x0000300			
FLASHCTL	0x4042A000	0x00001F0			
I2C0	0x40440000	0x0000200			
I2C1	0x400CD000	0x0000200			
UART1	0x400F0000	0x00001F0			
UART2	0x400F2000	0x00001F0			
UART0	0x40100000	0x00001F0			
CPUSS	0x40102000	0x00001F0			
WUC	0x40108000	0x00001F0			
IOMUX	0x40400000	0x00001F0			
DMA	0x40424000	0x0000050			
CRC	0x40428000	0x0000200			
SPI0	0x40468000	0x00001F0			
ADC0_SVT	0x4055A000	0x0000100			



Table 8-6. Peripherals Summary (continued)

PERIPHERAL NAME	BASE ADDRESS	SIZE		
TIMA0	0x40860000	0x00001F0		



8.8.3 Peripheral Interrupt Vector

Table 8-7shows the IRQ number and the interrupt group number for each peripheral in this device.

Table 8-7. Interrupt Vector Number

PERIPHERAL NAME	NVIC IRQ
SYSCTL	0
DEBUGSS	1
TIMG8	2
UART1	3
ADC0	4
COMP0	7
UART2	8
SPI0	9
UART0	15
TIMG14	16
TIMG2	17
TIMA0	18
TIMG1	19
GPIOA	22
GPIOB	23
I2C0	24
I2C1	25
FLASHCTL	27
WWDT0	29
LFSS	30
RTC_B	30
IWDT	30
DMA	31

8.9 Flash Memory

A single bank of nonvolatile flash memory is provided for storing executable program code and application data. Key features of the flash include:

- · In-circuit program and erase operations supported across the entire recommended supply range
- Small 1KB sector sizes (minimum erase resolution of 1KB)
- Up to 100,000 program/erase cycles on 32 selected sectors of the flash memory, with up to 10,000 program/erase cycles on the remaining flash memory (devices with 32kB support 100,000 cycles on the entire flash memory)

For more details, see the NVM chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.

8.10 **SRAM**

MSPM0Cxx MCUs include a low-power high-performance SRAM memory with zero wait state access across the supported CPU frequency range of the device. SRAM memory can be used for storing volatile information such as the call stack, heap, global data, and code. The SRAM memory content is fully retained in RUN, SLEEP, STOP, and STANDBY operating modes and is lost in SHUTDOWN mode. A write protection mechanism is provided to allow the application to dynamically write protect the SRAM memory with 1KB resolution. Write protection is useful when placing executable code into SRAM to provide a level of protection against unintentional overwrites of code by either the CPU or DMA. Placing code in SRAM can improve performance of critical loops by enabling zero wait state operation and lower power consumption.

8.11 **GPIO**

The general purpose input/output (GPIO) peripheral lets the application write data out and read data in through the device pins. Through the use of the Port A and Port B GPIO peripheral, these devices support up to 45 GPIO pins.

The key features of the GPIO module include:

- · Set/Clear/Toggle multiple bits without the need of a read-modify-write construct in software
- GPIOs with "Standard with Wake" drive functionality able to wake the device from SHUTDOWN mode
- "FastWake" feature enables low-power wakeup from STOP and STANDBY modes for any GPIO port
- User controlled input filtering

For more details, see the GPIO chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.

8.12 IOMUX

The IOMUX peripheral enables IO pad configuration and controls digital data flow to and from the device pins. The key features of the IOMUX include:

- · IO Pad configuration registers allow for programmable drive strength, speed, pullup-down, and more
- · Digital pin muxing allows for multiple peripheral signals to be routed to the same IO pad
- · Pin functions and capabilities are user-configured using the PINCM register

For more details, see the IOMUX chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.

8.13 ADC

The 12-bit analog-to-digital converter (ADC) module in these devices support fast 12-bit conversions with single-ended inputs.

ADC features include:

- 12-bit output resolution at up to 1.6-Msps with 10.6-bit ENOB (external reference)
- Up to 27 external input channels
- Internal channels for temperature sensing, supply monitoring, and analog signal chain
- · Software selectable reference:
 - Configurable internal dedicated ADC reference voltage of 1.4V or 2.5V (VREF)
 - MCU supply voltage (VDD)
 - Support for bringing in an external reference on VREF+/- device pins
 - Requires a decpoupling capacitor placed on VREF+/- pins for proper operation.
- Operates in RUN, SLEEP, and STOP modes and supports triggers from STANDBY mode

Table 8-8. ADC0 Channel Mapping

CHANNEL[0:7]	SIGNAL NAME	CHANNEL[8:15]	SIGNAL NAME	
0	A0	16	A16	
1	A1	17	A17	
2	A2	18	A18	
3	A3	19	A19	
4	A4	20	A20	
5	A5	21	A21	
6	A6	22	A22	
7	A7	23	A23	
8	A8	24	A24	
9	A9	25	A25	
10	10 A10		A26	

Supply/Battery Monitor

iable of the orange inappling (continuou)								
CHANNEL[0:7]	SIGNAL NAME	CHANNEL[8:15]	SIGNAL NAME					
11	A11	27	Reserved					
12	A12	28	Temperature Sensor					
13	A13	A13 29 VREF						
14	A14 30		Reserved					
	i e e e e e e e e e e e e e e e e e e e							

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Table 8-8. ADC0 Channel Mapping (continued)

Italicized signal names are internal to the SoC. These signals are used for internal peripheral interconnections.

For more details, see the ADC chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.

A15

8.14 Temperature Sensor

15

The temperature sensor provides a voltage output that changes linearly with device temperature. The temperature sensor output is internally connected to one of ADC input channels to enable a temperature-to-digital conversion.

A unit-specific single-point calibration value for the temperature sensor is provided in the factory constants memory region. This calibration value represents the ADC conversion result (in ADC code format) corresponding to the temperature sensor being measured in 12-bit mode with the 1.4V internal VREF at the factory trim temperature (TS_{TRIM}). This calibration value can be used with the temperature sensor temperature coefficient (TS_c) to estimate the device temperature. See the temperature sensor section of the *MSPMO C-Series Microcontrollers Technical Reference Manual* for guidance on estimating the device temperature with the factory trim value.

8.15 Low-Frequency Sub System (LFSS)

The Low-Frequency Sub-System (LFSS) is a sub-system which combines several functional peripherals under one shared subsystem. These peripherals are clocked by the low frequency clock (LFCLK) or need to be active during low power modes. The LFCLK has a typical frequency of 32kHz and is mainly intended for long-term timekeeping.

LFSS in this device contains following components:

- · Real Time Clock with additional prescalar extension and timestamp captures
- An asynchronous IWDT

For more details, see the LFSS chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.

8.16 VREF

The shared voltage reference module (VREF) in these devices contain a configurable voltage reference buffer which allows users to supply a stable reference to on-board analog peripherals. It also supports bringing in an external reference for applications where higher accuracy is required.

VREF features include:

- 1.4V and 2.5V user-selectable internal references. Same reference voltage will be selected for ADC and COMP
- Internal reference supports ADC operation up to 515ksps
- Support for bringing in an external reference on VREF+ and VREF- device pins

For more details, see the VREF chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.

8.17 COMP

The comparator peripheral in the device compares the voltage levels on two inputs terminals and provides a digital output based on this comparison. It supports the following key features:

Programmable hysteresis



- · Programmable reference voltage:
 - External reference voltage (VREF IO)
 - Integrated 8-bit reference DAC
- · Configurable operation modes:
 - High speed mode
 - Lower power mode
- Programmable output glitch filter delay
- Supports 6 blanking sources from TIMx instances (see Table 8-10)
- · Support output wake up device from all low power modes
- Output connected to advanced timer fault handling mechanism
- The IPSEL and IMSEL bits in comparator registers can be used to select the comparator channel inputs from device pins
- · 8-bit reference DAC can be used to output to device pins

Table 8-9. COMP0 Input Channel Selection

IPSEL / IMSEL BITS	POSITIVE TERMINAL INPUT	NEGATIVE TERMINAL INPUT
0x0	COMP0_IN0+	COMP0_IN0-
0x1	COMP0_IN1+	COMP0_IN1-
0x2	COMP0_IN2+	COMP0_IN2-
0x3	COMP0_IN3+	-
0x5	-	Temperature Sensor

Table 8-10. COMP0 Blanking Source Table

CTL2.BLANKSRC	Blanking Source Selected
1	TIMA0.CC2
2	TIMA0.CC3
3	TIMA0.CC1
4	TIMG0.CC1
5	TIMG1.CC1
6	TIMG8.CC1

For more information about device analog connections, refer to Section 8.27.

For more details, see the COMP chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.

8.18 Security

This device offers several security features, including:

- Debug security
- Unique Die ID
- Flexible firewalls for protecting code and data
 - Flash write-erase protection
 - Flash read-execute protection
 - Flash IP protection
 - SRAM write-execute mutual exclusion
- Secure boot
- · Secure firmware update
- · Customer secure code
- Cyclic redundancy checker (CRC-16) with support for custom polynomial

For more details, see the Security chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual

Submit Document Feedback

8.19 CRC

The cyclical redundancy check (CRC) module provides a signature for an input data sequence. Key features of the CRC module include:

- Support for 16-bit CRC based on CRC16-CCITT
- Support for bit reversal

For more details, see the CRC chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.

8.20 **UART**

The UART peripherals (UART0, UART1, UART2) provide the following key features:

- Standard asynchronous communication bits for start, stop, and parity
- Fully programmable serial interface
 - 5, 6, 7 or 8 data bits
 - Even, odd, stick, or no-parity bit generation and detection
 - 1 or 2 stop bit generation
 - Line-break detection
 - Glitch filter on the input signals
 - Programmable baud rate generation with oversampling by 16, 8 or 3
 - Local Interconnect Network (LIN) mode support
- Separated transmit and receive FIFOs support DAM data transfer
- Support transmit and receive loopback mode operation
- See Table 8-11 for detail information on supported protocols.

Table 8-11. UART Features

Table 6 TH 6/1/11 Gatares						
UART Features	UART0(Extend)	UART1, UART2(Main)				
Active in Stop and Standby Mode	Yes	Yes				
Separate transmit and receive FIFOs	Yes	Yes				
Support hardware flow control	Yes	Yes				
Support 9-bit configuration	Yes	Yes				
Support LIN mode	Yes	-				
Support DALI	Yes	-				
Support IrDA	Yes	-				
Support ISO7816 Smart Card	Yes	-				
Support Manchester coding	Yes	-				

For more details, see the UART chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.

8.21 I2C

The inter-integrated circuit interface (I²C) peripherals in these devices provide bidirectional data transfer with other I2C devices on the bus and support the following key features:

- 7-bit and 10-bit addressing mode with multiple 7-bit target addresses
- Multiple-controller transmitter or receiver mode
- Target receiver or transmitter mode with configurable clock stretching
- Support Standard-mode (Sm), with a bit rate up to 100kbps
- Support Fast-mode (Fm), with a bit rate up to 400kbps
- Support Fast-mode Plus (Fm+), with a bit rate up to 1Mbps
- Separated transmit and receive FIFOs support DMA data transfer
- Support SMBus 3.0 with PEC, ARP, timeout detection and host support
- · Wakeup from low power mode on address match
- Support analog and digital glitch filter for input signal glitch suppression

For more details, see the I2C chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.



8.22 SPI

The serial peripheral interface (SPI) peripherals in these devices support the following key features:

- Support ULPCLK/2 bit rate and up to 16Mbits/s in both controller and peripheral mode
- Configurable as a controller or a peripheral
- Configurable chip select for both controller and peripheral
- Programmable clock prescaler and bit rate
- Programmable data frame size from 4 bits to 16 bits (controller mode)
- Programmable data frame size from 7 bits to 16 bits (peripheral mode)
- Separated transmit and receive FIFOs support DMA data transfer
- Supports TI mode, Motorola mode, and National Microwire format

For more details, see the SPI chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.

8.23 IWDT

The independent watchdog timer (IWDT) in the LFSS is a device-independent supervisor which monitors code execution and overall hang up scenarios of the device. Due to the nature of LFSS, this IWDT has its own system independent power and clock source. If the application software does not successfully reset the watchdog within the programmed time, the watchdog generates a POR reset to the device.

Key features of the IWDT include:

- A 25-bit counter with closed and open window
- Counter driven from LFOSC (fixed 32kHz clock path) with a programmable clock divider
- Eight selectable watchdog timer periods

For more details, see the IWDT chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.

8.24 WWDT

The windowed watchdog timer (WWDT) can be used to supervise the operation of the device, specifically code execution. The WWDT can be used to generate a reset or an interrupt if the application software does not successfully reset the watchdog within a specified window of time. Key features of the WWDT include:

- 25-bit counter
- Programmable clock divider
- Eight software selectable watchdog timer periods
- Eight software selectable window sizes
- Support for stopping the WWDT automatically when entering a sleep mode
- Interval timer mode for applications which do not require watchdog functionality

For more details, see the WWDT chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.

8.25 RTC B

The RTC B instance of the real-time clock operates off of a 32kHz input clock source (typically a low frequency crystal) and provides a time base to the application with multiple options for interrupts to the CPU. The RTC_B provides common key features in relation to the Low-Frequency Sub System (LFSS).

Common key features of the RTC B include:

- Counters for seconds, minutes, hours, day of the week, day of the month, month, and year
- Binary or BCD format
- Leap-year handling
- · One customizable alarm interrupt based on minute, hour, day of the week, and day of the month
- Interval alarm interrupt to wake every minute, every hour, at midnight, or at noon
- Interval alarm interrupt providing periodic wake-up at 4096, 2048, 1024, 512, 256, or 128 Hz
- Interval alarm interrupt providing periodic wake-up at 64, 32, 16, 8, 4, 2, 1, and 0.5 Hz
- Calibration for crystal offset error (up to +/- 240ppm)

- Compensation for temperature drift (up to +/- 240ppm)
- RTC clock output to pin for calibration

Table 8-12 shows the RTC features supported in this device.

Table 8-12. RTC_B Key Features

RTC Features	RTC_B				
Power enable register	-				
Real-time clock and calendar mode providing seconds, minutes, hours, day of week, day of month, and year	Yes				
Selectable binary or binary-coded decimal (BCD) format	Yes				
Leap-year correction (valid for year 1901 through 2099)	Yes				
Two customizable calendar alarm interrupts based on minute, hour, day of the week, and day of the month	Yes				
Interval alarm interrupt to wake every minute, every hour, at midnight, or at noon	Yes				
Periodic interrupt to wake at 4096, 2048, 1024, 512, 256, or 128Hz	Yes				
Periodic interrupt to wake at 64, 32, 16, 8, 4, 2, 1, and 0.5Hz	Yes				
Interrupt capability down to STANDBY mode with STOPCLKSTBY	Yes				
Calibration for crystal offset error and crystal temperature drift (up to ±240 ppm total)	Yes				
RTC clock output to pin for calibration (GPIO)	Yes				
RTC clock output to pin for calibration (TIO)	-				
Three -bit prescaler for heartbeat function with interrupt generation	-				
RTC external clock selection of untrimmed 32kHz, trimmed 512Hz, 256Hz or 1Hz	-				
RTC time stamp capture upon detection of a timer stamp event, including: TIO event VDD fail event	-				
RTC counter lock function	-				

For more details, see the RTC chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.

8.26 Timers (TIMx)

The timer peripherals in these devices support the following key features. For specific configuration, see Table 8-13.

Specific features for the **general-purpose timer (TIMGx)** include:

- 16-bit down, up/down, or up counter with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- · Up to four independent CC channels for
 - Output compare
 - Input capture
 - PWM output
 - One-shot mode
- Support quadrature encoder interface (QEI) for positioning and movement sensing

- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt trigger generation and cross peripherals (such as ADC) trigger capability
- Cross-trigger event logic for Hall sensor inputs

Specific features for the advanced timer (TIMAx) include:

- 16-bit down or up-down counter, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Clock doubler to provide 2x clock source for improved timer resolution
- Repeat counter to generate an interrupt or event only after a given number of cycles of the counter
- · Up to four independent CC channels for
 - Output compare
 - Input capture
 - PWM output
 - One-shot mode
- Shadow register for load and CC register available
- · Complementary output PWM
- Asymmetric PWM with programmable dead band insertion
- Fault handling mechanism to keep the output signals in a safe user-defined state when a fault condition is encountered
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt trigger generation and cross peripherals (such as ADC) trigger capability
- · Two additional capture/compare channels for internal events

Table 8-13. TIMx Configurations

TIMER NAME	POWER DOMAIN	RESOLUTION	PRESCALER	REPEAT COUNTER	CAPTURE / COMPARE CHANNELS	PHASE	SHADOW	SHADOW	DEAD- BAND	FAULT	QEI
TIMG14	PD0	16 bit	8 bit	-	4	-	-	-	-	-	-
TIMG1	PD0	16 bit	8 bit	_	2	-	-	_	_	_	-
TIMG2	PD0	16 bit	8 bit	-	2	-	-	-	-	-	-
TIMG8	PD0	16 bit	8 bit	_	2	-	_	_	_	_	Yes
TIMA0	PD0	16 bit	8 bit	8-bit	4	Yes	Yes	Yes	Yes	Yes	-

For more details, see the TIMx chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.



8.27 Device Analog Connections

Figure 8-1 shows the internal analog connection of the device.

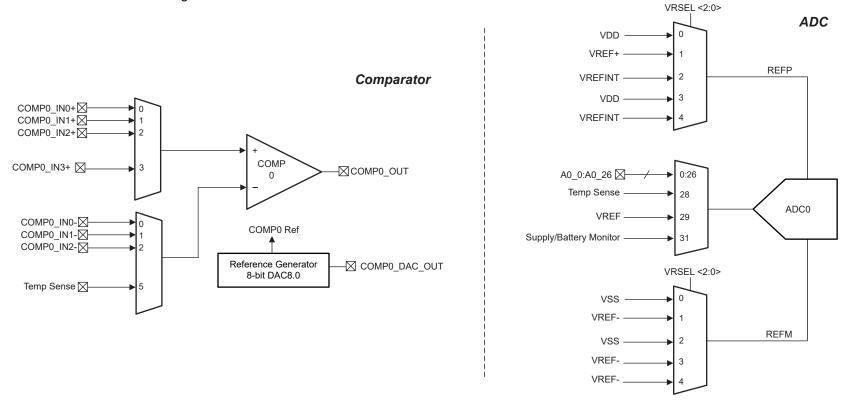


Figure 8-1. Device Analog Connection



8.28 Input/Output Diagrams

The IOMUX manages the selection of which peripheral function is to be used on a digital IO. It also provides the controls for the output driver, input path, and the wake-up logic for wakeup from SHUTDOWN mode. For more information, refer to the IOMUX section of the MSPMO C-Series Microcontrollers Technical Reference Manual.

The mixed-signal IO pin slice diagram for a full featured IO pin is shown in Figure 8-2. Not all pins will have analog functions, wake-up logic, drive strength control, and pullup or pulldown resistors available.

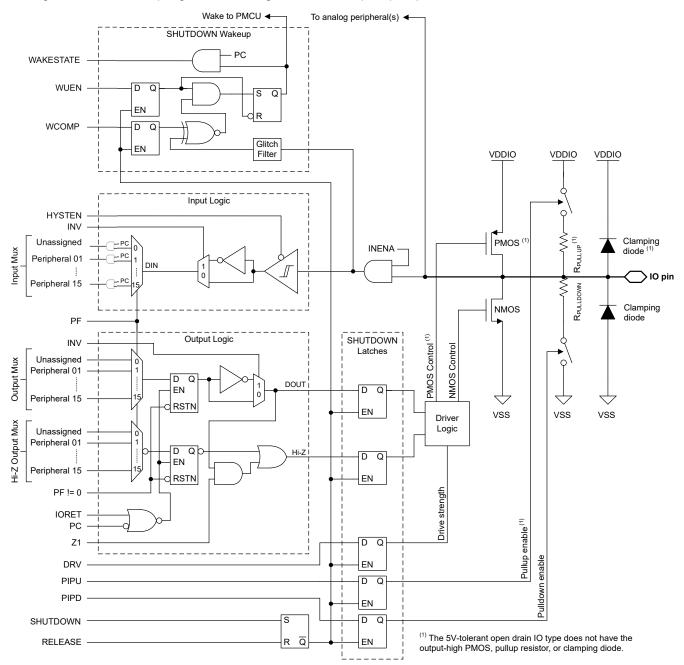


Figure 8-2. Superset Input/Output Diagram

8.29 Serial Wire Debug Interface

A serial wire debug (SWD) two-wire interface is provided via an Arm compatible serial wire debug port (SW-DP) to enable access to multiple debug functions within the device.

Table 8-14. Serial Wire Debug Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SWD FUNCTION
SWCLK	Input	Serial wire clock from debug probe
SWDIO	Input/Output	Bi-directional (shared) serial wire data

For a complete description of the debug functionality offered on MSPM0 devices, see the Debug chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.

8.30 DEBUGSS

The debug subsystem (DEBUGSS) interfaces the ARM Serial Wire Debug (SWD) two-wire physical interface to multiple debug functions within the device. MSPM0 devices support debugging of processor execution and the device state. The DEBUGSS also provides a mailbox system for communicating with software through SWD.

Key features provided by the debug subsystem include:

- The ARM Serial Wire Debug (SWD) two-wire (SWDIO, SWCLK) debug interface, compatible with both TI and 3rd party debug probes
 - On-chip pullup and pulldown resistors for SWDIO and SWCLK, respectively, enabled by default
 - Support for disabling SWD functions to use SWD pins as general-purpose input/output pins
 - Support for debug on all low power modes
- Debug of the processor
 - Run, halt, and step debug support
 - 2 hardware breakpoints (BPU)
 - 1 hardware watchpoints (DWT)
 - Supporting software breakpoints
- Software-configurable peripheral behavior during processor debug
 - Ability to free run select peripherals through debug halt
 - Ability to halt select peripherals on a debug halt
 - Ability to request reset and mode changes to the PMCU
- Mailbox (DSSM) for passing data and control signals between the SWD interface and boot ROM (as well as application software)
- Support for various security features, including SWD lockout and password authenticated debugging

For more details, see the DEBUGSS chapter of the MSPM0 C-Series Microcontrollers Technical Reference Manual.

8.31 Device Factory Constants

All devices include a memory-mapped FACTORY region which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Please refer to Factory Constants chapter of the MSPMO C-Series Microcontrollers Technical Reference Manual for more information.

Table 8-15. DEVICEID

DEVICEID address is 0x41C4.0004, PARTNUM is bit 12 to 27, MANUFACTURER is bit 1 to 11.

Device	PARTNUM	MANUFACTURER		
MSPM0C1105	0xBBBA	0x17		
MSPM0C1106	0xBBBA	0x17		

Table 8-16, USERID

USERID address is 0x41C4.0008. PART is bit 0 to 15. VARIANT is bit 16 to 23

<u> </u>									
Device	Part	Variant							
MSPM0C1105SPTR	CC25	31							
MSP32C031C6SPTR	CC25	53							
MSP32G031C6SPTR	CC25	54							
MSPM0C1105SDGS28R	CC25	33							



Table 8-16. USERID (continued)

USERID address is 0x41C4.0008, PART is bit 0 to 15, VARIANT is bit 16 to 23

Device	Part	Variant
MSPM0C1105SDGS20R	CC25	34
MSPM0C1105SRGZR	CC25	35
MSPM0C1105SRHBR	CC25	36
MSPM0C1105SRGER	CC25	37
MSPM0C1105SRUKR	CC25	38
MSP32G031C6SVFCR	CC25	39
MSP32C031C6SVFCR	CC25	55
MSPM0C1105SZCMR	CC25	60
MSPM0C1106SPTR	F5CF	3A
MSP32G031C8SPTR	F5CF	56
MSPM0C1106SDGS28R	F5CF	3C
MSPM0C1106SDGS20R	F5CF	3D
MSPM0C1106SRGZR	F5CF	3E
MSPM0C11106SRHBR	F5CF	3F
MSPM0C1106SRGER	F5CF	40
MSPM0C1106SRUKR	F5CF	41
MSP32G031C8SVFCR	F5CF	42
MSPM0C1106SZCMR	F5CF	61

8.32 Identification

Revision and Device Identification

The hardware revision and device identification values are stored in the memory-mapped FACTORY region, refer to Device Factory Constants section, which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Refer to the Factory Constants chapter of the MSPMO C-Series Microcontrollers Technical Reference Manual for more information.

The device revision and identification information are also included as part of the top-side marking on the device package. The device-specific errata sheet describes these markings (see Section 10.4).



9 Applications, Implementation, and Layout

9.1 Typical Application

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1.1 Schematic

TI recommends connecting a combination of a $10\mu\text{F}$ and a $0.1\mu\text{F}$ low-ESR ceramic decoupling capacitor to the VDD and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters).

The NRST reset pin is required to connect an external $47k\Omega$ pullup resistor with a 1000pF pulldown capacitor.

For devices supporting external crystals, external bypass capacitors for the crystal oscillator pins are required. Refer to *MSPM0 C-Series Microcontrollers Technical Reference Manual* which explains how to calculate the capacitor value.

For 5V-tolerant open drain IOs (ODIO), a pullup resistor is required to output a logic high signal. This is required for I²C and UART functions if the ODIO are used.

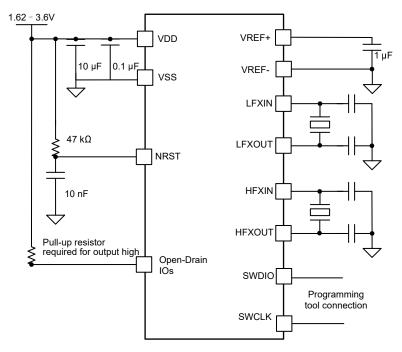


Figure 9-1. Typical Application Schematic



10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Getting Started and Next Steps

For more information on the MSP low-power microcontrollers and the tools and libraries that are available to help with development, visit the Texas Instruments *Arm Cortex-M0+ MCUs* page.

10.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices and support tools. Each MSP MCU commercial family member has one of two prefixes: MSP or X. These prefixes represent evolutionary stages of product development from engineering prototypes (X) through fully qualified production devices (MSP).

X – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP - Fully qualified production device

X devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes." MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. Tl's standard warranty applies. Predictions show that prototype devices (X) have a greater failure rate than the standard production devices. Tl recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 10-1 provides a legend for reading the complete device name.

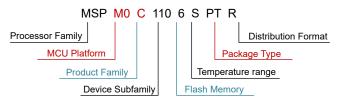


Figure 10-1. Device Nomenclature

Table 10-1. Device Nomenclature

Processor Family	MSP = Mixed-signal processor X= Experimental silicon				
MCU Platform	M0 = Arm based 32-bit M0+				
Product Family	C = 32MHz frequency				
Device Subfamily	1105/6 = 32MHz frequency, ADC, RTC, CMP				
Flash Memory	5 = 32KB 6= 64KB				
Temperature Range	S = -40°C to 125°C				
Package Type See the Device Comparison section and https://www.ti.com/packaging					
Distribution Format	R = Large reel No marking = Tube or tray				

For orderable part numbers of MSP devices in different package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.



10.3 Tools and Software

Design Kits and Evaluation Modules

MSPM0 LaunchPad (LP) Boards: LP-MSPM0C1106 Empowers you to immediately start developing on the industry's best integrated analog and most cost-optimized general purpose MSPM0 MCU family. Exposes all device pins and functionality; includes some built-in circuitry, out-of-box software demos, and on-board XDS110 debug probe for programming/debugging/EnergyTrace.

The LP ecosystem includes dozens of BoosterPack stackable plug-in modules to extend functionality.

Embedded Software

MSPM0 Software Development Kit (SDK)

Contains software drivers, middleware libraries, documentation, tools, and code examples that create a familiar and easy user experience for all MSPM0 devices.

Software Development Tools

TI Cloud Tools Start your evaluation and development on a web browser without any

installation. Cloud tools also have a downloadable, offline version.

TI Resource Explorer Online portal to TI SDKs. Accessible in CCS IDE or in TI Cloud Tools.

SysConfig Intuitive GUI to configure device and peripherals, resolve system conflicts,

generate configuration code, and automate pin mux settings. Accessible in

CCS IDE or in TI Cloud Tools. (offline version)

MSP Academy Great starting point for all developers to learn about the MSPM0 MCU Platform

with training modules that span a wide range of topics. Part of TIRex.

GUI Composer GUIs that simplify evaluation of certain MSPM0 features, such as configuring

and monitoring a fully integrated analog signal chain without any code needed.

IDE & compiler toolchains

Code Composer Studio™

(CCS)

Includes TI Arm-Clang compiler. Supports all TI Arm Cortex MCUs and boasts competitive code size performance advantages, fast compile time, code coverage support, safety certification support, and completely free to use.

IAR Embedded Workbench® IDE

Keil® MDK IDE

GNU Arm Embedded Toolchain

10.4 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the MSPM0 MCUs. Copies of these documents are available on the Internet at www.ti.com.

Technical Reference Manual

MSPM0 C-Series Microcontrollers Technical Reference Manual This manual describes the modules and peripherals of the family of devices. Each description presents the module or peripheral in a general sense. Not all features and functions of all modules or peripherals are present on all devices. In addition, modules or peripherals can differ in their exact implementation on different devices.



Pin functions, internal signal connections, and operational parameters differ from device to device. See the device-specific data sheet for these details.

10.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.6 Trademarks

LaunchPad[™], Code Composer Studio[™], and TI E2E[™] are trademarks of Texas Instruments. Arm[®] and Cortex[®] are registered trademarks of Arm Limited.

All trademarks are the property of their respective owners.

10.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.8 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Cha	anges from July 30, 2025 to September 30, 2025 (from Revision * (July 2025) to Revision A	
(Se	eptember 2025))	Page
• 1	Updated the power modes and package option section	1
•	Removed the DGS32 package information and updated the table footnotes	<mark>2</mark>
• (Updated the device comparison table footnotes and removed the DGS32 package	6
•	Removed the DGS32 pin diagram, pin attributes, and signal descriptions	<mark>7</mark>
	Updates to specifications encompassing Thermal Characteristics, Supply Current Characteristics, Pesupply Sequencing, Timing Characteristics, Clock Specifications, Analog MUX VBOOST, ADC, Tem	
	Sensor, VREF, SPI, and TIMx	•
• (Updated CPU features	58
	Edited the ADC ENOB with external reference	
•	Added the DEGUGSS section	75
• (Updated the DEVICEID and USERID tables	<mark>75</mark>



12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

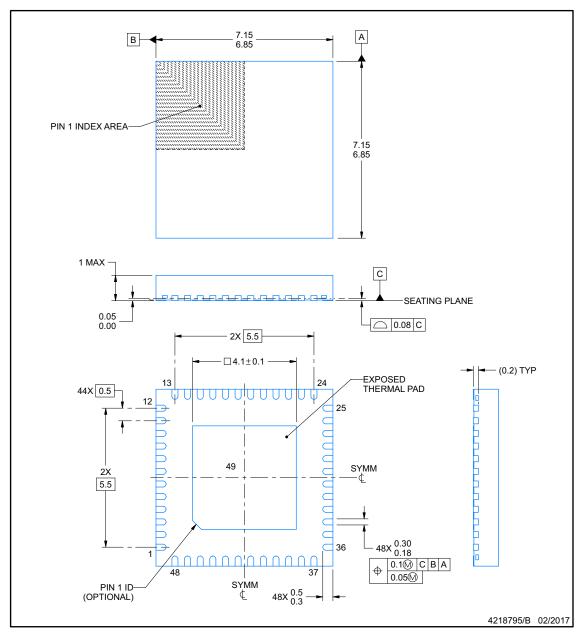




PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.
 The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



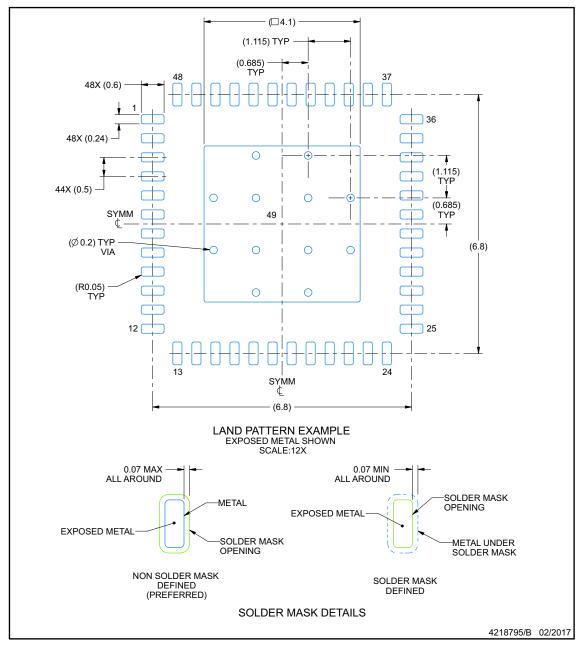


EXAMPLE BOARD LAYOUT

RGZ0048B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.





EXAMPLE STENCIL DESIGN

RGZ0048B

VQFN - 1 mm max height
PLASTIC QUAD FLATPACK - NO LEAD

48X (0.6)

48X (0.6)

48X (0.24)

48X (0.24)

48X (0.5)

5YMM

(R0.05) TYP

(R0.05) TYP

(R0.05) TYP

(Co.8)

12

12

13

SYMM

(6.8)

SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49 73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE SCALE:12X

4218795/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





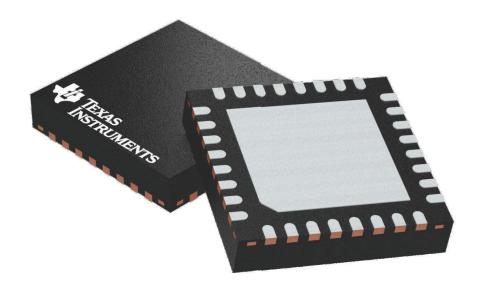
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4224745/A



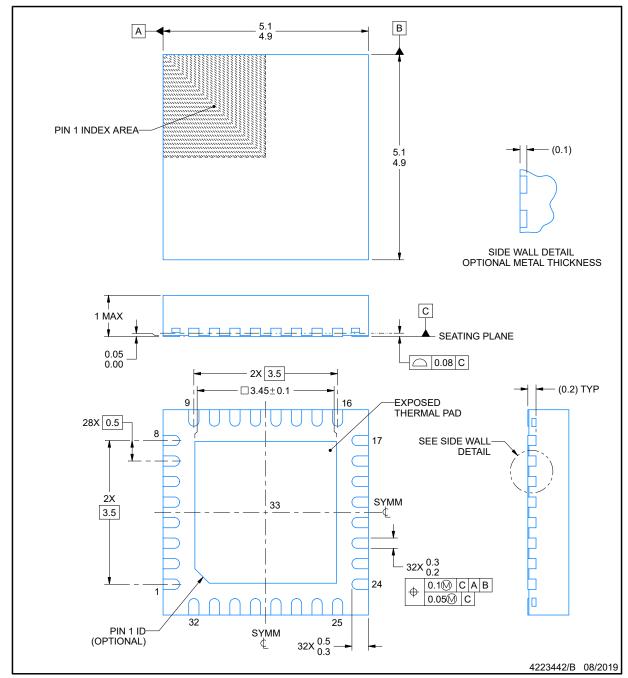
RHB0032E



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

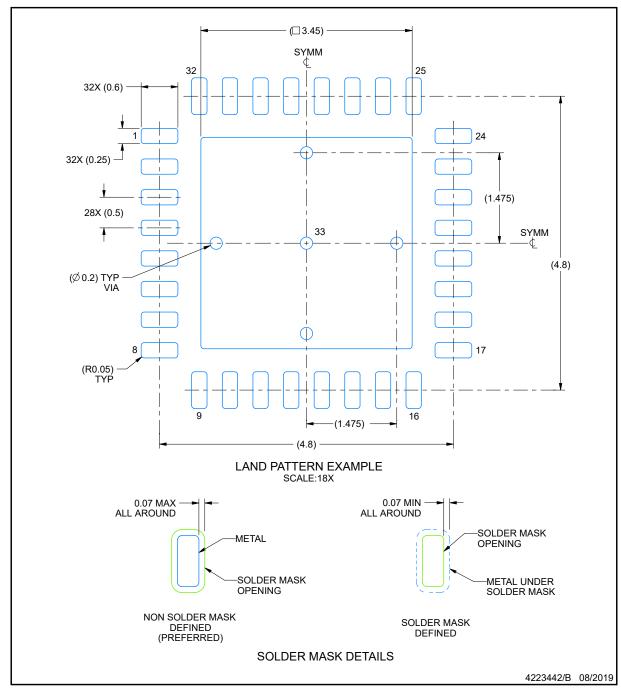


EXAMPLE BOARD LAYOUT

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

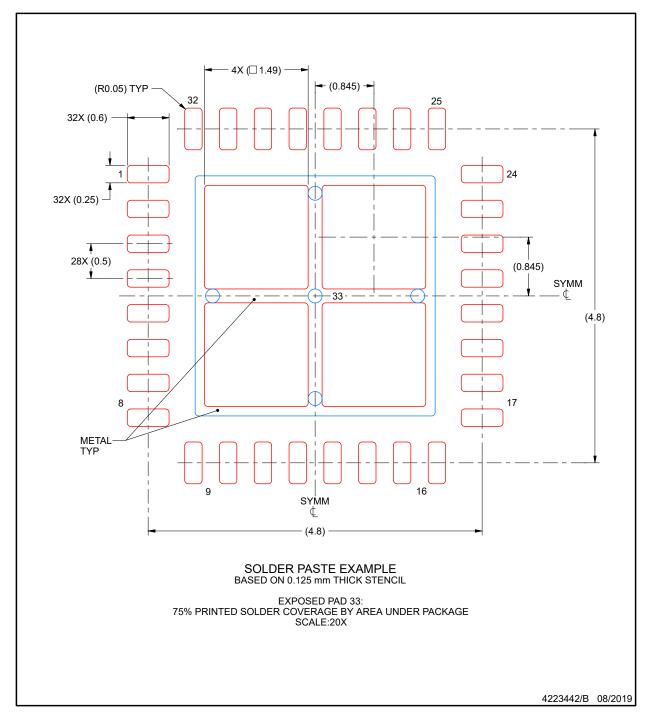


EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



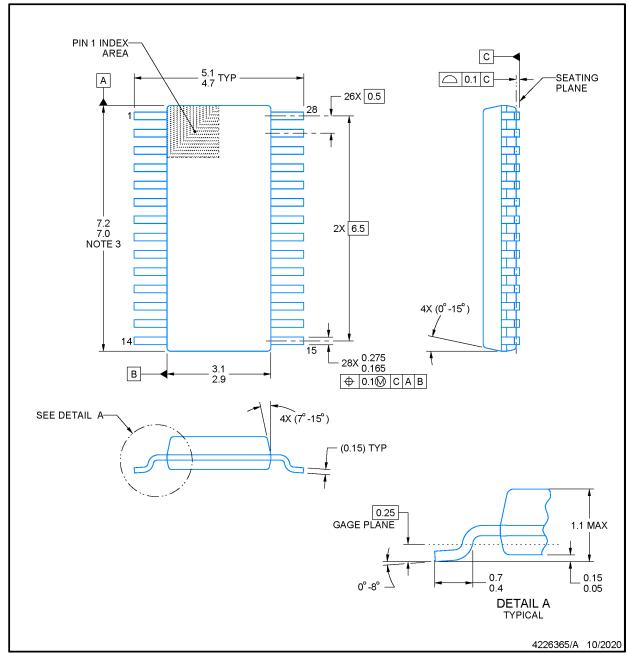
DGS0028A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. No JEDEC registration as of September 2020.
 5. Features may differ or may not be present.

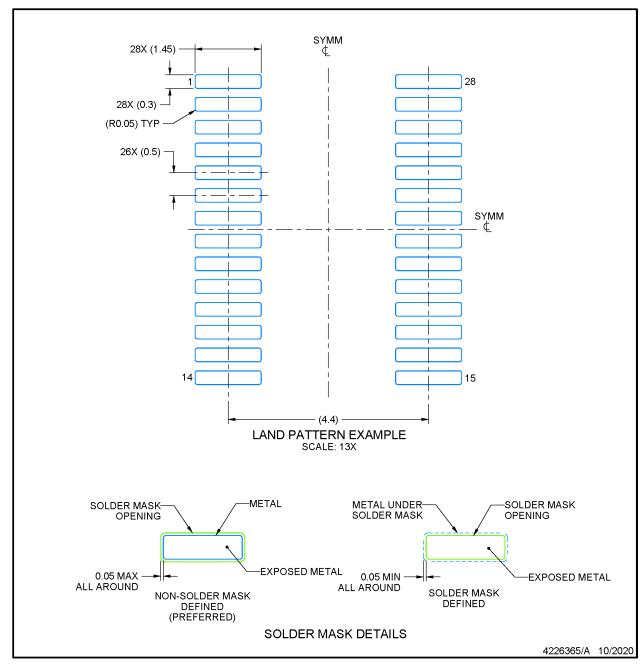


EXAMPLE BOARD LAYOUT

DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



- 6. Publication IPC-7351 may have alternate designs.7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
- 9. Size of metal pad may vary due to creepage requirement.
- 10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

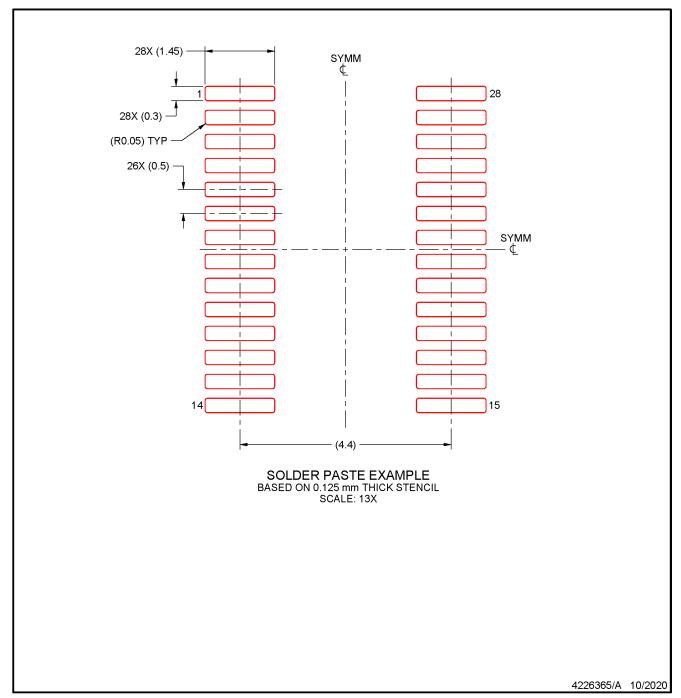


EXAMPLE STENCIL DESIGN

DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



^{11.} Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

^{12.} Board assembly site may have different recommendations for stencil design.

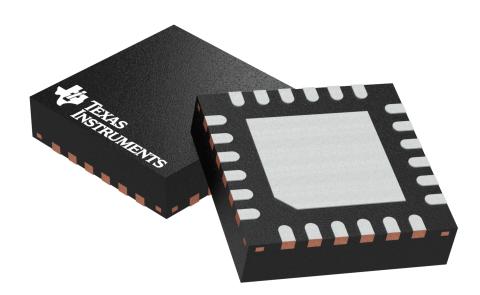
RGE 24



GENERIC PACKAGE VIEW

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4204104/H



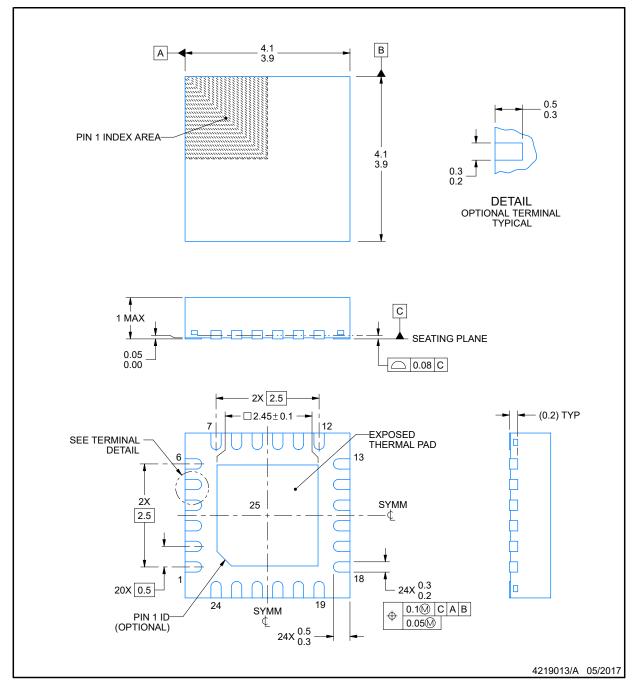
RGE0024B



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

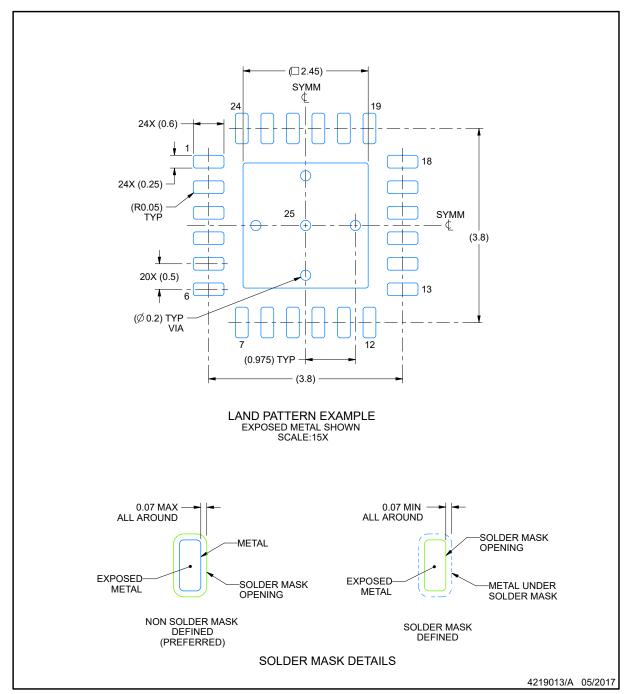


EXAMPLE BOARD LAYOUT

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

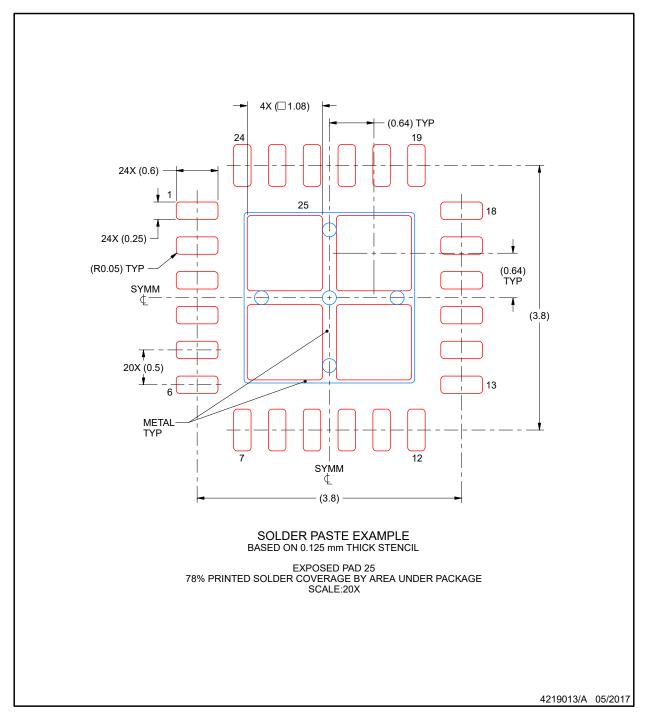


EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DGS0020A

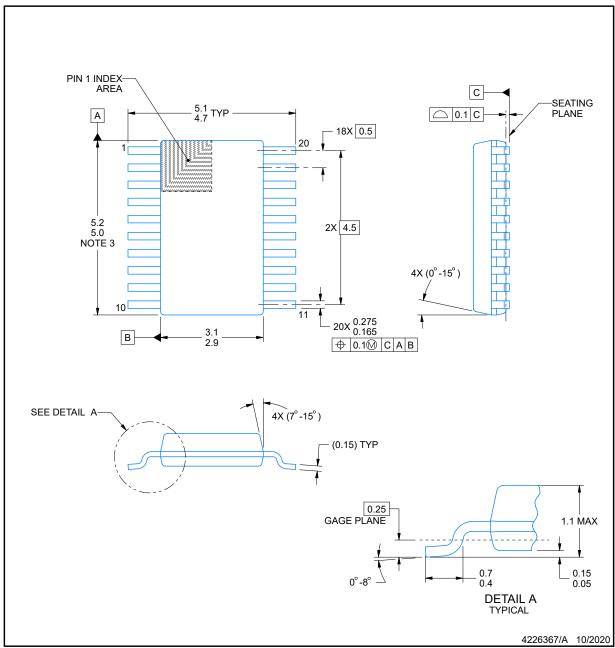




PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- 4. No JEDEC registration as of September 2020.
- 5. Features may differ or may not be present.

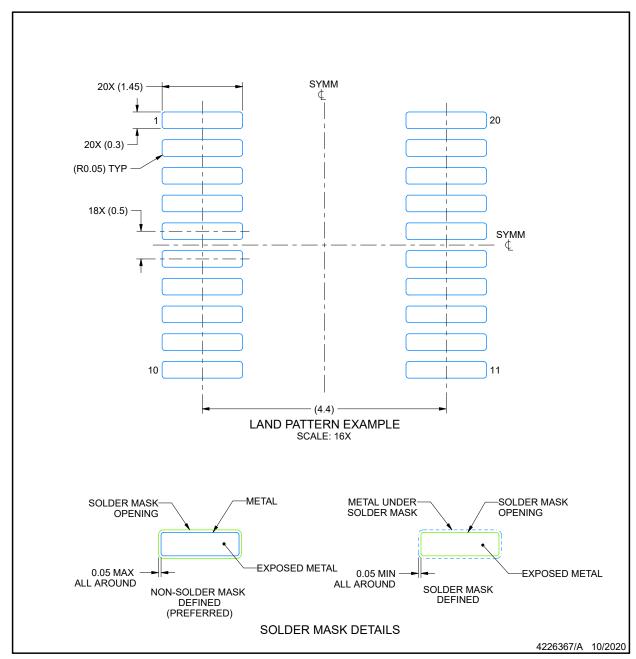


EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



- 6. Publication IPC-7351 may have alternate designs.
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.
 This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
- 9. Size of metal pad may vary due to creepage requirement.

 10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

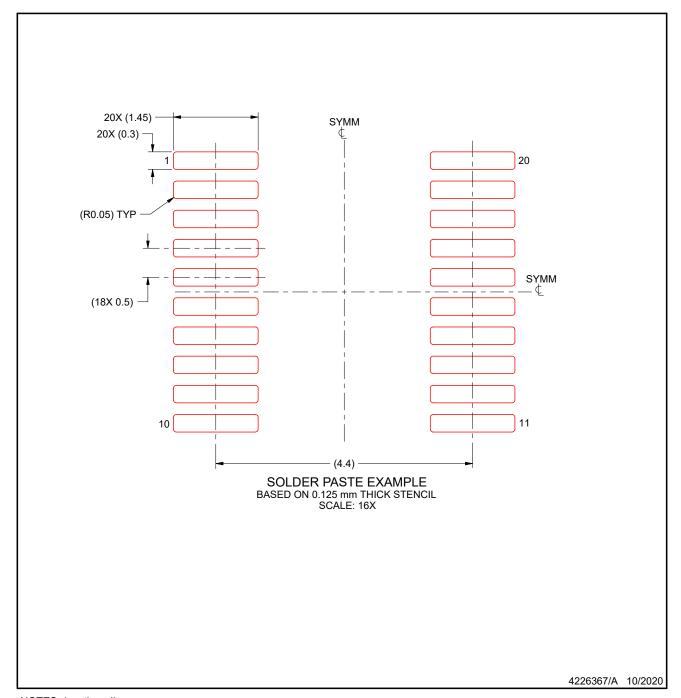


EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



^{11.} Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

^{12.} Board assembly site may have different recommendations for stencil design.



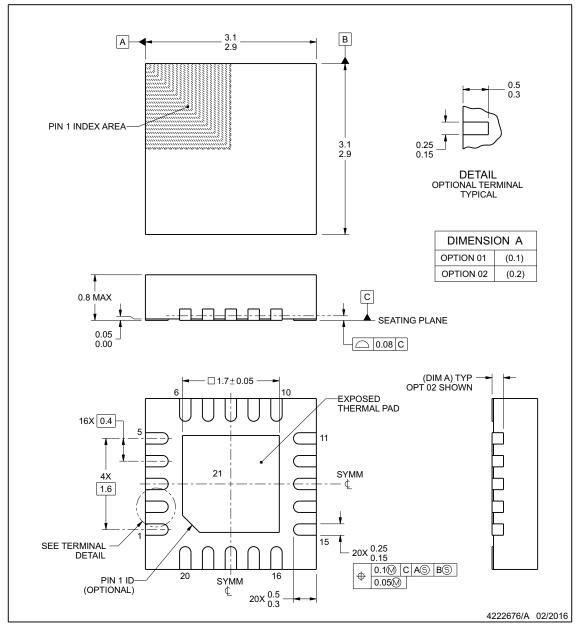
RUK0020B



PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

www.ti.com

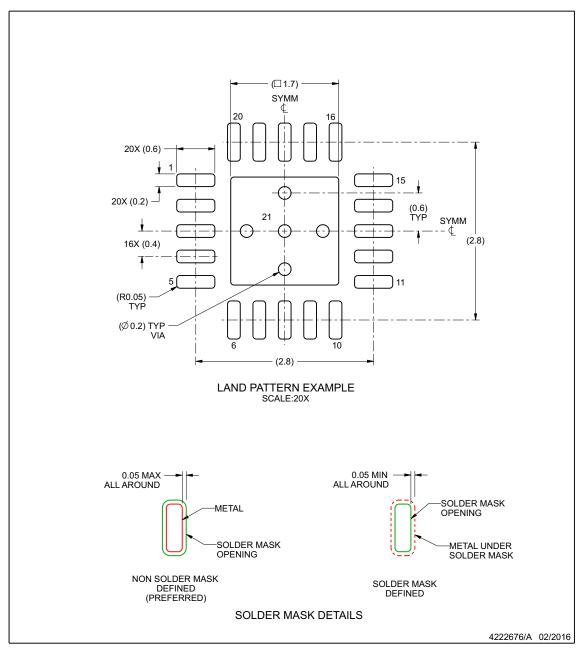


EXAMPLE BOARD LAYOUT

RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

www.ti.com

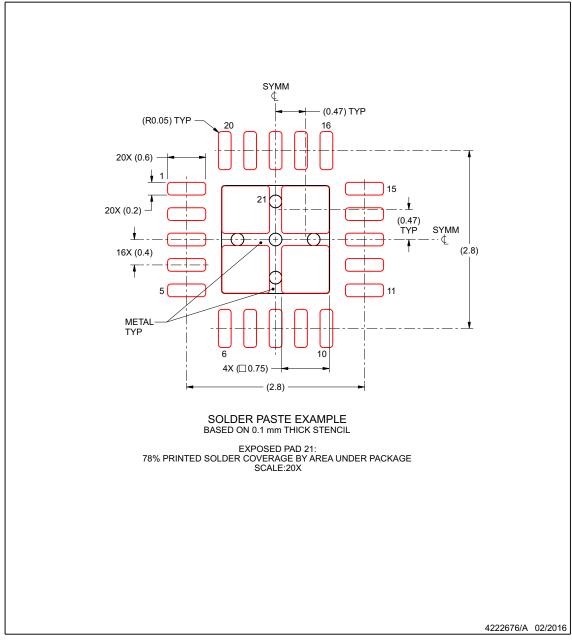


EXAMPLE STENCIL DESIGN

RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

www.ti.com

www.ti.com 21-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
						(4)	(5)		
MSPM0C1105SRGER	Active	Production	VQFN (RGE) 24	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MSPM0 C1105S
MSPM0C1105SRGZR	Active	Production	VQFN (RGZ) 48	4000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 C1105S
MSPM0C1105SRHBR	Active	Production	VQFN (RHB) 32	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 C1105S
MSPM0C1105SRUKR	Active	Production	WQFN (RUK) 20	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C1105S
MSPM0C1106SDGS20R	Active	Production	VSSOP (DGS) 20	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0C1106S
MSPM0C1106SDGS28R	Active	Production	VSSOP (DGS) 28	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	C1106S
MSPM0C1106SPTR	Active	Production	LQFP (PT) 48	1000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0C1106S
MSPM0C1106SRGER	Active	Production	VQFN (RGE) 24	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MSPM0 C1106S
MSPM0C1106SRGZR	Active	Production	VQFN (RGZ) 48	4000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 C1106S
MSPM0C1106SRHBR	Active	Production	VQFN (RHB) 32	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 C1106S
MSPM0C1106SRUKR	Active	Production	WQFN (RUK) 20	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C1106S
XMSM0C1106SDGS20R	Active	Preproduction	VSSOP (DGS) 20	5000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
XMSM0C1106SPTR	Active	Preproduction	LQFP (PT) 48	1000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
XMSM0C1106SRGER	Active	Preproduction	VQFN (RGE) 24	5000 LARGE T&R	=	Call TI	Call TI	-40 to 125	
XMSM0C1106SRGZR	Active	Preproduction	VQFN (RGZ) 48	4000 LARGE T&R	=	Call TI	Call TI	-40 to 125	
XMSM0C1106SRHBR	Active	Preproduction	VQFN (RHB) 32	5000 LARGE T&R	-	Call TI	Call TI	-40 to 125	

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

PACKAGE OPTION ADDENDUM

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(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF MSPM0C1106:

Automotive: MSPM0C1106-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



www.ti.com 24-Nov-2025

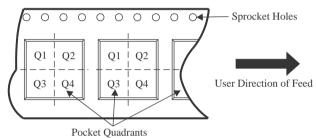
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSPM0C1105SRGER	VQFN	RGE	24	5000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSPM0C1105SRGZR	VQFN	RGZ	48	4000	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSPM0C1105SRHBR	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSPM0C1105SRUKR	WQFN	RUK	20	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
MSPM0C1106SDGS20R	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
MSPM0C1106SDGS28R	VSSOP	DGS	28	5000	330.0	16.4	5.5	7.4	1.45	8.0	16.0	Q1
MSPM0C1106SPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
MSPM0C1106SRGER	VQFN	RGE	24	5000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSPM0C1106SRGZR	VQFN	RGZ	48	4000	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSPM0C1106SRHBR	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSPM0C1106SRUKR	WQFN	RUK	20	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2



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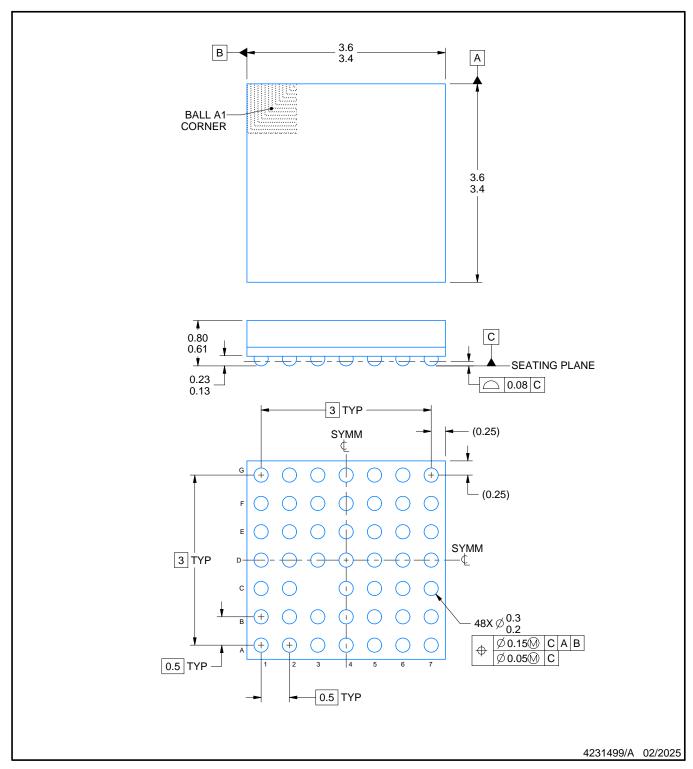


*All dimensions are nominal

All difficultions are norminal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSPM0C1105SRGER	VQFN	RGE	24	5000	367.0	367.0	35.0
MSPM0C1105SRGZR	VQFN	RGZ	48	4000	367.0	367.0	35.0
MSPM0C1105SRHBR	VQFN	RHB	32	5000	367.0	367.0	35.0
MSPM0C1105SRUKR	WQFN	RUK	20	5000	367.0	367.0	35.0
MSPM0C1106SDGS20R	VSSOP	DGS	20	5000	353.0	353.0	32.0
MSPM0C1106SDGS28R	VSSOP	DGS	28	5000	353.0	353.0	32.0
MSPM0C1106SPTR	LQFP	PT	48	1000	336.6	336.6	31.8
MSPM0C1106SRGER	VQFN	RGE	24	5000	367.0	367.0	35.0
MSPM0C1106SRGZR	VQFN	RGZ	48	4000	367.0	367.0	35.0
MSPM0C1106SRHBR	VQFN	RHB	32	5000	367.0	367.0	35.0
MSPM0C1106SRUKR	WQFN	RUK	20	5000	367.0	367.0	35.0



PLASTIC BALL GRID ARRAY



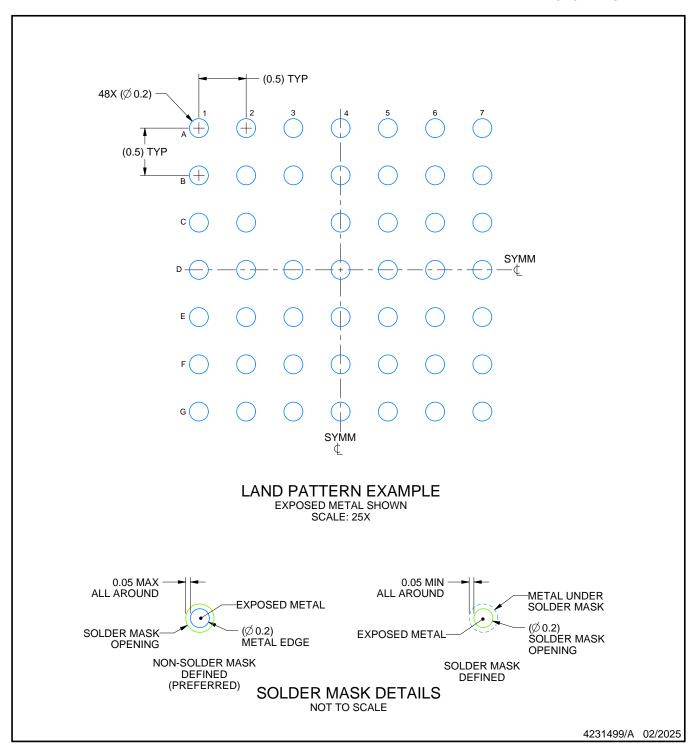
NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.



PLASTIC BALL GRID ARRAY

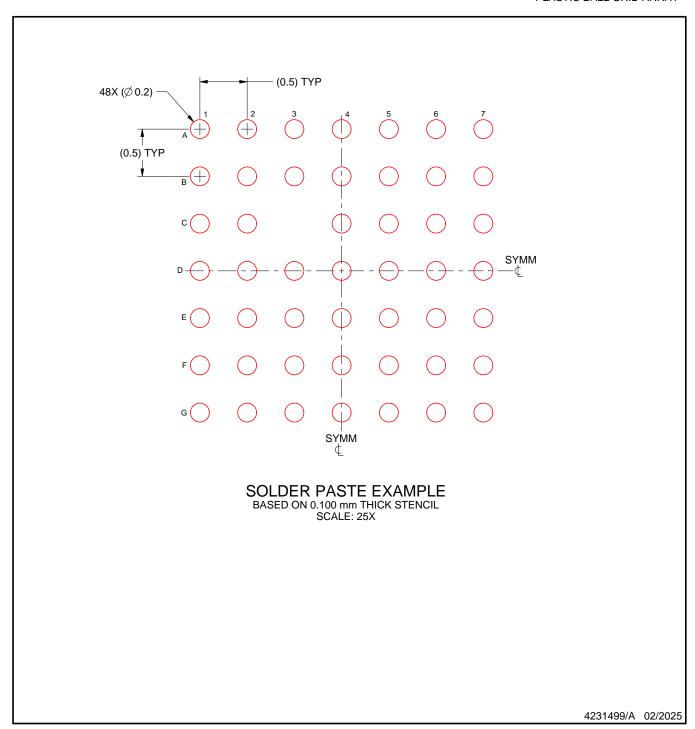


NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



PLASTIC BALL GRID ARRAY



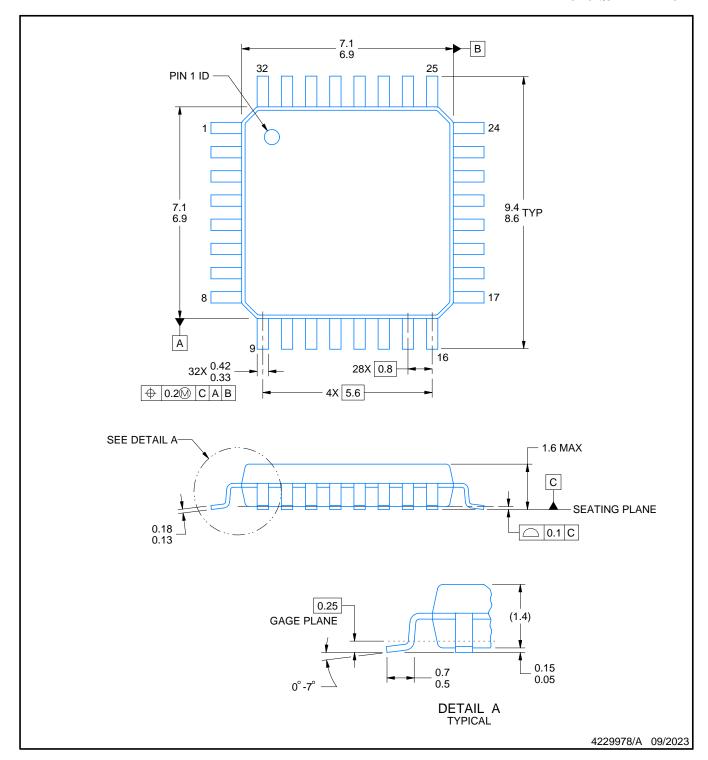
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.





PLASTIC QUAD FLATPACK



NOTES:

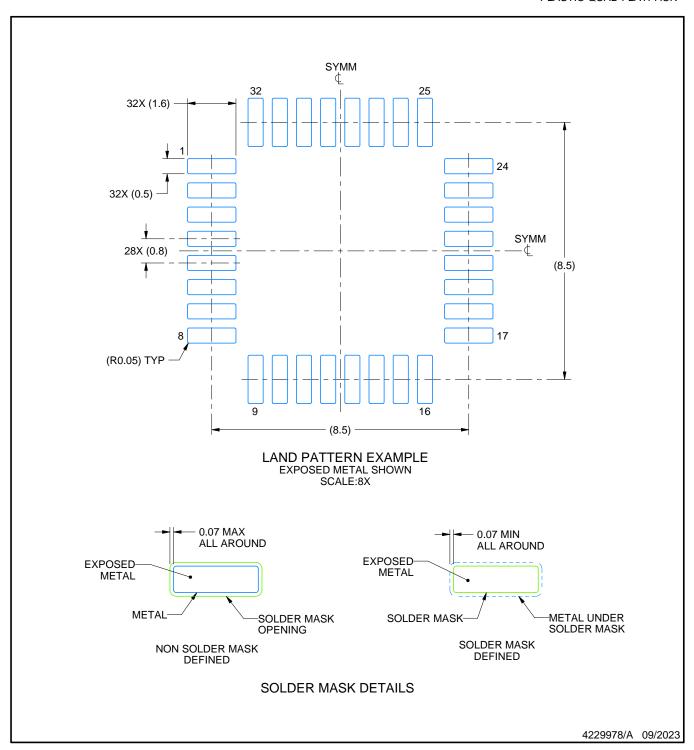
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Reference JEDEC registration MS-026.



PLASTIC QUAD FLATPACK

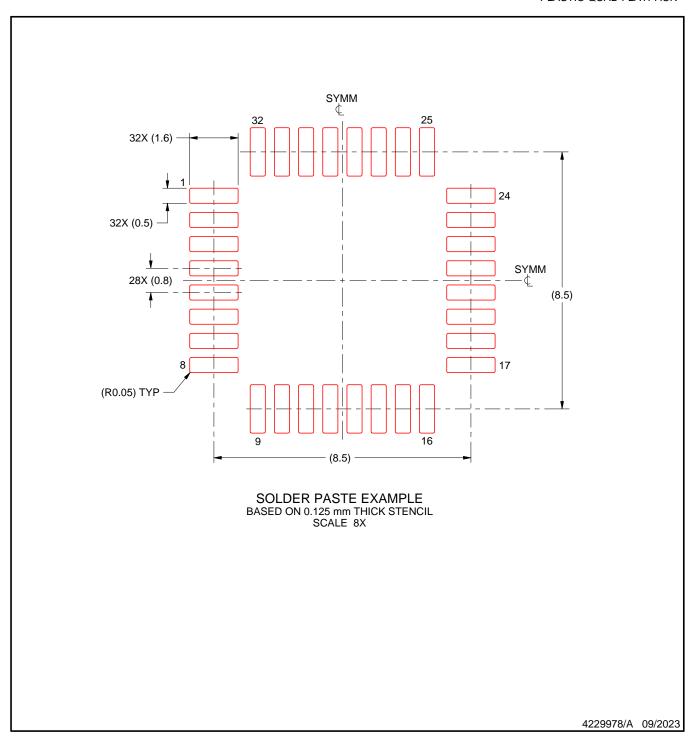


NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC QUAD FLATPACK

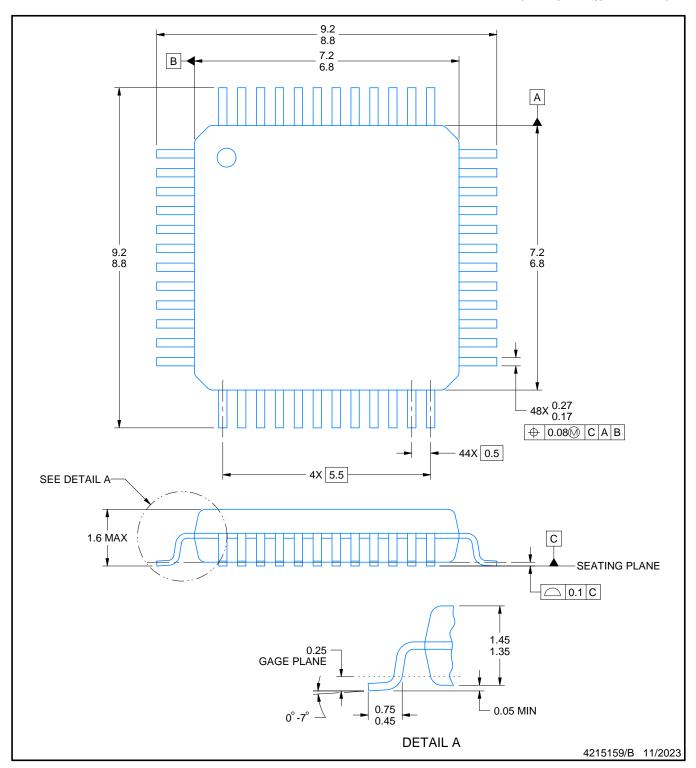


- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 7. Board assembly site may have different recommendations for stencil design.





LOW PROFILE QUAD FLATPACK

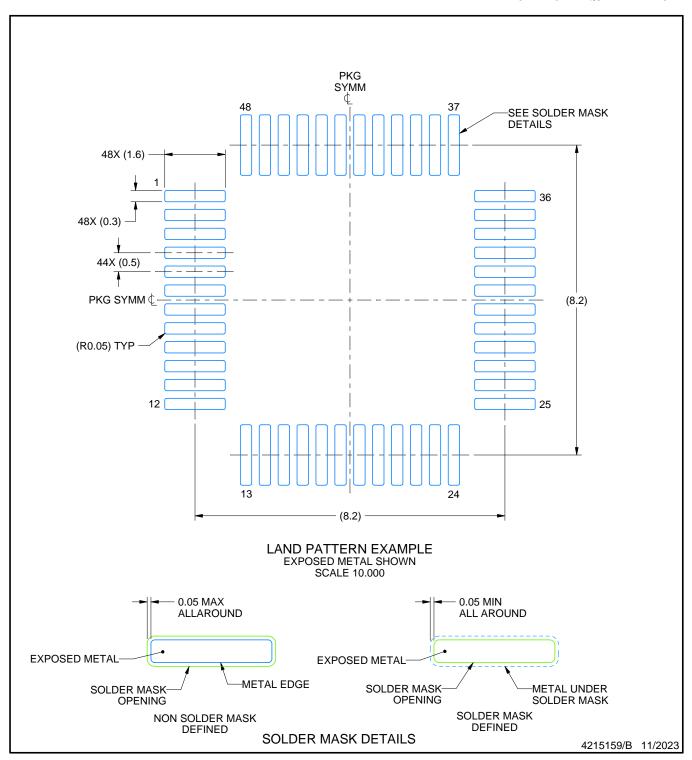


NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.
 Reference JEDEC registration MS-026.
 This may also be a thermally enhanced plastic package with leads conected to the die pads.



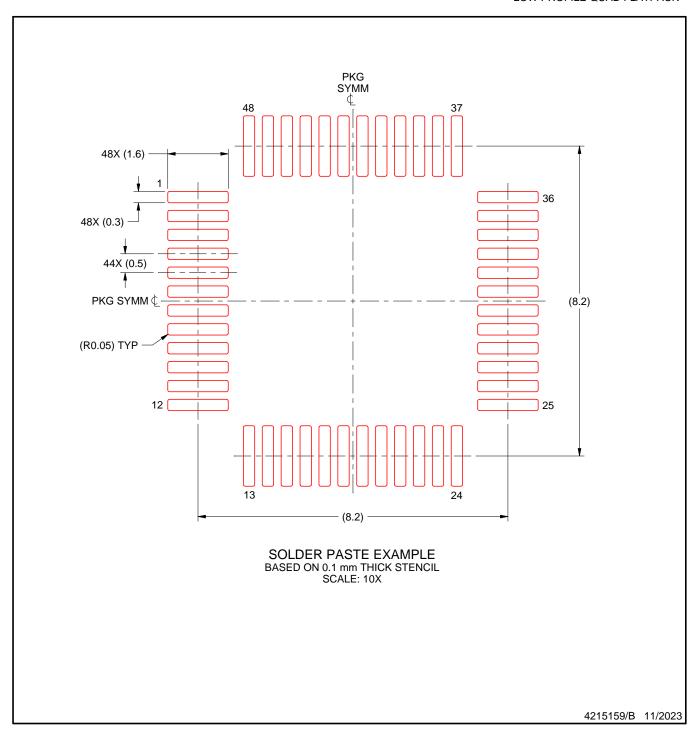
LOW PROFILE QUAD FLATPACK



- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



LOW PROFILE QUAD FLATPACK



- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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