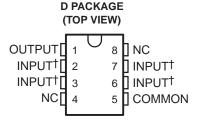
SLVS011D - OCTOBER 1982 - REVISED AUGUST 2003

- 3-Terminal Regulators
- Output Current Up To 100 mA
- No External Components Required
- Internal Thermal-Overload Protection
- Internal Short-Circuit Current Limiting
- Direct Replacement for Industry-Standard MC79L00 Series
- Available in 5% or 10% Selections

description/ordering information

This series of fixed negative-voltage integrated-circuit voltage regulators is designed for a wide range of applications. These include on-card regulation for elimination of noise and distribution problems associated with single-point



† Internally connected NC – No internal connection

LP PACKAGE (TOP VIEW)



regulation. In addition, they can be used to control series pass elements to make high-current voltage-regulator circuits. One of these regulators can deliver up to 100 mA of output current. The internal current-limiting and thermal-shutdown features essentially make the regulators immune to overload. When used as a replacement for a Zener-diode and resistor combination, these devices can provide an effective improvement in output impedance of two orders of magnitude, with lower bias current.

ORDERING INFORMATION

TJ	OUTPUT VOLTAGE TOLERANCE	NOMINAL OUTPUT VOLTAGE (V)	PACKAG	Ε [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
			SOIC (D)	Tube of 75	MC79L05ACD	701.054
		_	SOIC (D)	Reel of 2500	MC79L05ACDR	79L05A
		-5	TO 000 / TO 00 // D)	Bulk of 1000	MC79L05ACLP	701.0540
			TO-226 / TO-92 (LP)	Reel of 2000	MC79L05ACLPR	79L05AC
	5%		0010 (D)	Tube of 75	MC79L12ACD	701.404
			SOIC (D)	Reel of 2500	MC79L12ACDR	79L12A
0°C to 125°C		-12	TO 000 (TO 00 (I D)	Bulk of 1000	MC79L12ACLP	701.404.0
			TO-226 / TO-92 (LP)	Reel of 2000	MC79L12ACLPR	79L12AC
				Bulk of 1000	MC79L15ACLP	
		-15	TO-226 / TO-92 (LP)	Ammo of 2000	MC79L15ACLPM	79L15AC
				Reel of 2000	MC79L15ACLPR	1
	4.00/	-12	TO-226 / TO-92 (LP)	Bulk of 1000	MC79L12CLP	79L12C
	10%	-15	SOIC (D) Tube of 75		MC79L15CD	79L15C

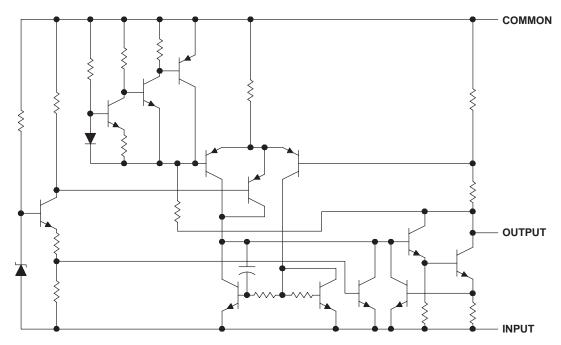
[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



equivalent schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage: MC79L05	30 V
MC79L12, MC79L15	35 V
Package thermal impedance, θ _{JA} (see Notes 1 and 2): D package	97°C/W
LP package	140°C/W
Operating free-air, case, or virtual junction temperature	150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T _{stg}	-65° C to 150° C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			MIN	MAX	UNIT
		MC79L05	-7	-20	
٧į	Input voltage	MC79L12	-14.5	-27	V
		MC79L15	-17.5	-30	
lo	Output current			100	mA
TJ	Operating virtual junction temperature		0	125	°C



NOTES: 1. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics at specified virtual junction temperature, $V_I = -10 \text{ V}$, $I_O = 40 \text{ mA}$ (unless otherwise noted)

DADAMETED	TTOT COMPLETIONS!	-	M	C79L05	С	МС	79L05A	C	
PARAMETER	TEST CONDITIONS†	TJ	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
		25°C	-4.6	-5	-5.4	-4.8	-5	-5.2	
Output voltage‡	$V_I = -7 \text{ V to } -20 \text{ V},$ $I_O = 1 \text{ mA to } 40 \text{ mA}$	0°C to 125°C	-4.5		-5.5	-4.75		-5.25	V
	$V_I = -10 \text{ V}, I_O = 1 \text{ mA to } 70 \text{ mA}$	0°C to 125°C	-4.5		-5.5	-4.75		-5.25	
	V _I = −7 V to −20 V	2500			200			150	.,
Input regulation	$V_{I} = -8 \text{ V to } -20 \text{ V}$	25°C			150			100	mV
Ripple rejection	$V_I = -8 \text{ V to } -18 \text{ V, f} = 120 \text{ Hz}$	25°C	40	49		41	49		dB
Outrast as audation	I _O = 1 mA to 100 mA	0500			60			60	>/
Output regulation	$I_O = 1 \text{ mA to } 40 \text{ mA}$	25°C			30			30	mV
Output noise voltage	f = 10 Hz to 100 kHz	25°C		40			40		μV
Dropout voltage	I _O = 40 mA	25°C		1.7			1.7		V
5:		25°C			6			6	
Bias current		125°C			5.5			5.5	mA
5:	V _I = -8 V to -20 V	202 / 4250			1.5			1.5	
Bias current change	$I_O = 1 \text{ mA to } 40 \text{ mA}$	0°C to 125°C			0.2			0.1	mA

[†] All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. ‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = -19 \text{ V}$, $I_O = 40 \text{ mA}$ (unless otherwise noted)

242445752		_	M	C79L12	С	МС	79L12A	C	
PARAMETER	TEST CONDITIONS†	TJ	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
		25°C	-11.1	-12	-12.9	-11.5	-12	-12.5	
Output voltage‡	$V_I = -14.5 \text{ V to } -27 \text{ V},$ $I_O = 1 \text{ mA to } 40 \text{ mA}$	0°C to 125°C	-10.8		-13.2	-11.4		-12.6	V
	$V_I = -19 \text{ V}, I_O = 1 \text{ mA to } 70 \text{ mA}$	0°C to 125°C	-10.8		-13.2	-11.4		-12.6	
	$V_{I} = -14.5 \text{ V to } -27 \text{ V}$	0500			250			250	.,
Input regulation	V _I = -16 V to -27 V	25°C		200				200	mV
Ripple rejection	$V_I = -15 \text{ V to } -25 \text{ V, f} = 120 \text{ Hz}$	25°C	36	42		37	42		dB
0	I _O = 1 mA to 100 mA	0500			100			100	.,
Output regulation	I _O = 1 mA to 40 mA	25°C			50			50	mV
Output noise voltage	f = 10 Hz to 100 kHz	25°C		80			80		μV
Dropout voltage	I _O = 40 mA	25°C		1.7			1.7		V
5.		25°C			6.5			6.5	•
Bias current		125°C			6			6	mA
D'an annual alcana	V _I = -16 V to -27 V	000 1- 40500			1.5			1.5	A
Bias current change	I _O = 1 mA to 40 mA	0°C to 125°C			0.2			0.1	mA

[†] All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. ‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.



MC79L00 SERIES NEGATIVE-VOLTAGE REGULATORS

SLVS011D - OCTOBER 1982 - REVISED AUGUST 2003

electrical characteristics at specified virtual junction temperature, $V_I = -23~V,\,I_O = 40~mA$ (unless otherwise noted)

DADAMETED	TTOT CONDITIONS!	_	M	C79L15	С	МС	79L15 <i>A</i>	/C	UNIT
PARAMETER	TEST CONDITIONS†	TJ	MIN	TYP	MAX	MIN	TYP	MAX	UNII
		25°C	-13.8	-15	-16.2	-14.4	-15	-15.6	
Output voltage‡	$V_I = -17.5 \text{ V to } -30 \text{ V},$ $I_O = 1 \text{ mA to } 40 \text{ mA}$	0°C to 125°C	-13.5		-16.5	-14.25		-15.75	V
	$V_1 = -23 \text{ V}, I_0 = 1 \text{ mA to } 70 \text{ mA}$	0°C to 125°C	-13.5		-16.5	-14.25		-15.75	
lament na medations	$V_I = -17.5 \text{ V to } -30 \text{ V}$	0500			300			300	\/
Input regulation	$V_{I} = -17.5 \text{ V to } -30 \text{ V}$	25°C			250			250	mV
Ripple rejection	V _I = -18.5 V to -28.5 V, f = 120 Hz	25°C	33	39		34	39		dB
Outside as and office	I _O = 1 mA to 100 mA	0500			150			150	>/
Output regulation	I _O = 1 mA to 40 mA	25°C			75			75	mV
Output noise voltage	f = 10 Hz to 100 kHz	25°C		90			90		μV
Dropout voltage	I _O = 40 mA	25°C		1.7			1.7		V
		25°C			6.5			6.5	
Bias current		125°C			6			6	mA
D'an annual alam	V _I = -20 V to -30 V	000 1- 40500			1.5			1.5	4
Bias current change	$I_O = 1 \text{ mA to } 40 \text{ mA}$	0°C to 125°C			0.2			0.1	mA

[†] All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. ‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.



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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
MC79L05ACD	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A
MC79L05ACD.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A
MC79L05ACDE4	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A
MC79L05ACDG4	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A
MC79L05ACDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A
MC79L05ACDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A
MC79L05ACDRE4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A
MC79L05ACDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A
MC79L05ACLP	Active	Production	TO-92 (LP) 3	1000 BULK	Yes	SN	N/A for Pkg Type	0 to 125	79L05AC
MC79L05ACLP.A	Active	Production	TO-92 (LP) 3	1000 BULK	Yes	SN	N/A for Pkg Type	0 to 125	79L05AC
MC79L05ACLPE3	Active	Production	TO-92 (LP) 3	1000 BULK	Yes	SN	N/A for Pkg Type	0 to 125	79L05AC
MC79L05ACLPR	Active	Production	TO-92 (LP) 3	2000 LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	79L05AC
MC79L05ACLPR.A	Active	Production	TO-92 (LP) 3	2000 LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	79L05AC
MC79L12ACD	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L12A
MC79L12ACD.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L12A
MC79L12ACDE4	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L12A
MC79L12ACDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L12A
MC79L12ACDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L12A
MC79L12ACLP	Active	Production	TO-92 (LP) 3	1000 BULK	Yes	SN	N/A for Pkg Type	0 to 125	79L12AC
MC79L12ACLP.A	Active	Production	TO-92 (LP) 3	1000 BULK	Yes	SN	N/A for Pkg Type	0 to 125	79L12AC
MC79L12ACLPE3	Active	Production	TO-92 (LP) 3	1000 BULK	Yes	SN	N/A for Pkg Type	0 to 125	79L12AC
MC79L12ACLPR	Active	Production	TO-92 (LP) 3	2000 LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	79L12AC
MC79L12ACLPR.A	Active	Production	TO-92 (LP) 3	2000 LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	79L12AC
MC79L12ACLPRE3	Active	Production	TO-92 (LP) 3	2000 LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	79L12AC
MC79L12CLP	Active	Production	TO-92 (LP) 3	1000 BULK	Yes	SN	N/A for Pkg Type	0 to 125	79L12C
MC79L12CLP.A	Active	Production	TO-92 (LP) 3	1000 BULK	Yes	SN	N/A for Pkg Type	0 to 125	79L12C
MC79L15ACLP	Active	Production	TO-92 (LP) 3	1000 BULK	Yes	SN	N/A for Pkg Type	0 to 125	79L15AC
MC79L15ACLP.A	Active	Production	TO-92 (LP) 3	1000 BULK	Yes	SN	N/A for Pkg Type	0 to 125	79L15AC
MC79L15ACLPE3	Active	Production	TO-92 (LP) 3	1000 BULK	Yes	SN	N/A for Pkg Type	0 to 125	79L15AC



14-Oct-2025



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Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
MC79L15ACLPR	Active	Production	TO-92 (LP) 3	2000 LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	79L15AC
MC79L15ACLPR.A	Active	Production	TO-92 (LP) 3	2000 LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	79L15AC
MC79L15ACLPRE3	Active	Production	TO-92 (LP) 3	2000 LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	79L15AC

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

www.ti.com 23-May-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MC79L05ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
MC79L12ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 23-May-2025



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MC79L05ACDR	SOIC	D	8	2500	353.0	353.0	32.0
MC79L12ACDR	SOIC	D	8	2500	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

www.ti.com 23-May-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MC79L05ACD	D	SOIC	8	75	507	8	3940	4.32
MC79L05ACD.A	D	SOIC	8	75	507	8	3940	4.32
MC79L05ACDE4	D	SOIC	8	75	507	8	3940	4.32
MC79L05ACDG4	D	SOIC	8	75	507	8	3940	4.32
MC79L12ACD	D	SOIC	8	75	507	8	3940	4.32
MC79L12ACD.A	D	SOIC	8	75	507	8	3940	4.32
MC79L12ACDE4	D	SOIC	8	75	507	8	3940	4.32



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



TO-92 - 5.34 mm max height

TO-92



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.
- 3. Lead dimensions are not controlled within this area. 4. Reference JEDEC TO-226, variation AA.
- 5. Shipping method:

 - a. Straight lead option available in bulk pack only.
 b. Formed lead option available in tape and reel or ammo pack.
 - c. Specific products can be offered in limited combinations of shipping medium and lead options.
 - d. Consult product folder for more information on available options.



TO-92





TO-92





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